

Features

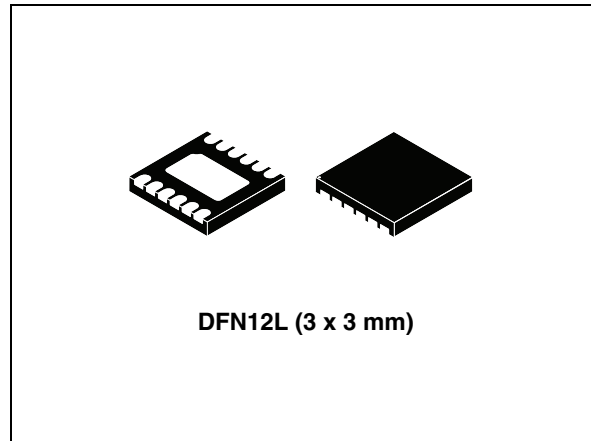
- Step-up and inverter converters
- Operating input voltage range from 2.5 V to 4.5 V
- Synchronous rectification for both DC-DC converters
- Minimum 250 mA output current
- 4.6 V fixed positive output voltage
- Programmable negative voltage by S_{WIRE} from -2.4 V to -6.4 V at 100 mV steps
- Typical efficiency 85%
- Pulse skipping mode in light load condition
- 1.5 MHz PWM mode control switching frequency
- TDMA noise high immunity
- Enable pin for shutdown mode
- Low quiescent current in shutdown mode
- Soft-start with inrush current protection
- Overtemperature protection
- Temperature range -40 °C to 85 °C
- True-shutdown mode
- Fast outputs discharge circuit after shutdown
- Short-circuit protection
- Package DFN12L (3 x 3) 0.6 mm height

Applications

- Active matrix AMOLED power supply in portable devices
- Cellular phones
- Camcorders and digital still cameras
- Multimedia players

Table 1. Device summary

| Order code | Positive voltage | Negative voltage | Package | Packaging |
|-------------|------------------|------------------|------------------|---------------------|
| STOD13ATPUR | 4.6V | -2.4V to -6.4V | DFN12L (3 x 3mm) | 3000 parts per reel |



Description

The STOD13A is a dual DC-DC converter for AMOLED display panels. It integrates a step-up and an inverting DC-DC converter making it particularly suitable for battery operated products, in which the major concern is overall system efficiency. It works in pulse skipping mode during low load conditions and PWM-MODE at 1.5 MHz frequency for medium/high load conditions. The high frequency allows the value and size of external components to be reduced. The Enable pin allows the device to be turned off, therefore reducing the current consumption to less than 1 μ A. The negative output voltage can be programmed by an MCU through a dedicated pin which implements single-wire protocol. Soft-start with controlled inrush current limit, thermal shutdown and short-circuit protection are integrated functions of the device.

Contents

- 1 Schematic 3**
- 2 Pin configuration 5**
- 3 Maximum ratings 6**
- 4 Electrical characteristics 7**
- 5 Typical performance characteristics 10**
- 6 Detailed description 12**
 - 6.1 S_{WIRE} 12
 - 6.1.1 S_{WIRE} features and benefits 12
 - 6.1.2 S_{WIRE} protocol 12
 - 6.1.3 S_{WIRE} basic operations 12
 - 6.2 Negative output voltage levels 13
- 7 Application information 15**
 - 7.1 External passive components 15
 - 7.1.1 Inductor selection 15
 - 7.1.2 Input and output capacitor selection 15
 - 7.2 Recommended PCB layout 16
- 8 Detailed description 18**
 - 8.1 General description 18
 - 8.1.1 Multiple operation modes 18
 - 8.1.2 Enable pin 19
 - 8.1.3 Soft-start and inrush current limiting 19
 - 8.1.4 Undervoltage lockout 19
 - 8.1.5 Overtemperature protection 19
 - 8.1.6 Short-circuit protection 19
 - 8.1.7 Fast discharge 19
- 9 Package mechanical data 20**

10 **Revision history** **23**

1 Schematic

Figure 1. Application schematic

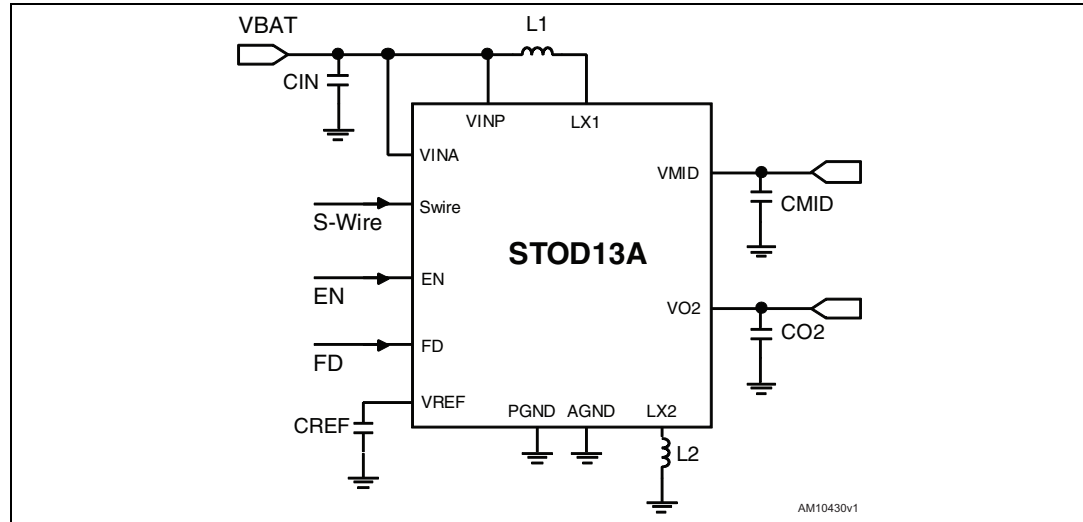


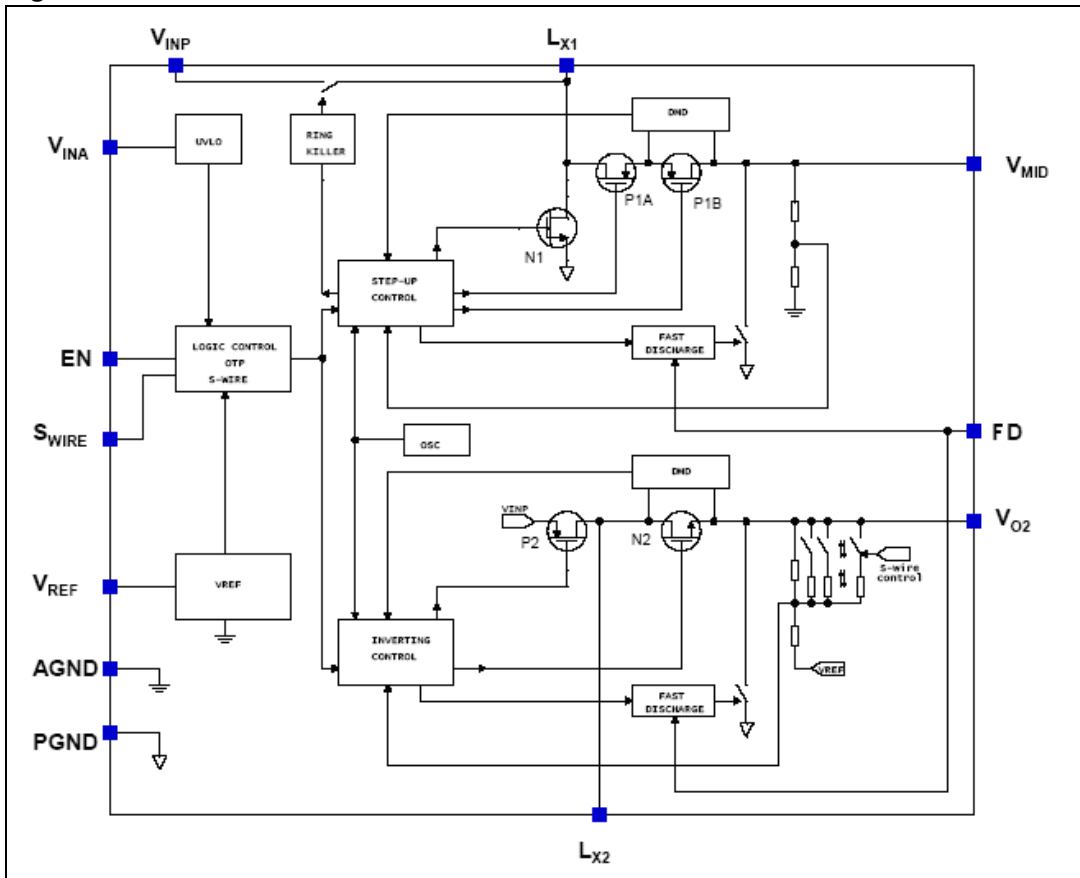
Table 2. Typical external components

| Comp. | Manufacturer | Part number | Value | Size | Ratings |
|-------------------------------|--------------|--------------------------|-------|-----------------|-------------------------------|
| L ₁ ⁽¹⁾ | CoilCraft | LPS4012-472ML | 4.7μH | 4.0 x 4.0 x 1.2 | ±20%, curr. 1.7A, res. 0.175Ω |
| | Murata | LQH3NPN4R7MJ0 | | 3.0 x 3.0 x 1.1 | ±20%, curr. 1.1A, res. 0.156Ω |
| | SEMCO | CIG22B4R7MNE | | 2.5 x 2.0 x 1.0 | ±20%, curr. 1.1A, res. 0.300Ω |
| | ABCO | LPF2810T-4R7M | | 2.8 x 2.8 x 1.0 | ±20%, curr. 0.85A, res. 0.33Ω |
| | | | | | |
| L ₂ ⁽²⁾ | CoilCraft | LPS4012-472ML | 4.7μH | 4.0 x 4.0 x 1.2 | ±20%, curr. 1.7A, res. 0.175Ω |
| | Murata | LQH3NPN4R7MJ0 | | 3.0 x 3.0 x 1.1 | ±20%, curr. 1.1A, res. 0.156Ω |
| | TOKO | DFE252012C 1239AS-H-4R7N | | 2.5 x 2.0 x 1.2 | ±30%, curr. 1.2A, res. 0.252Ω |
| C _{IN} | Murata | GRM219R61A106KE44 | 2 x | 0805 | ±10%, X5R, 10V |
| | Taiyo Yuden | LMK212BJ106KD-T | 10μF | 0805 | ±10%, X5R, 10V |
| C _{MID} | Murata | GRM219R61A106KE44 | 10μF | 0805 | ±10%, X5R, 10V |
| | Taiyo Yuden | LMK212BJ106KD-T | | 0805 | ±10%, X5R, 10V |
| C _{CO2} | Murata | GRM219R61A106KE44 | 2 x | 0805 | ±10%, X5R, 10V |
| | Taiyo Yuden | LMK212BJ106KD-T | 10μF | 0805 | ±10%, X5R, 10V |
| C _{REF} | Murata | GRM185R60J105KE26 | 1μF | 0603 | ±10%, X5R, 6.3V |
| | Taiyo Yuden | JMK107BJ105KK-T | | 0603 | ±10%, X5R, 6.3V |

1. A 250 mA load can be provided with inductor saturation current as a minimum of 0.9 A.
2. At -6.4 V, a 250 mA load can be provided with inductor saturation current as a minimum of 1.5 A. See [Section 7.1.1](#).

Note: All the above components refer to the typical application performance characteristics. Operation of the device is not limited to the choice of these external components. Inductor values ranging from 3.3 μH to 6.8 μH can be used together with the STOD13A.

Figure 2. Block schematic



2 Pin configuration

Figure 3. Pin configuration (top view)

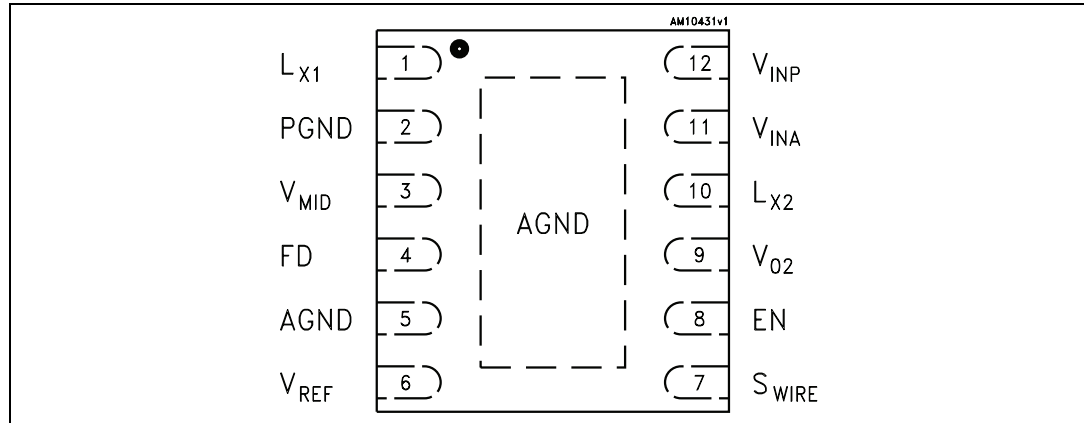


Table 3. Pin description

| Pin name | Pin number | Description |
|-------------------|-------------|--|
| L _{X1} | 1 | Boost converter switching node. |
| PGND | 2 | Power ground pin. |
| V _{MID} | 3 | Boost converter output voltage. |
| FD | 4 | Fast discharge control pin. When pulled LOW the fast discharge after shutdown is active. When pulled HIGH the fast discharge is OFF. |
| AGND | 5 | Signal ground pin. This pin must be connected to the power ground layer. |
| V _{REF} | 6 | Voltage reference output. 1μF bypass capacitor must be connected between this pin and AGND. |
| S _{WIRE} | 7 | Negative voltage setting pin. |
| EN | 8 | Enable control pin. high = converter on; low = converter in shutdown mode. |
| V _{O2} | 9 | Inverting converter output voltage. |
| L _{X2} | 10 | Inverting converter switching node. |
| V _{INA} | 11 | Analogic input supply voltage. |
| V _{INP} | 12 | Power input supply voltage. |
| | Exposed Pad | Internally connected to AGND. Exposed pad must be connected to ground layers in the PCB layout in order to guarantee proper operation of the device. |

3 Maximum ratings

Table 4. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|--------------------|--|------------------------|------|
| V_{INA}, V_{INP} | DC supply voltage | - 0.3 to 6 | V |
| EN, S_{WIRE} | Logic input pins | - 0.3 to 4.6 | V |
| FD | Logic input pin | - 0.3 to $V_{INA}+0.3$ | V |
| ILX_2 | Inverting converter switching current | Internally limited | A |
| LX_2 | Inverting converter switching node voltage | - 10 to $V_{INP}+0.3$ | V |
| VO_2 | Inverting converter output voltage | - 10 to AGND+0.3 | V |
| V_{MID} | Step-up converter output voltage | -0.3 to 6 | V |
| LX_1 | Step-up converter switching node voltage | - 0.3 to $V_{MID}+0.3$ | V |
| ILX_1 | Step-up converter's switching current | Internally limited | A |
| V_{REF} | Reference voltage | - 0.3 to 3 | V |
| P_D | Power dissipation | Internally limited | mW |
| T_{ST} | Storage temperature range | - 65 to 150 | °C |
| T_J | Maximum junction temperature | +150 | °C |
| ESD | Human body model protection | ± 2 | kV |
| | Machine body model protection | ± 200 | V |

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 5. Thermal data

| Symbol | Parameter | Value | Unit |
|------------|--|-------|------|
| R_{thJA} | Thermal resistance junction-ambient | 33 | °C/W |
| R_{thJC} | Thermal resistance junction-case (FR-4 PCB) ⁽¹⁾ | 2.12 | °C/W |

1. The package is mounted on a 4-layer (2S2P) JEDEC board as per JESD51-7.

4 Electrical characteristics

$T_J = 25\text{ }^\circ\text{C}$, $V_{INA} = V_{INP} = 3.7\text{ V}$, $I_{MID,O2} = 30\text{ mA}$, $C_{IN} = 2 \times 10\text{ }\mu\text{F}$, $C_{MID} = 10\text{ }\mu\text{F}$,
 $C_{O2} = 2 \times 10\text{ }\mu\text{F}$, $C_{REF} = 1\text{ }\mu\text{F}$, $L1 = L2 = 4.7\text{ }\mu\text{H}$, $V_{EN} = 2\text{ V}$, $V_{MID} = 4.6\text{ V}$, $V_{O2} = -4.9\text{ V}$ unless
 otherwise specified.

Table 6. Electrical characteristics

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------------------------------|--|---|-------|-------|-------|---------------|
| General section | | | | | | |
| V_{INA}, V_{INP} | Supply input voltage | | 2.5 | 3.7 | 4.5 | V |
| UVLO_H | Undervoltage lockout HIGH | V_{INA} rising | | 2.22 | 2.25 | V |
| UVLO_L | Undervoltage lockout LOW | V_{INA} Falling | 1.9 | 2.18 | | V |
| I_{VI} | Input current | No load condition | | 1.7 | 2.1 | mA |
| I_{Q_SH} | Shutdown current | $V_{EN}=\text{GND}$; $T_J=-40^\circ\text{C}$ to $+85^\circ\text{C}$ | | | 1 | μA |
| $V_{EN\ H}$ | Enable high threshold | $V_{INA}=2.5\text{V}$ to 4.5V , $T_J=-40^\circ\text{C}$ to $+85^\circ\text{C}$ | 1.2 | | | V |
| $V_{EN\ L}$ | Enable low threshold | | | | 0.4 | |
| I_{EN} | Enable input current | $V_{EN}=V_{INA}=4.5\text{V}$; $T_J=-40^\circ\text{C}$ to $+85^\circ\text{C}$ | | | 1 | μA |
| $V_{FD\ H}$ | Fast discharge high threshold | $V_{INA}=2.5\text{V}$ to 4.5V , $T_J=-40^\circ\text{C}$ to $+85^\circ\text{C}$ | 1.2 | | | V |
| $V_{FD\ L}$ | Fast discharge low threshold | | | | 0.4 | |
| fs | Switching frequency | PWM mode | 1.35 | 1.5 | 1.65 | MHz |
| D1_MAX | Step-up maximum duty cycle | No load | | 87 | | % |
| D2_MAX | Inverting maximum duty cycle | No load | | 87 | | % |
| | Total system efficiency | $I_{MID,O2}=10$ to 30mA , $V_{MID}=4.6\text{V}$, $V_{O2}=-4.9\text{V}$ | | 78 | | % |
| | | $I_{MID,O2}=30$ to 150mA , $V_{MID}=4.6\text{V}$, $V_{O2}=-4.9\text{V}$ | | 85 | | |
| | | $I_{MID,O2}=150$ to 250mA , $V_{MID}=4.6\text{V}$, $V_{O2}=-4.9\text{V}$ | | | 82 | |
| V_{REF} | Reference voltage | $I_{REF}=10\mu\text{A}$ | 1.208 | 1.220 | 1.232 | V |
| I_{REF} | Reference current capability | At 98.5% of no load reference voltage | 100 | | | μA |
| Step-up converter section | | | | | | |
| V_{MID} | Positive output voltage | | | 4.6 | | V |
| | Positive output voltage total variation | $V_{INA}=V_{INP}=2.9\text{V}$ to 4.5V ; $I_{MID}=5\text{mA}$ to 250mA , I_{O2} no load $T_J = -40^\circ\text{C}$ to $+85^\circ\text{C}$ | -0.8 | | 0.8 | % |
| $\Delta V_{MID\ LT}$ | Line transient | $V_{INA,P}=3.4\text{V}$ to 2.9V , $I_{MID}=100\text{mA}$; $T_R=T_F=10\mu\text{s}$ | | -10 | | mV |

Table 6. Electrical characteristics (continued)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|------------------------------------|--|---|-------|----------|-------|------------|
| $\Delta V_{MID T}$ | Load transient response | $I_{MID}=3$ to 30mA and $I_{MID}=30$ to 3mA, $T_R=T_F=150\mu s$ | | ± 20 | | mV |
| | | $I_{MID}=10$ to 100mA and $I_{MID}=100$ to 10mA, $T_R=T_F=150\mu s$ | | ± 25 | | mV |
| TDMA Noise | Undershoot/overshoot | $I_{MID}=10$ to 100mA; I_{O2} no load ⁽¹⁾ | | ± 20 | | mV |
| | Static variation between low and high V_{IN} level | | | 4 | | |
| $I_{MID MAX}$ | Maximum output current | $V_{INA,P}=2.9V$ to 4.5V | 250 | | | mA |
| $I-L_{1MAX}$ | Step-up inductor peak current | V_{MID} 10% below nominal value | 1.08 | | 1.32 | A |
| R_{DSONP1} | P-channel static drain-source ON resistance | $V_{INA}=V_{INP}=3.7V$, $I_{SW-P1}=100mA$ | | 1.0 | 2.0 | Ω |
| R_{DSONN1} | N-channel static drain-source ON resistance | $V_{INA}=V_{INP}=3.7V$, $I_{SW-N1}=100mA$ | | 0.4 | 1.0 | Ω |
| Inverting converter section | | | | | | |
| V_{O2} | Negative output voltage range | 41 different values set by the S_{WIRE} pin (see Section 6.1.2) | -6.4 | | -2.4 | V |
| | Negative output voltage | | | -4.9 | | V |
| | Negative output voltage total variation | $V_{INA}=V_{INP}=2.9V$ to 4.5V; $I_{O2}=5mA$ to 250mA, I_{MID} no load $T_J=-40^\circ C$ to $+85^\circ C$ | -1.7 | | 1.7 | % |
| $\Delta V_{O2 LT}$ | Line transient | $V_{INA,P}=3.4V$ to 2.9V, $I_{O2}=100mA$, $T_R=T_F=10\mu s$ | | +10 | | mV |
| $\Delta V_{O2 T}$ | Load transient response | $I_{O2}=3$ to 30mA and $I_{O2}=30$ to 3mA, $T_R=T_F=150\mu s$ | | ± 20 | | mV |
| | | $I_{O2}=10$ to 100mA and $I_{O2}=100$ to 10mA, $T_R=T_F=150\mu s$ | | ± 25 | | mV |
| TDMA Noise | Undershoot/overshoot | $I_{O2}=10$ to 100mA; I_{MID} no load ⁽¹⁾ | | ± 20 | | mV |
| | Static variation between low and high V_{IN} level | | | 5 | | |
| $I_{O2 MAX}$ | Maximum output current | $V_{INA,P}=2.9V$ to 4.5V | -250 | | | mA |
| $I-L_{2MAX}$ | Inverting peak current | V_{O2} below 10% nominal value | -1.43 | | -1.17 | A |
| R_{DSONP2} | P-channel static drain-source ON resistance | $V_{INA}=V_{INP}=3.7V$, $I_{SW-P2}=100mA$ | | 0.42 | 0.8 | Ω |
| R_{DSONN2} | N-channel Static Drain-source ON resistance | $V_{INA}=V_{INP}=3.7V$, $I_{SW-N2}=100mA$ | | 0.43 | 0.8 | Ω |
| Thermal shutdown | | | | | | |
| OTP | Overtemperature protection | | | 140 | | $^\circ C$ |
| OTP _{HYST} | Overtemperature protection hysteresis | | | 15 | | $^\circ C$ |

Table 6. Electrical characteristics (continued)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------------------|----------------|--|------|------|------|----------|
| Discharge resistor | | | | | | |
| R_{DIS} | Resistor value | No load, EN=SW=FD=Low | | 400 | | Ω |
| T_{DIS} | Discharge time | No load, EN=SW=FD=Low, V_{MID}^- V_{O2} at 10% of nominal value | | 10 | | ms |

1. $V_{INA,P} = 4.2$ to 3.7 V, 3.7 to 3.2 V, 3.4 to 2.9 V, $f = 200$ Hz; $t_{ON} = 3.65$ ms; $t_{OFF} = 1.25$ ms; $T_R = T_F = 10$ μ s, pulse signal.

5 Typical performance characteristics

$V_{INA} = V_{INP} = 3.7\text{ V}$, $V_{O2} = -4.9\text{ V}$, $T_J = 25^\circ\text{C}$; see [Table 1](#) for external components used in the tests below.

Figure 4. Maximum power output vs. input voltage ($V_{INA} = V_{INP} = 2.9$ to 4.2 V)

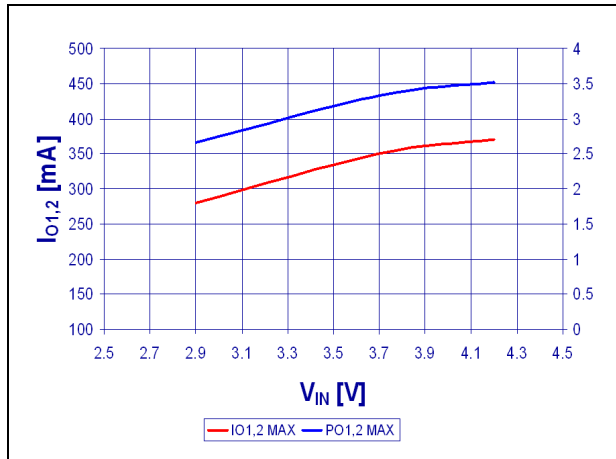


Figure 5. Efficiency vs. output current

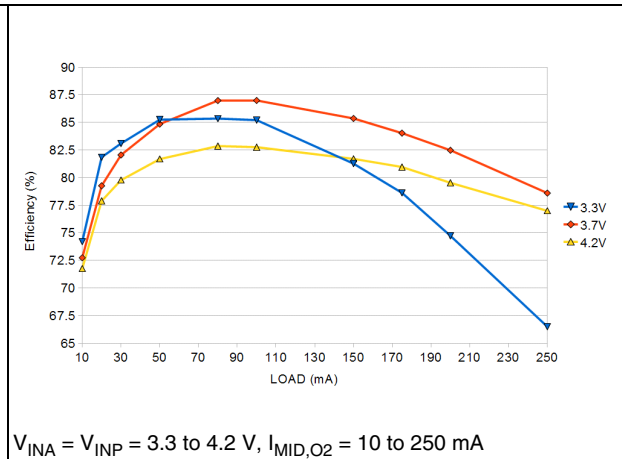


Figure 6. Efficiency vs. inductor

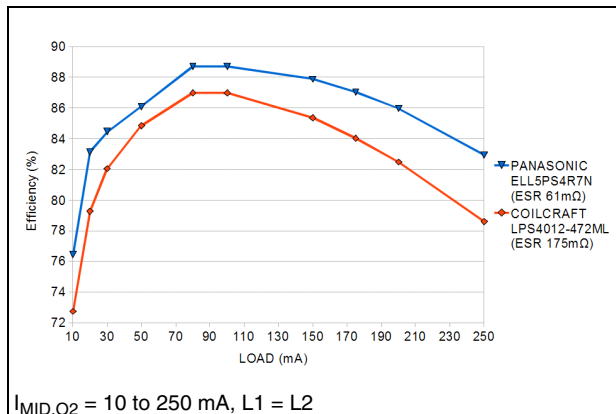


Figure 7. Soft-start and inrush current (no load)

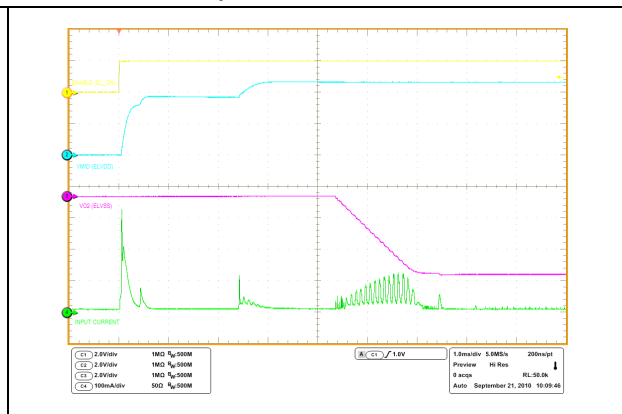


Figure 8. Fast discharge

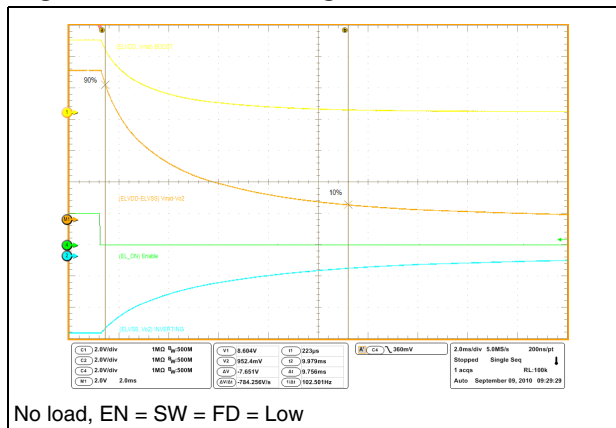


Figure 9. Switching and output waveforms

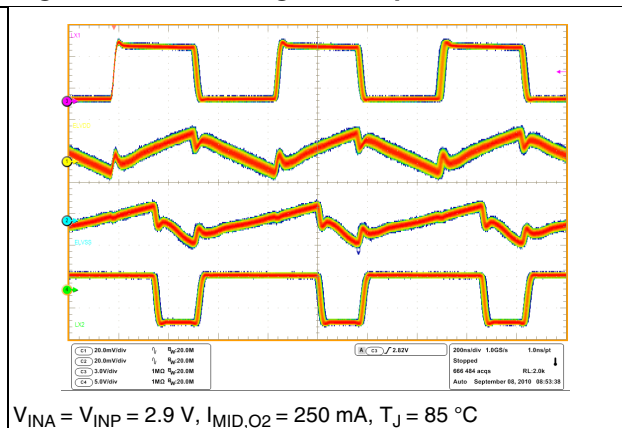
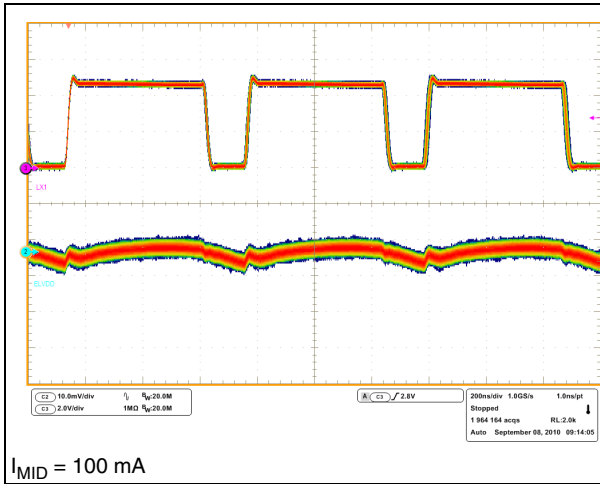
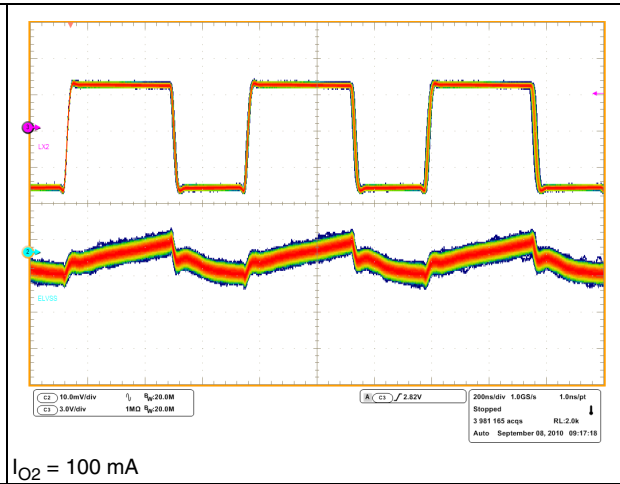


Figure 10. Step-up CCM operation



$I_{MID} = 100 \text{ mA}$

Figure 11. Inverting CCM operation



$I_{O2} = 100 \text{ mA}$

6 Detailed description

6.1 S_{WIRE}

- Protocol: to digitally communicate over a single cable with single-wire components
- Single-wire's 3 components:
 1. an external MCU
 2. wiring and associated connectors
 3. the STOD13A device with a dedicated single-wire pin.

6.1.1 S_{WIRE} features and benefits

- Fully digital signal
- No handshake needed
- Protection against glitches and spikes through an internal low pass filter acting on both rising and falling edges
- Uses a single wire (plus analog ground) to accomplish both communication and power control transmission
- Simplified design with an interface protocol that supplies control and signaling over a single-wire connection to set the output voltages.

6.1.2 S_{WIRE} protocol

- Single-wire protocol uses conventional CMOS/TTL logic levels (maximum 0.6 V for logic “zero” and a minimum 1.2 V for logic “one”) with operation specified over a supply voltage range of 2.5 V to 4.5 V
- Both master (MCU) and slave (STOD13A) are configured to permit bit sequential data to flow only in one direction at a time; master initiates and controls the device
- Data is bit-sequential with a START bit and a STOP bit
- Signal is transferred in real time
- System clock is not required; each single-wire pulse is self-clocked by the oscillator integrated in the master and is asserted valid within a frequency range of 250 kHz (maximum).

6.1.3 S_{WIRE} basic operations

- The negative output voltage levels are selectable within a wide range (steps of 100 mV)
- The device can be enabled / disabled via S_{WIRE} in combination with the Enable pin.

6.2 Negative output voltage levels

Table 7. Negative output voltage levels

| Pulse | V _{O2} | Pulse | V _{O2} | Pulse | V _{O2} | Pulse | V _{O2} |
|-------|-----------------|-------------------|-----------------|-------|-----------------|-------|-----------------|
| 1 | -6.4 | 11 | -5.4 | 21 | -4.4 | 31 | -3.4 |
| 2 | -6.3 | 12 | -5.3 | 22 | -4.3 | 32 | -3.3 |
| 3 | -6.2 | 13 | -5.2 | 23 | -4.2 | 33 | -3.2 |
| 4 | -6.1 | 14 | -5.1 | 24 | -4.1 | 34 | -3.1 |
| 5 | -6.0 | 15 | -5.0 | 25 | -4.0 | 35 | -3.0 |
| 6 | -5.9 | 16 ⁽¹⁾ | -4.9 | 26 | -3.9 | 36 | -2.9 |
| 7 | -5.8 | 17 | -4.8 | 27 | -3.8 | 37 | -2.8 |
| 8 | -5.7 | 18 | -4.7 | 28 | -3.7 | 38 | -2.7 |
| 9 | -5.6 | 19 | -4.6 | 29 | -3.6 | 39 | -2.6 |
| 10 | -5.5 | 20 | -4.5 | 30 | -3.5 | 40 | -2.5 |
| | | | | | | 41 | -2.4 |

1. Default value.

Table 8. Enable and S_{WIRE} operation table⁽¹⁾

| Enable | S _{WIRE} | Action |
|--------|-------------------|--|
| Low | Low | Device off |
| Low | High | Negative output set by S _{WIRE} |
| High | Low | Default negative output voltage |
| High | High | Default negative output voltage |

1. The Enable pin must be set to AGND while using the S_{WIRE} function.

Table 9. Fast Discharge operation table

| FD pin | Action |
|--------|---|
| Low | Fast discharge active after IC shutdown |
| High | No fast discharge function |

The FD function is only controlled by the FD pin. It is not related to the enable block.

7 Application information

7.1 External passive components

7.1.1 Inductor selection

Magnetic shielded low ESR power inductors must be chosen as the key passive components for switching converters.

For the step-up converter an inductance between 4.7 μH and 6.8 μH is recommended.

For the inverting stage the suggested inductance ranges from 3.3 μH to 4.7 μH .

It is very important to select the right inductor according to the maximum current the inductor can handle to avoid saturation. The step-up and the inverting peak current can be calculated as follows:

Equation 1

$$I_{\text{PEAK-BOOST}} = \frac{V_{\text{MID}} \times I_{\text{OUT}}}{\eta_1 \times V_{\text{IN}_{\text{MIN}}}} + \frac{V_{\text{IN}_{\text{MIN}}} \times (V_{\text{MID}} - V_{\text{IN}_{\text{MIN}}})}{2 \times V_{\text{MID}} \times f_s \times L_1}$$

Equation 2

$$I_{\text{PEAK-INVERTING}} = \frac{(V_{\text{IN}_{\text{MIN}}} - V_{\text{O2}_{\text{MIN}}}) \times I_{\text{OUT}}}{\eta_2 \times V_{\text{IN}_{\text{MIN}}}} + \frac{V_{\text{IN}_{\text{MIN}}} \times V_{\text{O2}_{\text{MIN}}}}{2 \times (V_{\text{O2}_{\text{MIN}}} - V_{\text{IN}_{\text{MIN}}}) \times f_s \times L_2}$$

where

V_{MID} : step-up output voltage, fixed at 4.6 V;

V_{O2} : inverting output voltage including sign (minimum value is the absolute maximum value);

I_{O} : output current for both DC-DC converters;

V_{IN} : input voltage for the STOD03A;

f_s : switching frequency. Use the minimum value of 1.35 MHz for the worst case;

η_1 : efficiency of step-up converter. Typical value is 0.70;

η_2 : efficiency of inverting converter. Typical value is 0.60.

The negative output voltage can be set via S_{WIRE} at - 6.4 V. Accordingly, the inductor peak current, at the maximum load condition, increases. A proper inductor, with a saturation current as a minimum of 1.5 A, is preferred.

7.1.2 Input and output capacitor selection

It is recommended to use X5R or X7R low ESR ceramic capacitors as input and output capacitors in order to filter any disturbance present in the input line and to obtain stable operation for the two switching converters. A minimum real capacitance value of 6 μF must be guaranteed for C_{MID} and C_{O2} in all conditions. Considering tolerance, temperature variation and DC polarization, a 10 μF 10 V $\pm 10\%$ capacitor as C_{MID} and 2 x 10 μF 10 V $\pm 10\%$ as C_{O2} , can be used to achieve the required 6 μF .

7.2 Recommended PCB layout

The STOD13A is high frequency power switching device and therefore requires a proper PCB layout in order to obtain the necessary stability and optimize line/load regulation and output voltage ripple.

Analog input (V_{INA}) and power input (V_{INP}) must be kept separated and connected together at the C_{IN} pad only. The input capacitor must be as close as possible to the IC.

In order to minimize the ground noise, a common ground node for power ground and a different one for analog ground must be used. In the recommended layout, the AGND node is placed close to C_{REF} ground while the PGND node is centered at C_{IN} ground. They are connected by a separated layer routing on the bottom through vias.

The exposed pad is connected to AGND through vias.

Figure 12. Top layer and silk-screen (top view, not to scale)

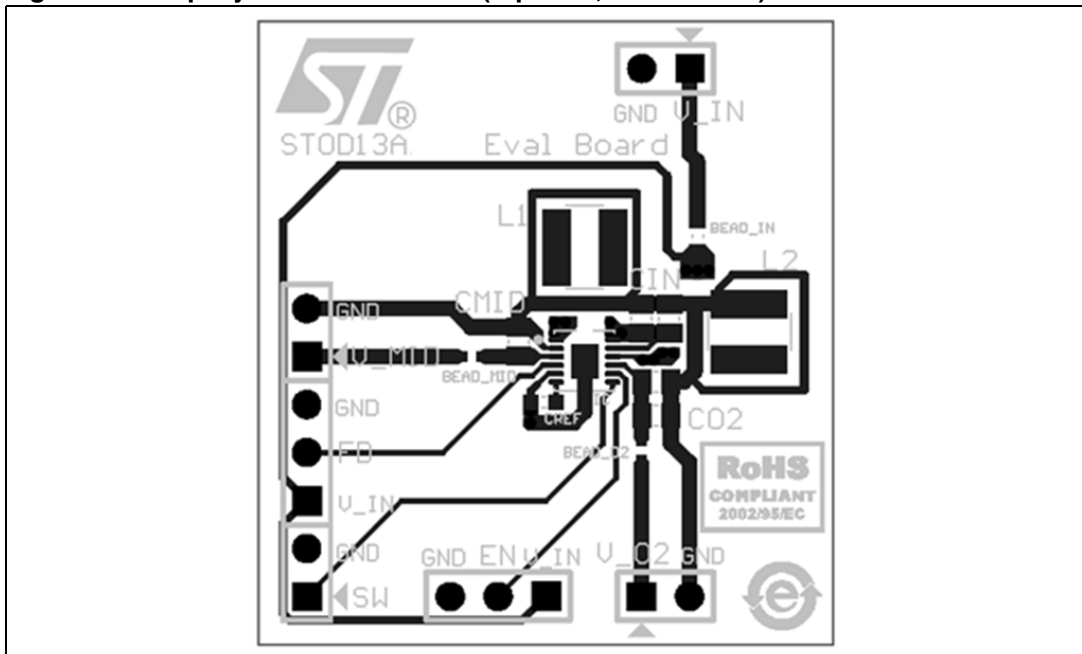
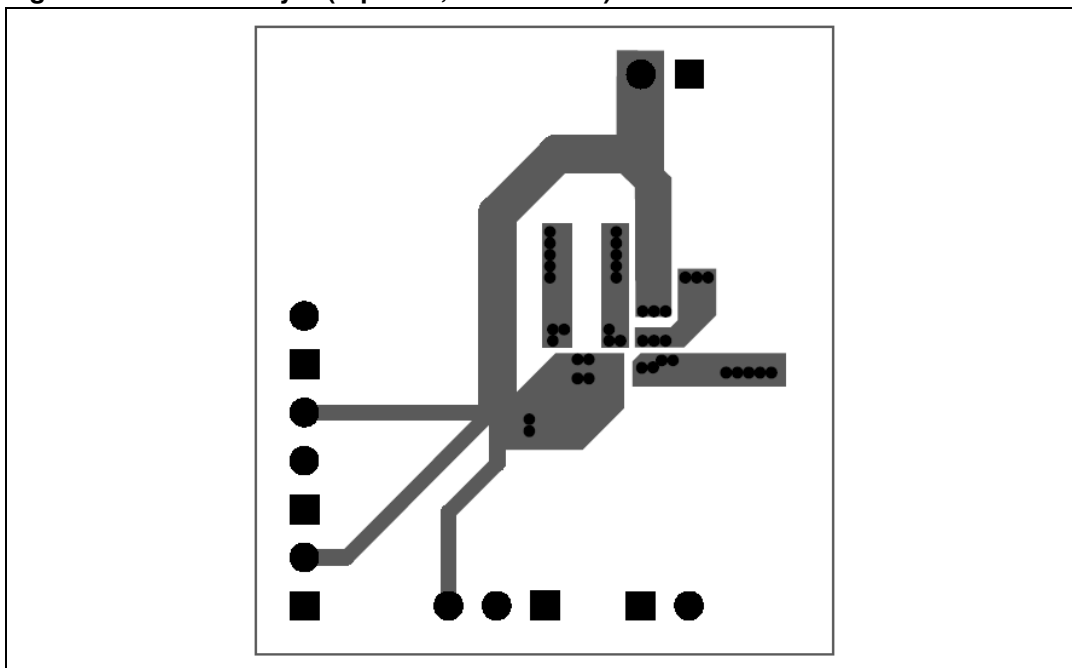


Figure 13. Bottom layer (top view, not to scale)



8 Detailed description

8.1 General description

The STOD13A is a high efficiency dual DC-DC converter which integrates a step-up and inverting power stage suitable for supplying AMOLED panels. Thanks to the high level of integration it needs only 6 external components to operate and it achieves very high efficiency using a synchronous rectification technique for each of the two DC-DC converters.

The controller uses an average current mode technique in order to obtain good stability and precise voltage regulation in all possible conditions of input voltage, output voltage, and output current. In addition, the peak inductor current is monitored in order to avoid saturation of the coils.

The STOD13A implements a power saving technique in order to maintain high efficiency at very light load and it switches to PWM operation as the load increases in order to guarantee the best dynamic performances and low noise operation.

The STOD13A avoids battery leakage thanks to the true-shutdown feature and it is self protected from overtemperature. Undervoltage lockout and soft-start guarantee proper operation during startup.

8.1.1 Multiple operation modes

Both the step-up and the inverting stage of the STOD13A operate in three different modes: pulse skipping (PSM), discontinuous conduction mode (DCM) and continuous conduction mode (CCM). It switches automatically between the three modes according to input voltage, output current, and output voltage conditions.

Pulse skipping operation:

The STOD13A works in pulse skipping mode when the load current is below a few mA.

The load current level at which this way of operation occurs depends on input voltage only for the step-up converter and on input voltage and negative output voltage (VO2) for the inverting converter.

Discontinuous conduction mode:

When the load increases above some tens of mA, the STOD13A enters DCM operation.

In order to obtain this type of operation the controller must avoid the inductor current going negative. The discontinuous mode detector (DMD) blocks sense the voltage across the synchronous rectifiers (P1B for the step-up and N2 for the inverting) and turn off the switches when the voltage crosses a defined threshold which, in turn, represents a certain current in the inductor. This current can vary according to the slope of the inductor current which depends on input voltage, inductance value, and output voltage.

Continuous conduction mode:

At medium/high output loads, the STOD13A enters in full CCM at constant switching frequency mode for each of the two DC-DC converters.

8.1.2 Enable pin

The device operates when the EN pin is set high. If the EN pin is set low, the device stops switching, and all the internal blocks are turned off. In this condition the current drawn from V_{INP}/V_{INA} is below 1 μ A in the whole temperature range. In addition, the internal switches are in an OFF state so the load is electrically disconnected from the input, this avoids unwanted current leakage from the input to the load.

8.1.3 Soft-start and inrush current limiting

After the EN pin is pulled high, or after a suitable voltage is applied to V_{INP} V_{INA} and EN the device initiates the startup phase. As a first step, the C_{MID} capacitor is charged, the P1B switch implements a current limiting technique in order to keep the charge current below 400 mA. This avoids the battery overloading during startup. After V_{MID} reaches the V_{INP} voltage level, the P1B switch is fully turned on and the soft-start procedure for the step-up is started.

After around 2 ms the soft-start for the inverting is started. The positive and negative voltages are under regulation at around 6ms after the EN pin is asserted high.

8.1.4 Undervoltage lockout

The undervoltage lockout function avoids improper operation of the STOD13A when the input voltage is not high enough. When the input voltage is below the UVLO threshold the device is in shutdown mode. The hysteresis of 50 mV avoids unstable operation when the input voltage is close to the UVLO threshold.

8.1.5 Overtemperature protection

An internal temperature sensor continuously monitors the IC junction temperature. If the IC temperature exceeds 140 °C, typical, the device stops operating. As soon as the temperature falls below 125 °C, typical, normal operation is restored.

8.1.6 Short-circuit protection

When short-circuit occurs, the device is able to detect the voltage difference between V_{IN} and V_{OUT} . Overshoots are limited, decreasing the inductor current. After that, the output stages of the device are turned off. This status is maintained, avoiding current flowing to the load. A new ENABLE transition is needed to restart the device. During startup the short-circuit protection is active.

8.1.7 Fast discharge

When ENABLE turns from high to low level and the FD pin is low, the device goes into shutdown mode and LX1 and LX2 stop switching. Then, the discharge switch between V_{MID} and V_{IN} and the switch between V_{O2} and GND turn on and discharge the positive output voltage and negative output voltage. When the output voltages are discharged to 0 V, the switches turn off and the outputs are high impedance. When the FD pin is high, the fast discharge after shutdown is off.

9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST registered trademark.

DFN12L (3 x 3 x 0.6 mm) mechanical data

| Dim. | mm. | | | inch. | | |
|------|------|------|------|-------|-------|-------|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 0.51 | 0.55 | 0.60 | 0.020 | 0.022 | 0.024 |
| A1 | 0 | 0.02 | 0.05 | 0 | 0.001 | 0.002 |
| A3 | | 0.20 | | | 0.008 | |
| b | 0.18 | 0.25 | 0.30 | 0.007 | 0.010 | 0.012 |
| D | 2.85 | 3 | 3.15 | 0.112 | 0.118 | 0.124 |
| D2 | 1.87 | 2.02 | 2.12 | 0.074 | 0.080 | 0.083 |
| E | 2.85 | 3 | 3.15 | 0.112 | 0.118 | 0.124 |
| E2 | 1.06 | 1.21 | 1.31 | 0.042 | 0.048 | 0.052 |
| e | | 0.45 | | | 0.018 | |
| L | 0.30 | 0.40 | 0.50 | 0.012 | 0.016 | 0.020 |

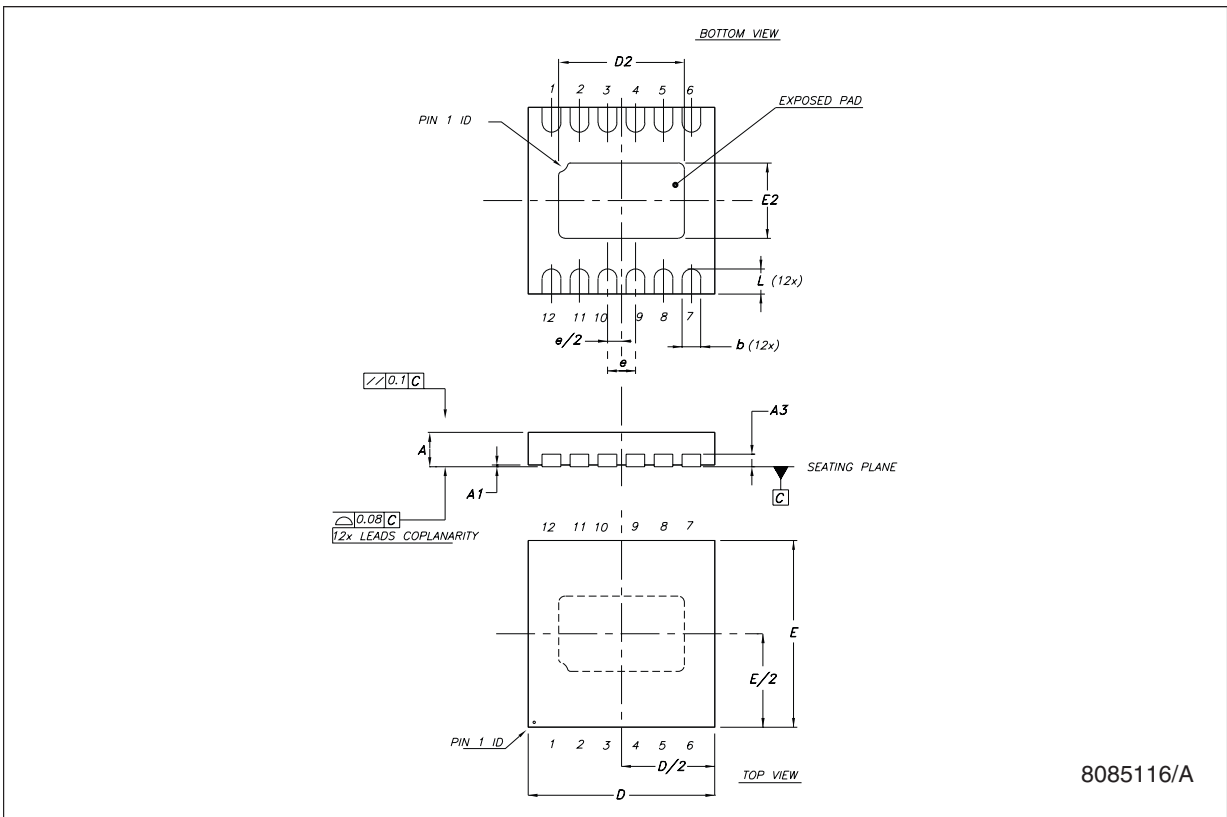
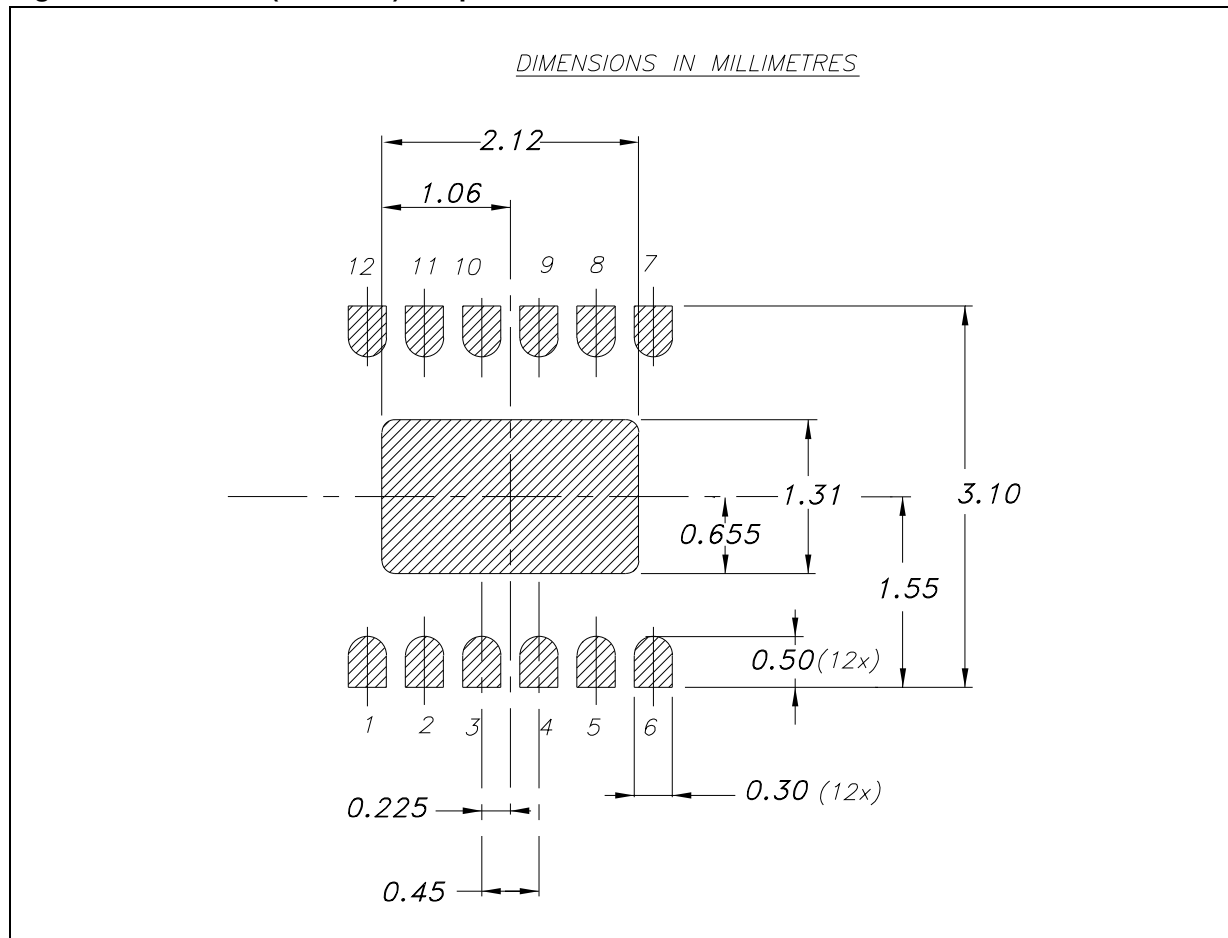


Figure 14. DFN12L (3 x 3 mm) footprint recommended data



10 Revision history

Table 10. Document revision history

| Date | Revision | Changes |
|-------------|----------|------------------|
| 14-Dec-2011 | 1 | Initial release. |

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