STOD1812

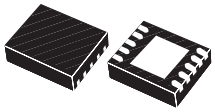
Power supply for PMOLED display panel

Features

- Synchronous step-up converter
- Input voltage range from 2.5 V to 5.5 V
- Maximum output current 120 mA
- Efficiency: 75 % at I_O = 10 mA - 30 mA; 85 % at I_O = 30 mA - 120 mA
- Switching at 1.2 MHz in typical application conditions
- Enable pin for shutdown mode
- True load disconnect
- Soft-start to limit inrush current
- UVLO protection
- Adjustable output voltage up to 20 V
- Low quiescent current: < 1 µA in shutdown mode
- Over-temperature protection
- Package: DFN10L 3x3 mm, 0.8 mm
- Operating junction temperature range: -40 °C to 125 °C

Applications

- Passive matrix OLED power supplies
- Mobile phones
- PDAs
- Camcorders
- Digital still cameras



DFN10L (3x3 mm)

Description

STOD1812 is a step-up converter designed to power passive matrix OLED (PMOLED) displays, providing the pre-charge and biasing voltage of the column matrix driver. STOD1812 uses a pulsed frequency modulation (PFM) control mode technique. The high switching frequency makes it possible to reduce the value and size of the external components. This device is particularly suitable for battery-operated applications, where overall system efficiency is the major concern.

Synchronous rectification has been integrated in the device in order to eliminate the external Schottky diode. An internal compensation net is also integrated, enabling the STOD1812 to provide excellent load transient performance in addition to good load regulation.

The output voltage is set using two external resistors. Over-temperature protection and under-voltage lockout (UVLO) functions are integrated in the device. An additional switch implements a true load disconnection feature which stops the currrent flowing from the input when the device is in shutdown mode. The EN pin turns off the device, reducing the quiescent current to 0.1 µA.

Table 1. Device summary

Order code	Package	Packaging
STOD1812PUR	DFN10L (3x3 mm)	3000 parts per reel

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1 Diagram

Figure 1. Internal block diagram

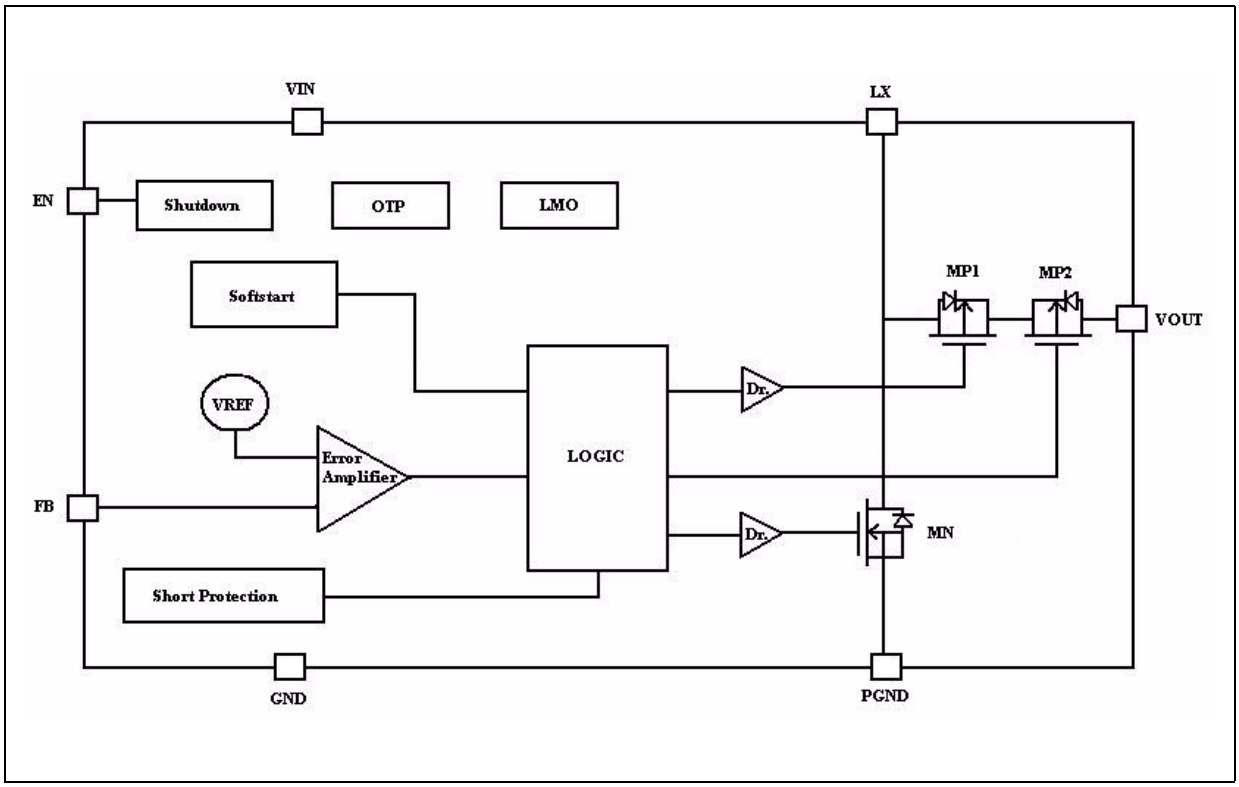
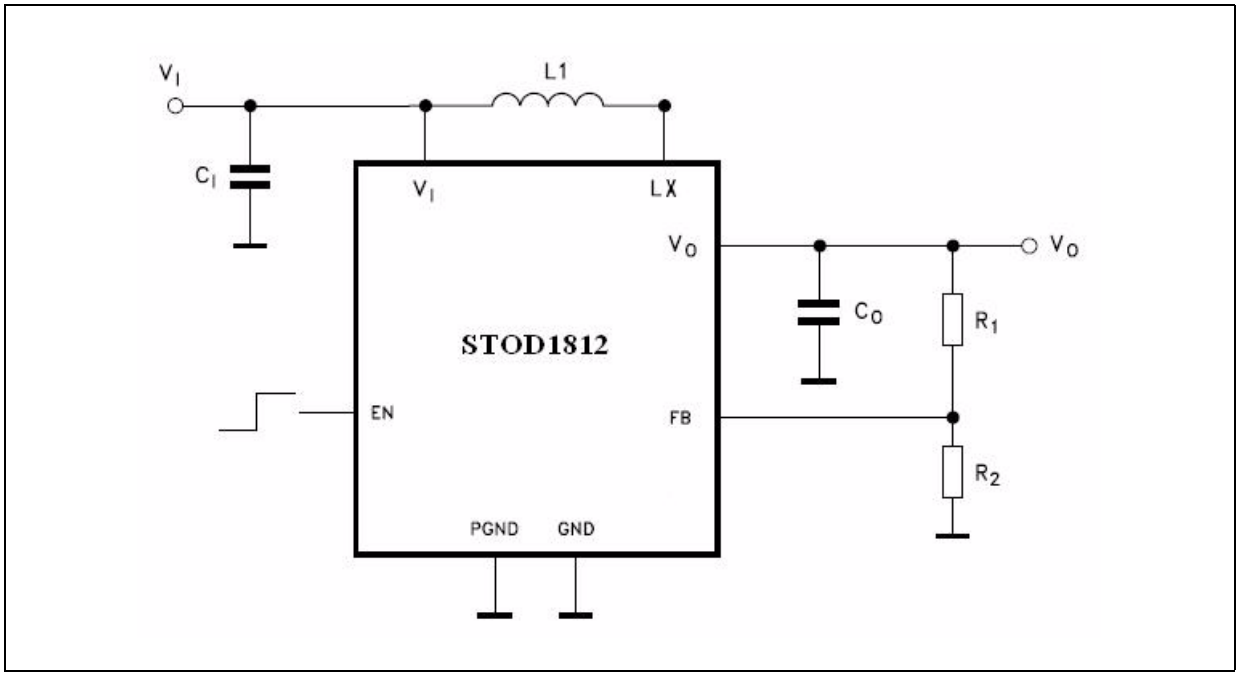


Figure 2. Schematic diagram



2 Pin configuration

Figure 3. Pin connections (top view)

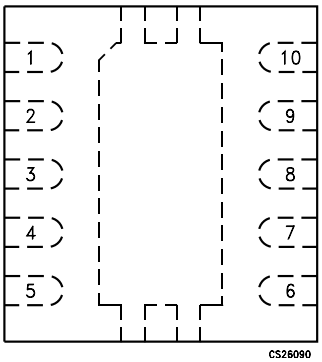


Table 2. Pin description

Pin n°	Symbol	Description
1	OUT	Output voltage
2	OUT	Output voltage
3	GND	Ground
4	FB	Feedback
5	EN	DC supply voltage enable control pin. ON =V_I. When pulled low put the device in shutdown mode.
6	V_I	Input supply voltage.
7	L_X	Switching node
8	L_X	Switching node
9	PGND	Power ground
10	PGND	Power ground
	Exp Pad	Exposed Pad. It must be connected to power ground

3 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_I	DC supply voltage	-0.3 to 6	V
EN	Enable pin	-0.3 to 6	V
FB	Feedback pin	-0.3 to 6	V
L_X	Switching node	-0.3 to 20	V
I_{LX}	Switching current	Internally limited	A
V_{OUT}	Converter output voltage	-0.3 to 20	V
P_D	Power dissipation	Internally limited	mW
T_{STG}	Storage temperature range	-65 to 150	°C
T_J	Operating temperature range	-40 to 125	°C

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient (tested on 2 layers board)	30.9	°C/W

Table 5. ESD data

Symbol	Parameter	Value	Unit
ESD	Human Body Model	2	kV

4 Electrical characteristics

Table 6. Electrical characteristics
(T_J = -40 °C to 125 °C, V_I = 3.6 V, $C_I = C_O$ = 4.7 µF, L = 2.2 µH, I_O = 80 mA, $V_{EN} = V_I$, V_O = 18 V, R_1=270 kΩ, R_2 = 20 kΩ unless otherwise specified).

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply section						
V_I	Supply input voltage	I_O=0 to 120mA	2.5		5.5	V
I_O	Load current	V_I=2.5V to 5.5V	120			mA
UVLO_H	Under voltage lockout HIGH			2.3	2.4	V
UVLO_L	Under voltage lockout LOW		2.1	2.2		V
I_Q	Quiescent current	I_O=120mA		1.3		mA
		No Load, Switching		0.3		mA
		$V_{FB}=V_I$ - No Load, No Switching		35	50	µA
		V_{EN} =GND		100	300	nA
V_{EN} H	Enable high threshold	V_I=2.5V to 5.5V	1.2			V
V_{EN} L	Enable low threshold	V_I=2.5V to 5.5V			0.4	V
I_{EN}	Enable input current	V_{EN}=Vi			500	nA
Dynamic performance						
$T_{ON\ MAX}$	T_{ON} max time			0.5		µs
T_{SS}	Soft-start time	From enable to output regulation		0.6		ms
D_{MAX}	Maximum duty cycle			95		%
ν	Efficiency	I_O=5 to 30mA		75		%
		I_O=30 to 120mA		85		%
Step-up converter section						
V_{FB1}	Feedback voltage	V_I=2.5V to 5.5V	1.18	1.21	1.24	V
I_{FB}	Feedback leakage current	V_I=2.5V to 5.5V		30	100	nA
V_{O_MAX}	Output voltage range	V_I=2.5V to 5.5V; I_O=0 to 120mA	18			V
ΔV_{O_SLI}	Static line regulation	V_I=2.5V to 5.5V, I_{O1}=120mA,		0.6		%/V
ΔV_{O_SLO}	Static load regulation	I_O=0 to 120mA, V_I=3.6V;		0.0016		%/mA
ΔV_{O_LIT}	Line transient regulation	V_I=2.5V to 3.0V, I_{O1}=120mA, $T_R=T_F$=50µs T_A=25°C		80		mV
ΔV_{O_LOT}	Load transient regulation	I_O=5 to 120mA and I_O=120 to 5mA, $T_R=T_F$=10µs T_A=25°C, peak to peak		250		mV

Table 6. Electrical characteristics (continued)
(T_J = -40 °C to 125 °C, V_I = 3.6 V, C_I = C_O = 4.7 µF, L = 2.2 µH, I_O = 80 mA, V_{EN} = V_I, V_O = 18 V, R_1=270 kΩ, R_2 = 20 kΩ unless otherwise specified).

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
SVR	Supply voltage rejection	I_O=5 to 120mA at 200Hz-Pulse 0.5V_{PP} TDMA noise standard, T_A=25°C see *Figure 14*		40		mV
I_{PK}	Inductor peak current	T_A=25°C		2.4		A
$R_{DSON}P$	Resistance on P-channel			0.60	0.80	Ω
$R_{DSON}N$	Resistance on N-channel			0.25	0.65	Ω
Thermal shutdown						
OTP	Over temperature protection			150		°C
OTP_{HYST}	Over temperature protection hysteresis			20		°C

5 Functional description

5.1 Boost controller

STOD1812 is a boost converter operating in PFM (pulsed frequency modulation) mode. The converter monitors the output voltage through the bridge resistor divider R_1 and R_2, and when the feedback voltage falls below the feedback voltage, the boost switch t_{SW} turns on and the inductor current ramps up. The inductor current is measured by detecting the temperature compensated drain voltage of the boost MOSFET. The boost turns off when its drain voltage reaches the internal reference, the main switch remains off until the minimum off time has passed and the feedback voltage is below the reference again. A maximum ON time prevents the switch t_{SW} from staying ON for an excessively long period.

In order to calculate the values of the bridge resistors with a fixed V_O, the following formula can be used:

$$\frac{V_O}{1{,}21} - 1 = \frac{R_1}{R_2}$$

5.2 Enable

The ENABLE pin is a logic input signal that turns on the controller when the voltage on this pin is equal to or higher than 1.2 V. When the voltage is at or below 0.4 V the STOD1812 goes into shutdown mode. In this case, the true-shutdown switch is turned off and the overall power consumption is reduced to 0.1 µA. No pull-up or pull-down is present on this pin.

5.3 Efficiency

The total consumption of some PMOLED displays can be as low as 1 mA. In order to increase the battery life of the device, the STOD1812 offers high efficiency over a wide range of output load current and input voltages. See typical application efficiency performance in *Section 8 on page 11*.

5.4 Under voltage lockout (UVLO)

The minimum supply voltage is 2.5 V, under which the undervoltage lockout circuit operates with a typical threshold of 2.3 V.

6 Typical application information

Figure 4. Typical application circuit connections

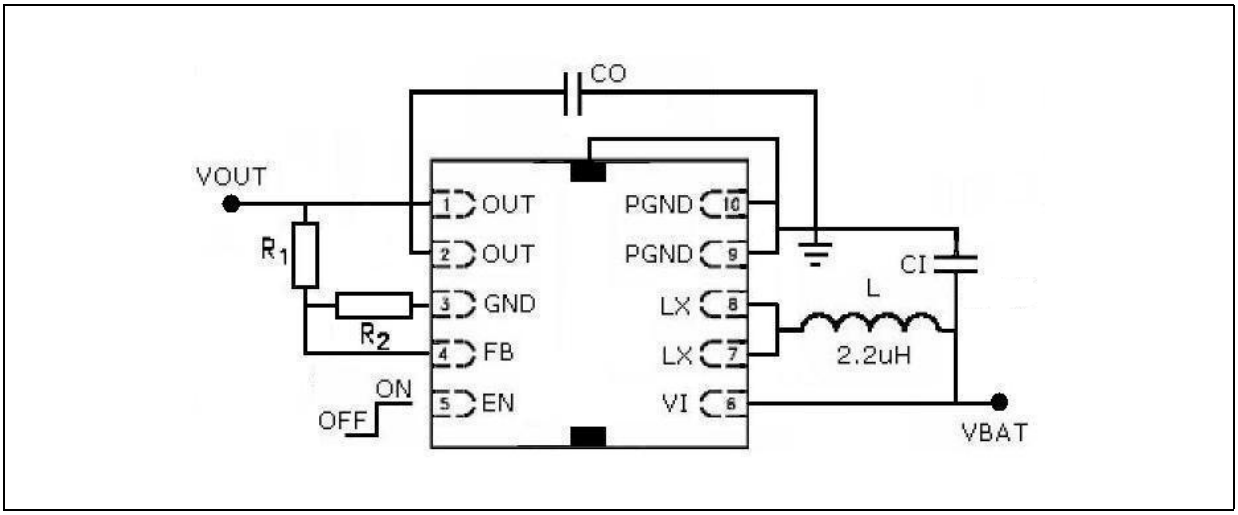


Table 7. External components

Symbol	Parameter	Min.	Typ.	Max.	Unit
L	Inductor (I_{SAT} = 2.5 A)		2.2		µH
C_I	Ceramic capacitor SMD		4.7		µF
C_O	Ceramic capacitor SMD		4.7		µF
R1	Feedback resistor (for V_O = 18 V)		270		kΩ
R2	Feedback resistor (for V_O = 18 V)		20		kΩ

Note: The external components suggested in this document should be considered as a design reference guide. The performance data mentioned in the electrical characteristics table are not guaranteed for all the possible electrical parameters of the components included in this list. However, the operation of STOD1812 is not limited to the use of components included in this list.

7 Demonstration board

Figure 5. Demonstration board photo

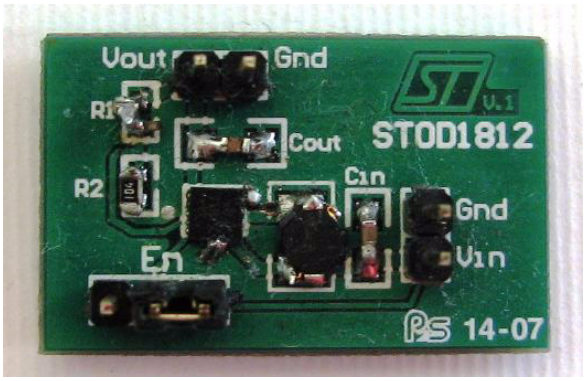


Figure 6. Suggested demonstration board schematic (top layer view)

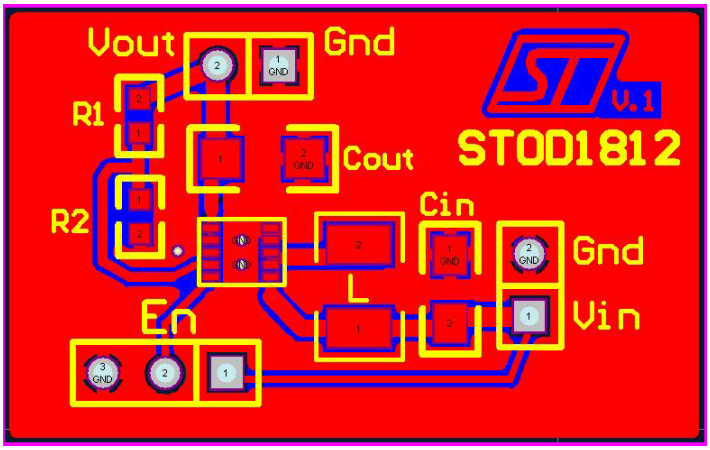
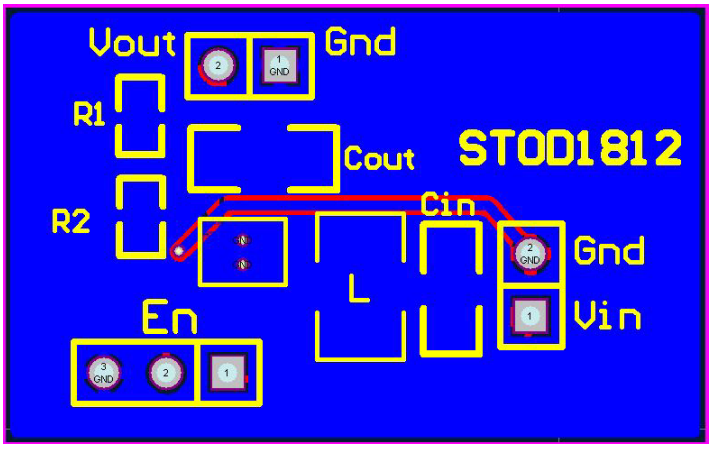


Figure 7. Suggested demonstration board schematic (bottom layer view)



8 Typical application performance

(V_O = 18 V, L = 2.2 µH, C_I = C_O = 4.7 µF, R_1 = 270 kΩ, R_2 = 20 kΩ)

Figure 8. Efficiency vs output current

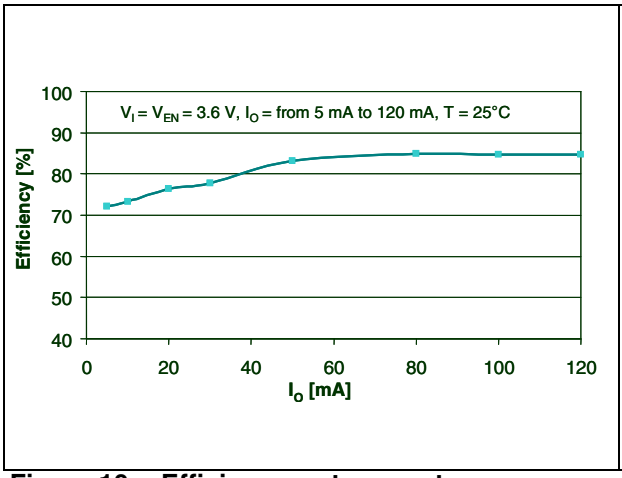


Figure 9. Efficiency vs input voltage

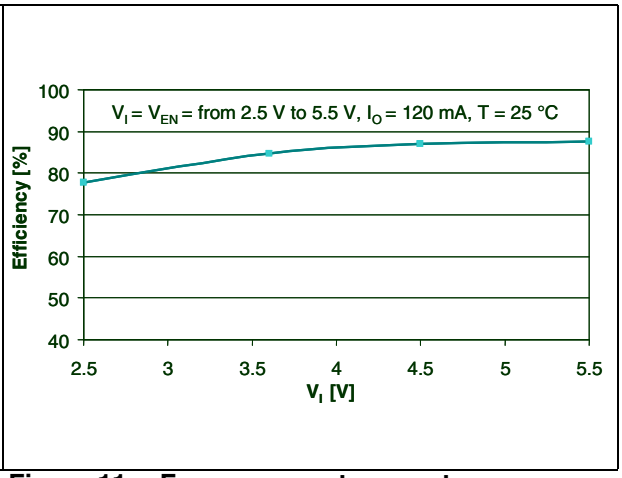


Figure 10. Efficiency vs temperature

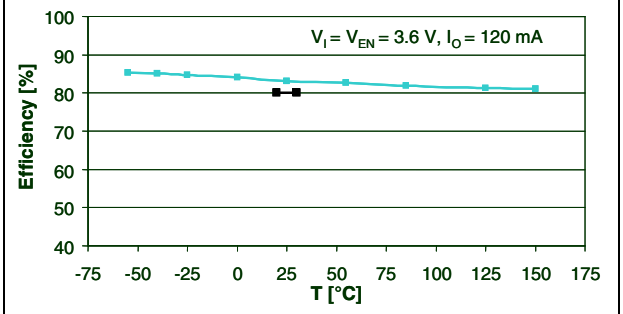


Figure 11. Frequency vs temperature

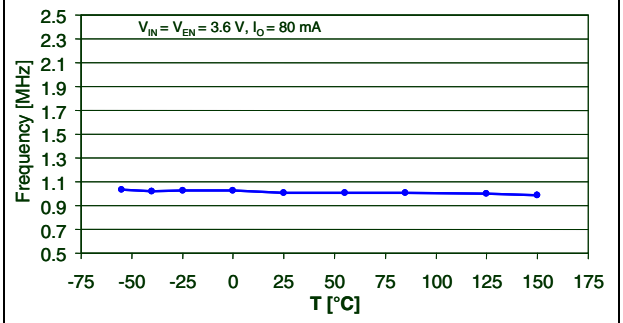
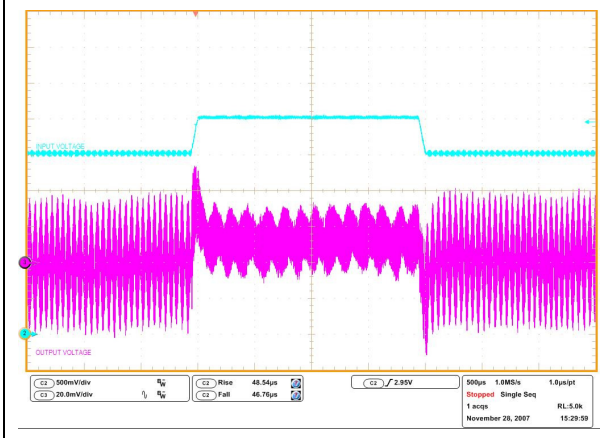
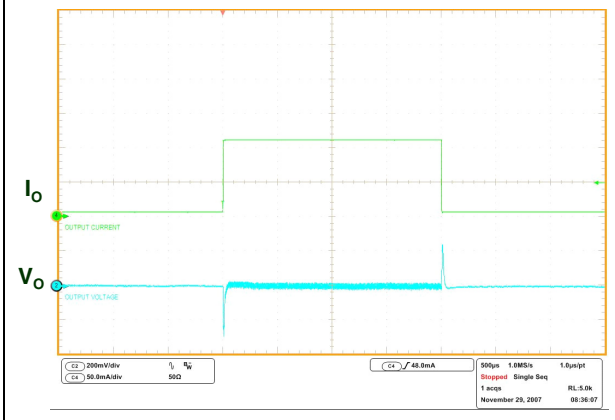


Figure 12. Line transient



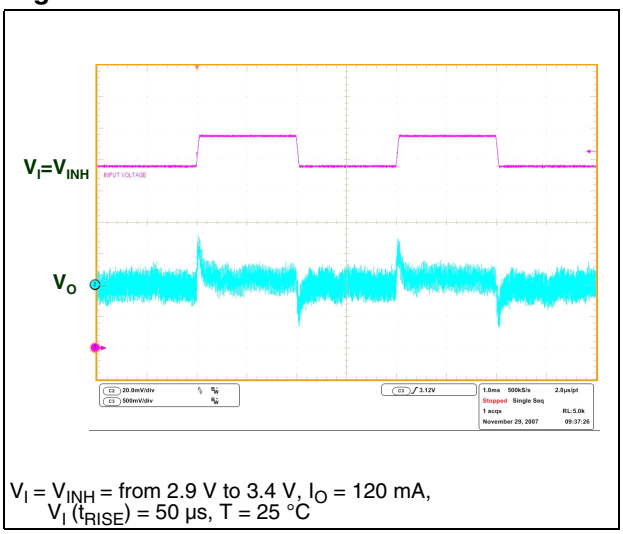
V_I = from 2.5 V to 3 V, I_O = 120 mA, V_I (t_{RISE} = t_{FALL}) = 50µs, T = 25 °C

Figure 13. Load transient response



V_I = 3.6 V, I_O from 5mA to 120mA, t_{RISE} = t_{FALL} = 10 µs, T = 25 °C

Figure 14. TDMA noise



$V_I = V_{INH}$ = from 2.9 V to 3.4 V, I_O = 120 mA,
V_I (t_{RISE}) = 50 µs, T = 25 °C

9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 15. DFN10L package outline

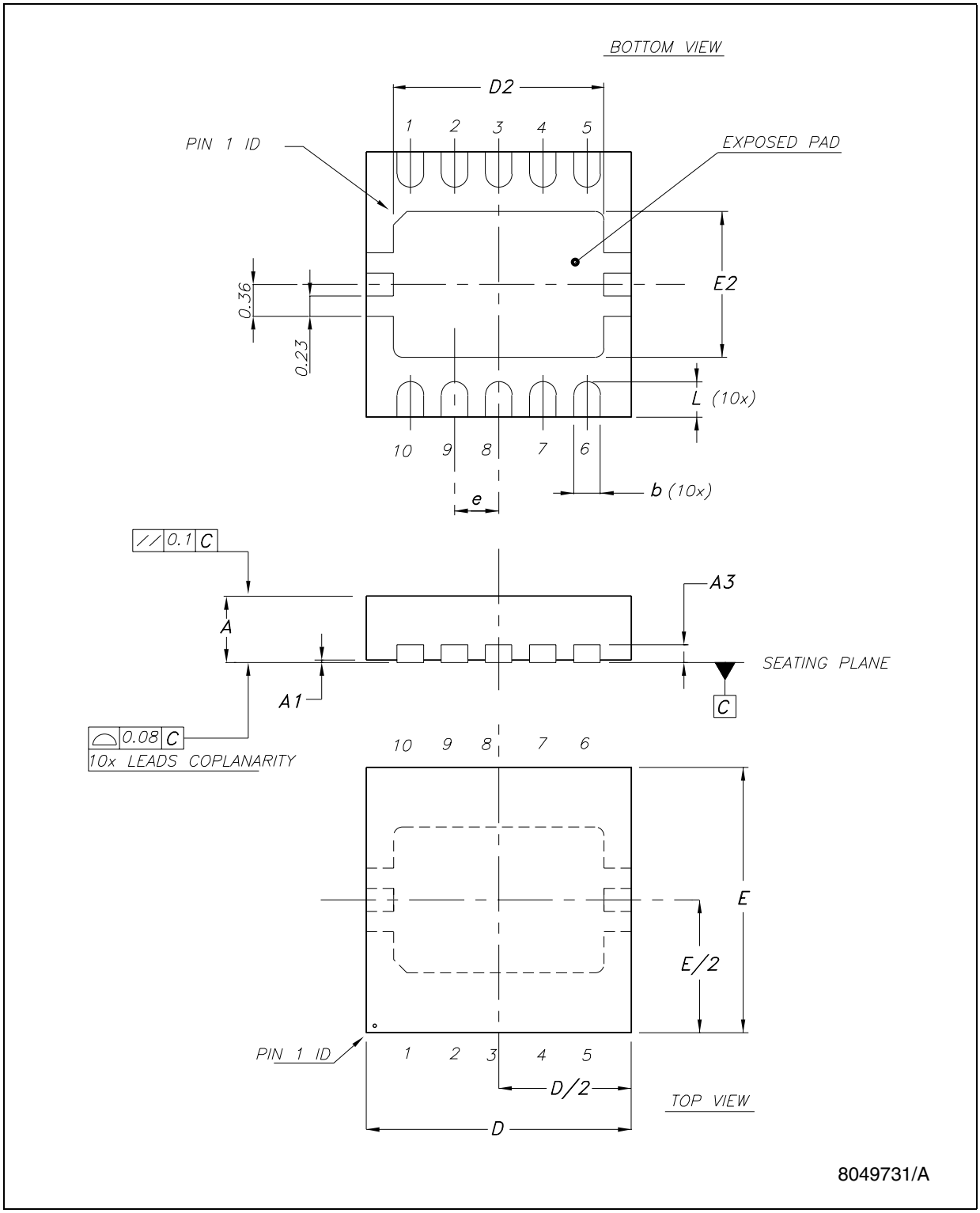
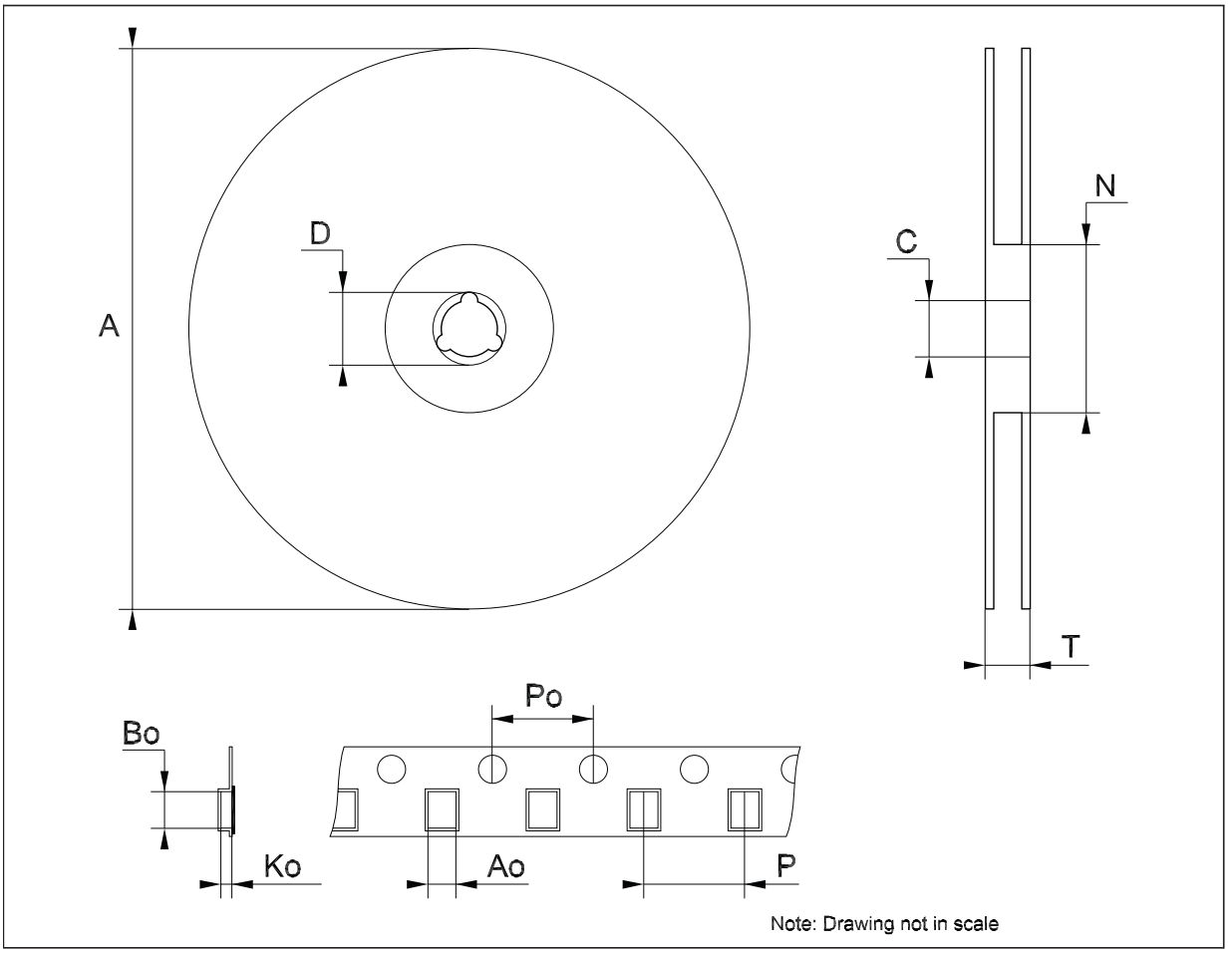


Table 8. DFN10L mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0	0.02	0.05	0	0.001	0.002
A3		0.20			0.008	
b	0.18	0.25	0.30	0.007	0.010	0.012
D	2.90	3	3.10	0.114	0.118	0.122
D2	2.23	2.38	2.48	0.088	0.094	0.098
E	2.90	3	3.10	0.114	0.118	0.122
E2	1.49	1.64	1.74	0.059	0.065	0.069
e		0.50			0.020	
L	0.30	0.40	0.50	0.012	0.016	0.020

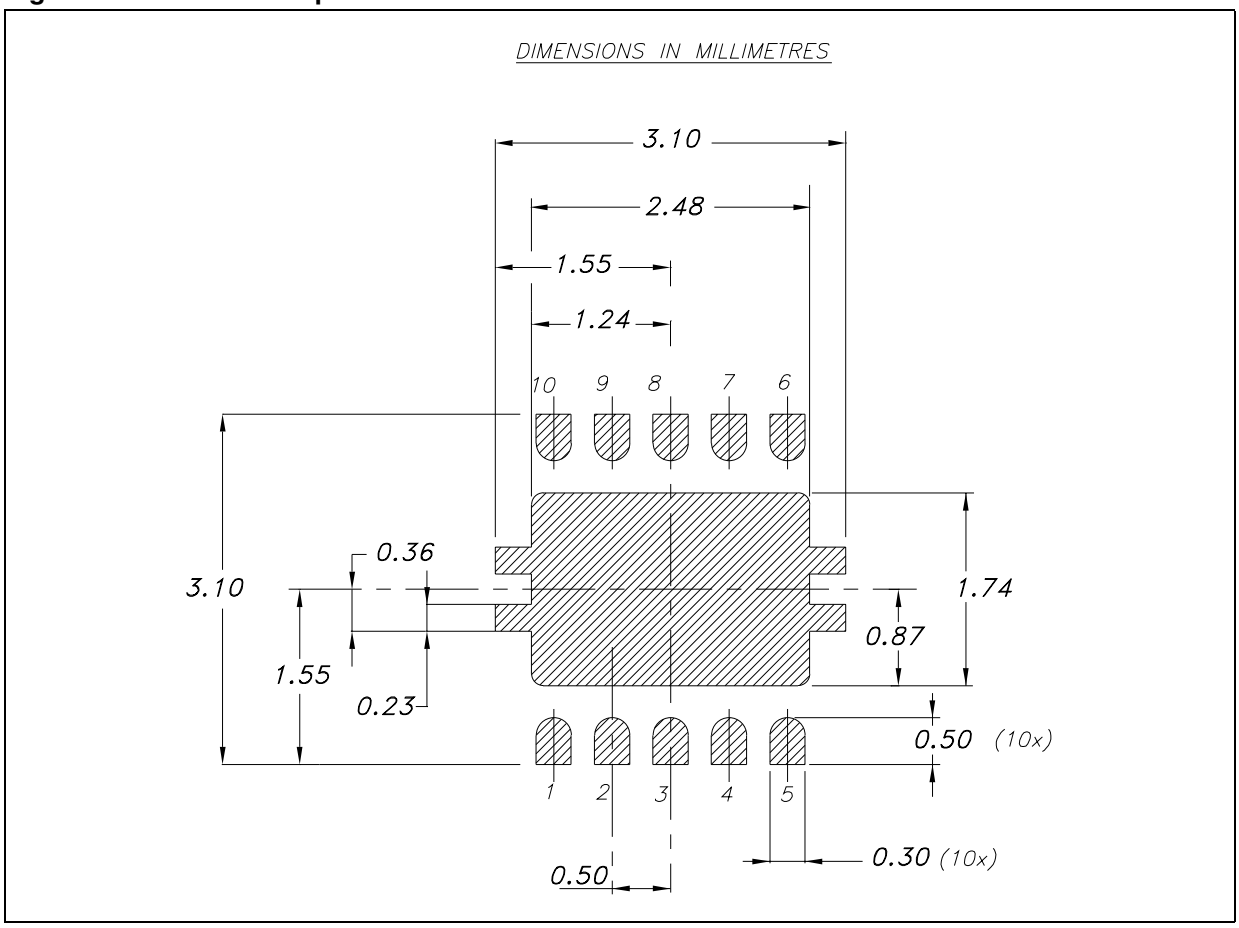
Tape & reel QFNxx/DFNxx (3x3) mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			180			7.087
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			14.4			0.567
Ao		3.3			0.130	
Bo		3.3			0.130	
Ko		1.1			0.043	
Po		4			0.157	
P		8			0.315	



Note: Drawing not in scale

Figure 16. DFN10L footprint - recommended data



10 Revision history

Table 9. Document revision history

Date	Revision	Changes
25-Mar-2008	1	Initial release.

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