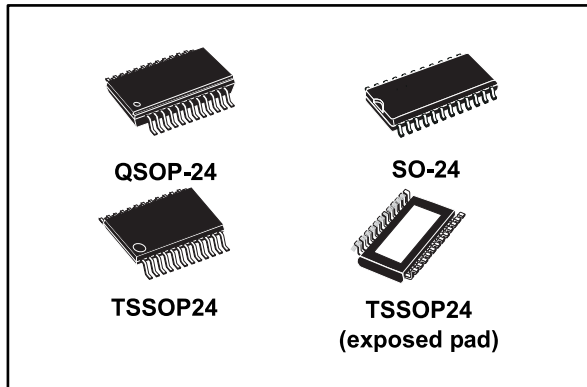


## Low voltage 16-bit constant current LED sink driver with balanced output rise/fall time

Datasheet - production data



### Description

The STP16CPC05 is a monolithic, low voltage, low current power 16-bit shift register designed for LED panel displays. The STP16CPC05 contains a 16-bit serial-in, parallel-out shift register that feeds a 16-bit, D-type storage register. In the output stage, sixteen regulated current sources provide from 5 mA to 100 mA constant current to drive the LEDs. The STP16CPC05's output stage is designed to optimize the turn-on and turn-off time, typically 100 nS. The balanced turning ON/OFF improves the system performances reducing the parasitic capacitance in applications where parasitic inductance generate ringing or noise in the system. The LEDs' brightness can be controlled by using an external resistor to adjust the STP16CPC05 output current. The STP16CPC05 guarantees a 20 V output driving capability, allowing users to connect more LEDs in series. The high clock frequency, 30 MHz, makes the device suitable for high data rate transmission. The 3.3 V voltage supply is useful in applications that interface with a 3.3 V microcontroller.

### Features

- Low voltage power supply down to 3 V
- 16 constant current output channels
- Adjustable output current through external resistor
- Serial data IN/parallel data OUT
- Can be driven by a 3.3 V microcontroller
- Output current: 5-100 mA
- Max clock frequency 30 MHz
- ESD protection 2.5 kV HBM, 200 V MM

Table 1: Device summary

Order code	Package	Packing
STP16CPC05MTR	SO-24	1000 parts per reel
STP16CPC05TTR	TSSOP24	2500 parts per reel
STP16CPC05XTTR	TSSOP24 exposed pad	2500 parts per reel
STP16CPC05PTR	QSOP-24	2500 parts per reel

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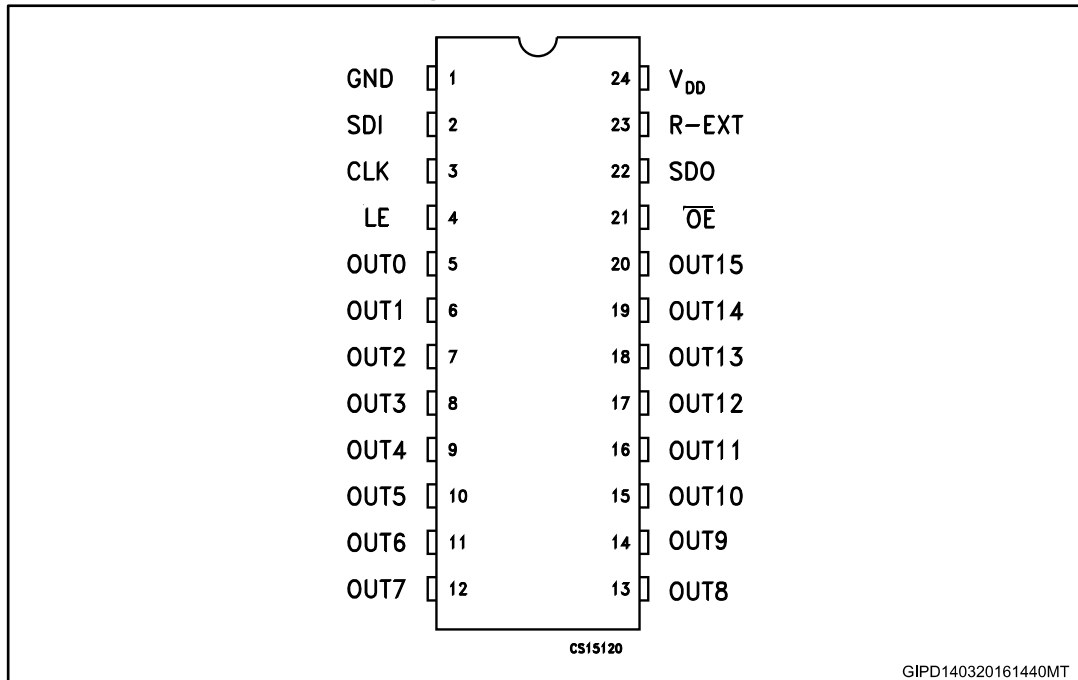
# 1 Summary description

Table 2: Typical current accuracy

Output voltage	Current accuracy		Output current	V <sub>DD</sub>	Temperature
	Between bits	Between ICs			
≥ 1.3 V	± 1.5 %	± 5 %	≥20 to 100 mA	3.3 V to 5 V	25 °C

## 1.1 Pin connection and description

Figure 1: Pin connection



The exposed pad should be electrically connected to a metal land electrically isolated or connected to ground.

Table 3: Pin description

Pin n°	Symbol	Name and function
1	GND	Ground terminal
2	SDI	Serial data input terminal
3	CLK	Clock input terminal
4	LE	Latch input terminal
5-20	OUT 0-15	Output terminal
21	$\overline{OE}$	Input terminal of output enable (active low)
22	SDO	Serial data out terminal
23	R-EXT	Input terminal for an external resistor for constant current programming
24	V <sub>DD</sub>	Supply voltage terminal

## 2 Electrical ratings

### 2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	Supply voltage	0 to 7	V
V <sub>O</sub>	Output voltage	-0.5 to 20	V
I <sub>O</sub>	Output current	100	mA
V <sub>I</sub>	Input voltage	-0.4 to V <sub>DD</sub> +0.4	V
I <sub>GND</sub>	GND terminal current	1600	mA
f <sub>CLK</sub>	Clock frequency	50	MHz

### 2.2 Thermal data

Table 5: Thermal data

Symbol	Parameter	Value	Unit	
T <sub>OPR</sub>	Operating temperature range	-40 to +125	°C	
T <sub>STG</sub>	Storage temperature range	-55 to +150	°C	
R <sub>thja</sub>	Thermal resistance junction-ambient	SO-24	60	°C/W
		TSSOP24	85	°C/W
		TSSOP24 <sup>(1)</sup> exposed pad	37.5	°C/W
		QSOP-24	72	°C/W

**Notes:**

<sup>(1)</sup> The exposed pad should be soldered directly to the PCB to realize the thermal benefits.

## 2.3 Recommended operating conditions

Table 6: Recommended operating conditions  $T_A = 25\text{ }^\circ\text{C}$

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{DD}$	Supply voltage		3.0	-	5.5	V
$V_O$	Output voltage			-	20	V
$I_o$	Output current	OUTn	3	-	100	mA
$I_{OH}$	Output current	SERIAL-OUT		-	+1	mA
$I_{OL}$	Output current	SERIAL-OUT		-	-1	mA
$V_{IH}$	Input voltage		$0.7 V_{DD}$	-	$V_{DD}+0.3$	V
$V_{IL}$	Input voltage		-0.3	-	$0.3 V_{DD}$	V
$t_{wLAT}$	LE pulse width	$V_{DD} = 3.0\text{ V to } 5.0\text{ V}$	20	-		ns
$t_{wCLK}$	CLK pulse width		16	-		ns
$t_{wEN}$	$\overline{OE}$ pulse width		200	-		ns
$t_{SETUP(D)}$	Setup time for DATA		8	-		ns
$t_{HOLD(D)}$	Hold time for DATA		4	-		ns
$t_{SETUP(L)}$	Setup time for LATCH		5	-		ns
$f_{CLK}$	Clock frequency		Cascade operation <sup>(1)</sup> $V_{DD} = 5\text{ V}$		-	30

**Notes:**

<sup>(1)</sup> If the device is connected in cascade, it may not be possible to achieve the maximum data transfer. Please consider the timings carefully.

### 3 Electrical characteristics

$V_{DD} = 3.3\text{ V to }5\text{ V}$ ,  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified.

Table 7: Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{IH}$	Input voltage high level		$0.7 V_{DD}$		$V_{DD}$	V
$V_{IL}$	Input voltage low level		GND		$0.3 V_{DD}$	V
$I_{OH}$	Output leakage current	$V_{OH} = 20\text{ V}$			10	$\mu\text{A}$
$V_{OL}$	Output voltage (serial-OUT)	$I_{OL} = 1\text{ mA}$			0.4	V
$V_{OH}$	Output voltage (serial-OUT)	$I_{OH} = -1\text{ mA}$	$V_{DD}-0.4\text{ V}$			V
$I_{OL1}$	Output current	$V_O = 0.3\text{ V}$ , $R_{ext} = 4.2\text{ k}\Omega$	4.25	5	5.75	mA
$I_{OL2}$		$V_O = 0.3\text{ V}$ , $R_{ext} = 1\text{ k}\Omega$	19	20	21	
$I_{OL3}$		$V_O = 1.3\text{ V}$ , $R_{ext} = 200\ \Omega$	96	100	104	
$\Delta I_{OL1}$	Output current error between bit (all output ON)	$V_O = 0.3\text{ V}$ , $R_{ext} = 4.2\text{ k}\Omega$		$\pm 5$	$\pm 8$	%
$\Delta I_{OL2}$		$V_O = 0.3\text{ V}$ , $R_{ext} = 1\text{ k}\Omega$		$\pm 1.5$	$\pm 3$	
$\Delta I_{OL3}$		$V_O = 1.3\text{ V}$ , $R_{ext} = 200\ \Omega$		$\pm 1.2$	$\pm 3$	
$R_{SIN(up)}$	Pull-up resistor		150	300	600	k $\Omega$
$R_{SIN(down)}$	Pull-down resistor		100	200	400	k $\Omega$
$I_{DD(OFF1)}$	Supply current (OFF)	$R_{ext} = 1\text{ k}\Omega$ , OUT 0 to 15 = OFF		4		mA
$I_{DD(OFF2)}$		$R_{ext} = 250\ \Omega$ , OUT 0 to 15 = OFF		11.2		
$I_{DD(ON1)}$	Supply current (ON)	$R_{ext} = 1\text{ k}\Omega$ , OUT 0 to 15 = ON		4.5		
$I_{DD(ON2)}$		$R_{ext} = 250\ \Omega$ , OUT 0 to 15 = ON		11.7		
Thermal	Thermal protection			170		$^\circ\text{C}$

$V_{DD} = 5\text{ V}$ ,  $T_A = 25\text{ °C}$ , unless otherwise specified.

Table 8: Switching characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	
$t_{PLH1}$	Propagation delay time, CLK- $\overline{\text{OUTn}}$ , LE = H, $\overline{\text{OE}} = \text{L}$		$V_{DD} = 3.3\text{ V}$	-	175	227	ns
			$V_{DD} = 5\text{ V}$	-	159	206	
$t_{PLH2}$	Propagation delay time, LE- $\overline{\text{OUTn}}$ , $\overline{\text{OE}} = \text{L}$		$V_{DD} = 3.3\text{ V}$	-	176	228	ns
			$V_{DD} = 5\text{ V}$	-	158	205	
$t_{PLH3}$	Propagation delay time, $\overline{\text{OE}} - \overline{\text{OUTn}}$ , LE = H		$V_{DD} = 3.3\text{ V}$	-	235	305	ns
			$V_{DD} = 5\text{ V}$	-	192	250	
$t_{PLH}$	Propagation delay time, CLK-SDO		$V_{DD} = 3.3\text{ V}$	-	20	26	ns
			$V_{DD} = 5\text{ V}$	-	14	18	
$t_{PHL1}$	Propagation delay time, CLK- $\overline{\text{OUTn}}$ , LE = H, $\overline{\text{OE}} = \text{L}$	$V_{IH} = V_{DD}$ $V_{IL} = \text{GND}$ $C_L = 10\text{ pF}$ $I_O = 20\text{ mA}$ $V_L = 3.0\text{ V}$ $R_{\text{-EXT}} = 1\text{ K}\Omega$ $R_L = 60\text{ }\Omega$	$V_{DD} = 3.3\text{ V}$	-	70	91	ns
			$V_{DD} = 5\text{ V}$	-	68	88	
$t_{PHL2}$	Propagation delay time, LE- $\overline{\text{OUTn}}$ , $\overline{\text{OE}} = \text{L}$		$V_{DD} = 3.3\text{ V}$	-	56	73	ns
			$V_{DD} = 5\text{ V}$	-	54	70	
$t_{PHL3}$	Propagation delay time, $\overline{\text{OE}} - \overline{\text{OUTn}}$ , LE = H		$V_{DD} = 3.3\text{ V}$	-	102	132	ns
			$V_{DD} = 5\text{ V}$	-	100	130	
$t_{PHL}$	Propagation delay time, CLK-SDO		$V_{DD} = 3.3\text{ V}$	-	25	32	ns
			$V_{DD} = 5\text{ V}$	-	17	22	
$t_{ON}$	Output rise time 10~90% of voltage waveform		$V_{DD} = 3.3\text{ V}$	-	116	150	ns
			$V_{DD} = 5\text{ V}$	-	108	140	
$t_{OFF}$	Output fall time 90~10% of voltage waveform		$V_{DD} = 3.3\text{ V}$	-	80	104	ns
			$V_{DD} = 5\text{ V}$	-	80	104	
$t_r$	CLK rise time <sup>(1)</sup>		-		5000	ns	
$t_f$	CLK fall time <sup>(1)</sup>		-		5000	ns	

**Notes:**

<sup>(1)</sup> In order to achieve high cascade data transfer, please consider  $t_r/t_f$  timings carefully.

### 4 Equivalent circuit and outputs

Figure 2: OE terminal

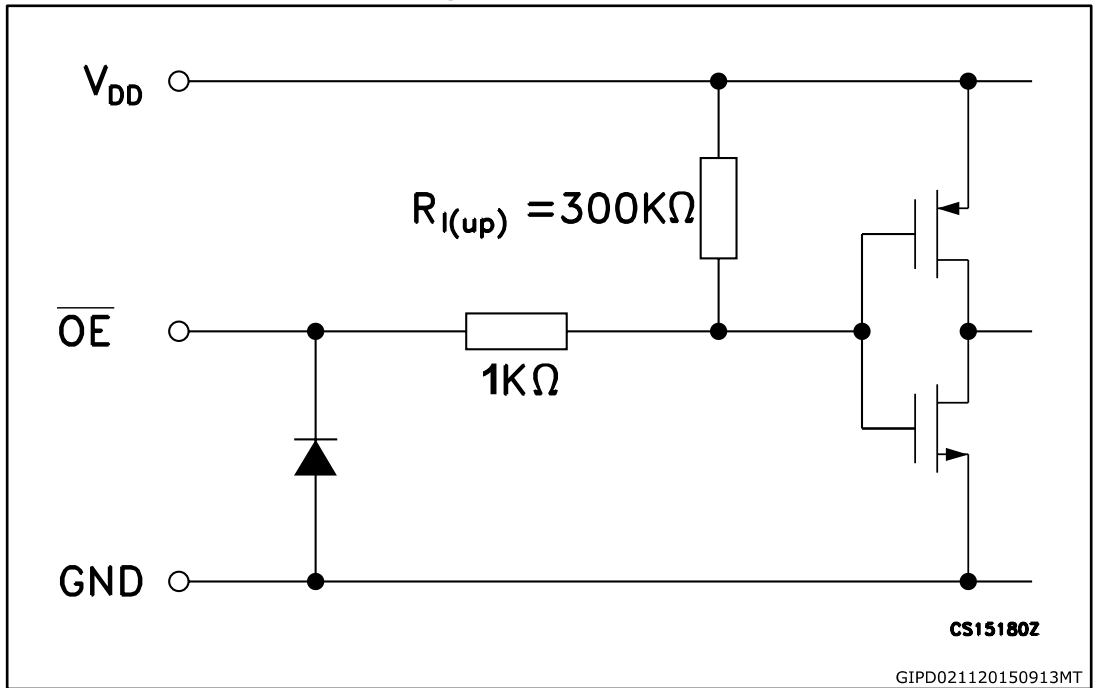


Figure 3: LE terminal

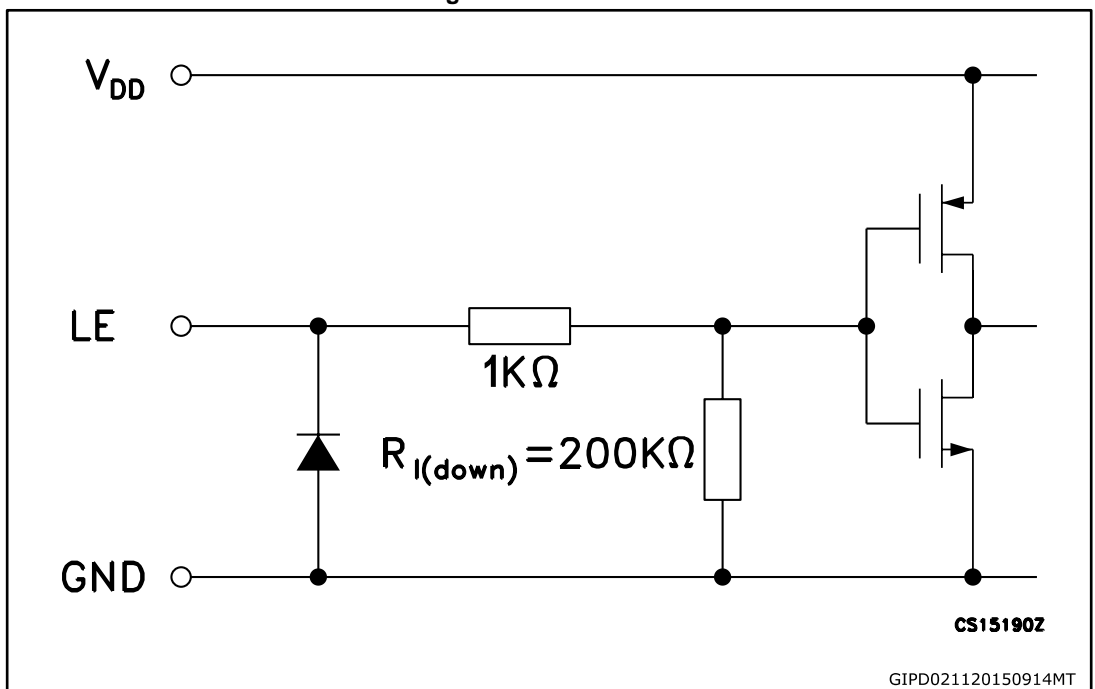




Figure 4: CLK, SDI terminal



Figure 5: SDO terminal

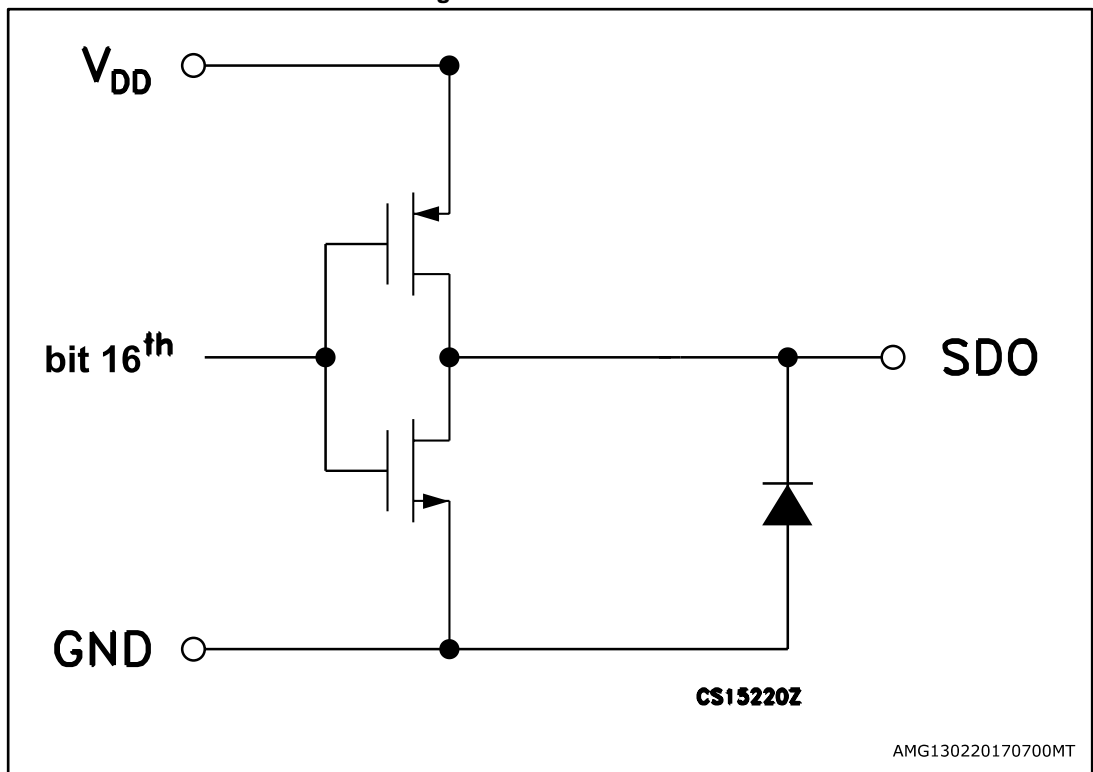
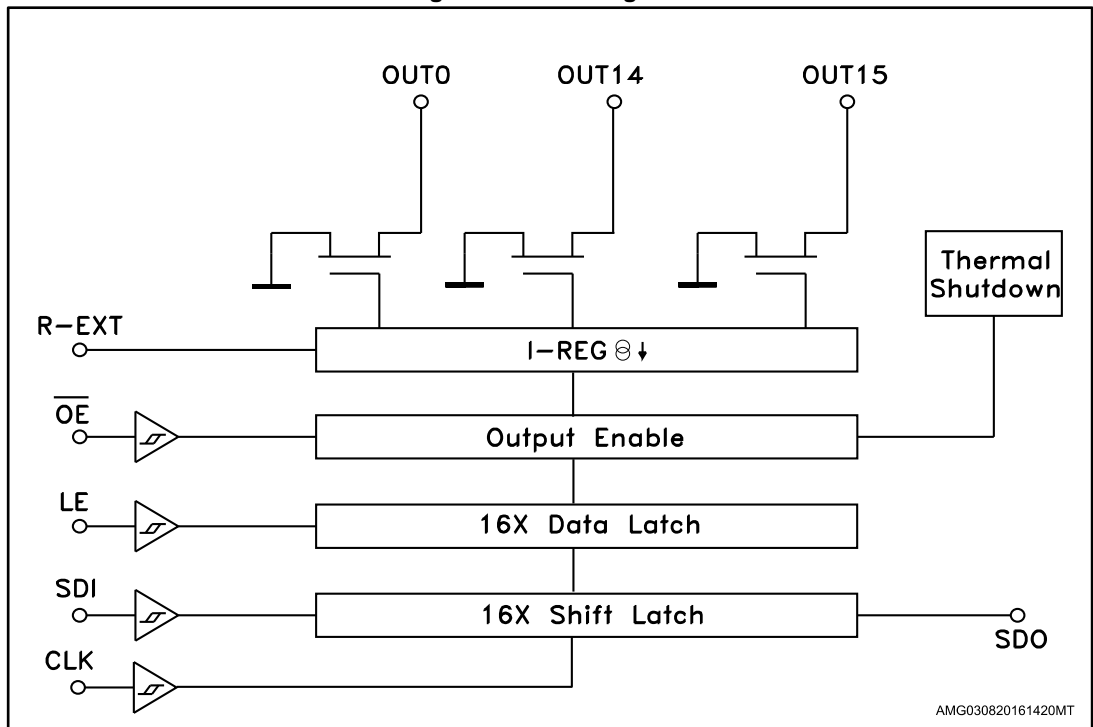


Figure 6: Block diagram



# 5 Timing diagrams

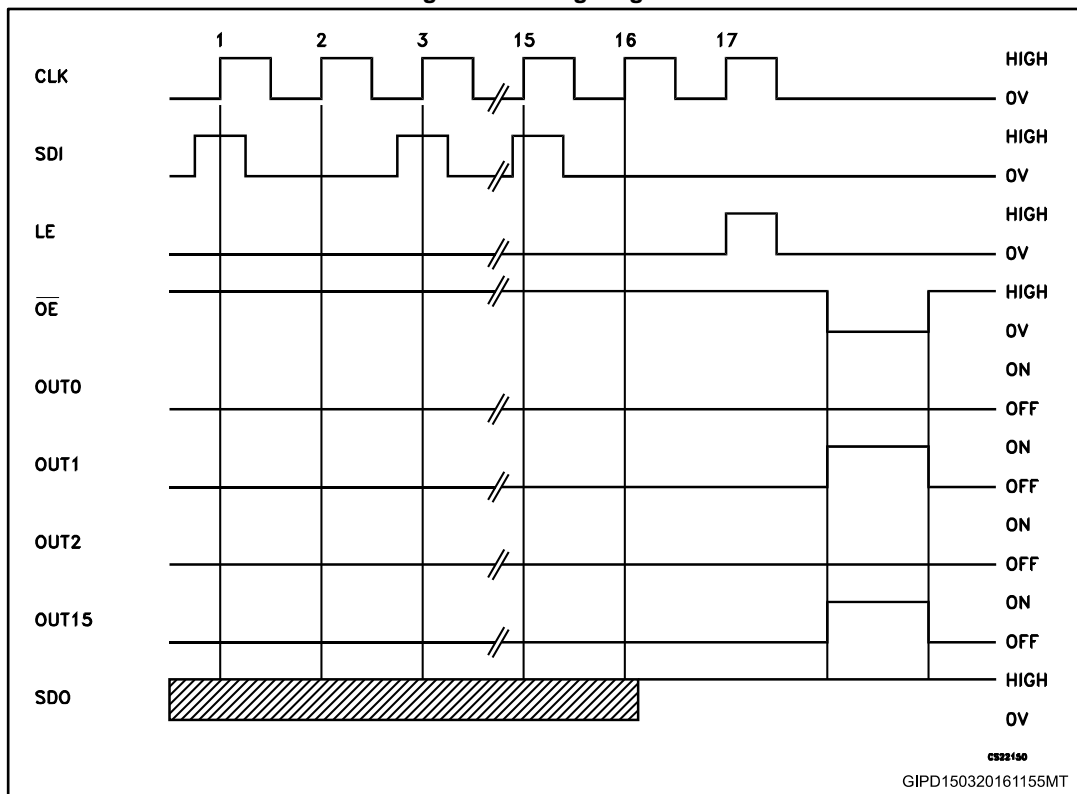
Table 9: Truth table

CLOCK	LE	$\overline{OE}$	Serial-IN	$\overline{OUT0}$ ..... $\overline{OUT7}$ ..... $\overline{OUT15}$	SDO
$\downarrow$	H	L	Dn	Dn ..... Dn - 7 ..... Dn -15	Dn - 15
$\downarrow$	L	L	Dn + 1	No change	Dn - 14
$\downarrow$	H	L	Dn + 2	Dn + 2 ..... Dn - 5 ..... Dn -13	Dn - 13
$\downarrow$	X	L	Dn + 3	Dn + 2 ..... Dn - 5 ..... Dn -13	Dn - 13
$\downarrow$	X	H	Dn + 3	OFF	Dn - 13



OUTn = ON when Dn = H OUTn = OFF when Dn = L.

Figure 7: Timing diagram



1 When LE terminal is at high level, latch circuit does not hold the data it passes from the input to the output.

2 When  $\overline{OE}$  terminal is at low level, output terminals OUT0 to OUT15 respond to the data, either ON or OFF.

3 When  $\overline{OE}$  terminal is at high level, it switches off all the data on the output terminal.

Figure 8: Clock, serial-in, serial-out

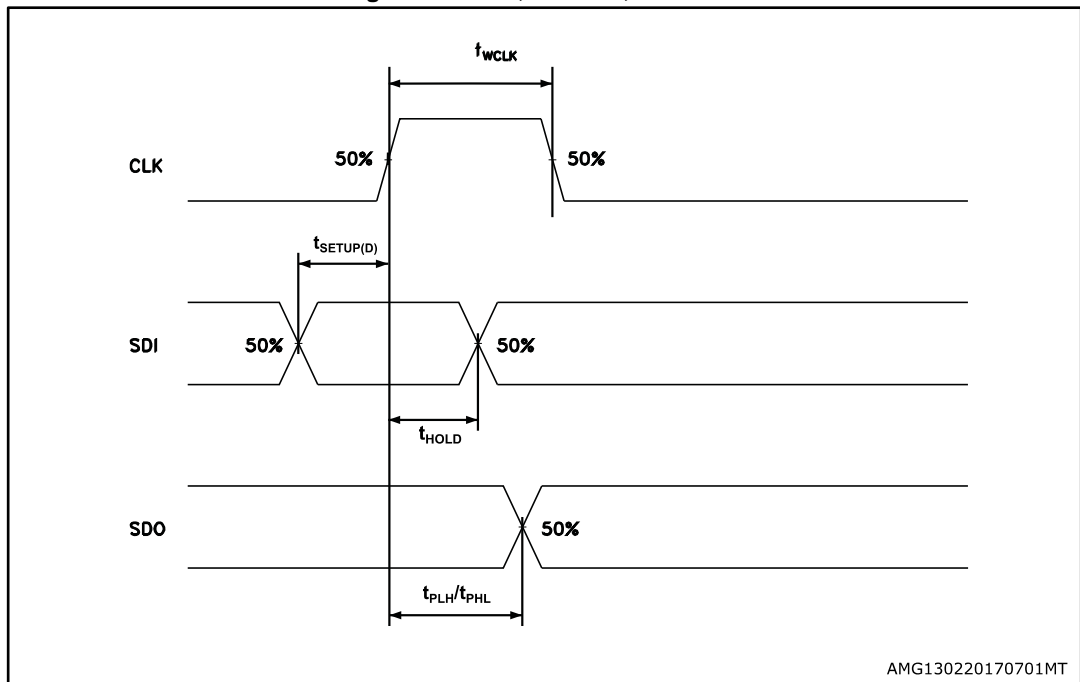


Figure 9: Clock, serial-in, latch, enable, outputs



Figure 10: Outputs



## 6 Typical characteristics

Figure 11: Output current-R-EXT resistor

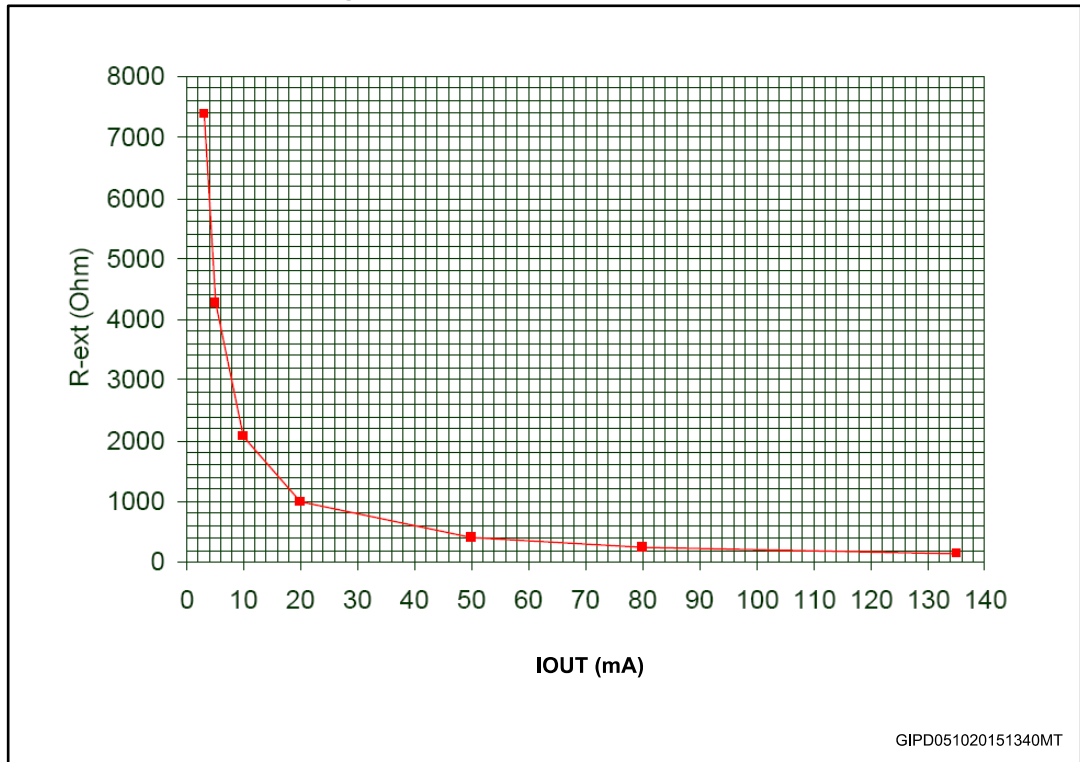


Table 10: Output current-R-EXT resistor

R-EXT (Ω)	Output current (mA)
7370	3
4270	5
2056	10
1006	20
382	50
251	80
200	100

Figure 12: Output current vs  $\pm \Delta I_{OL}(\%)$   $T_A = 25^\circ C$

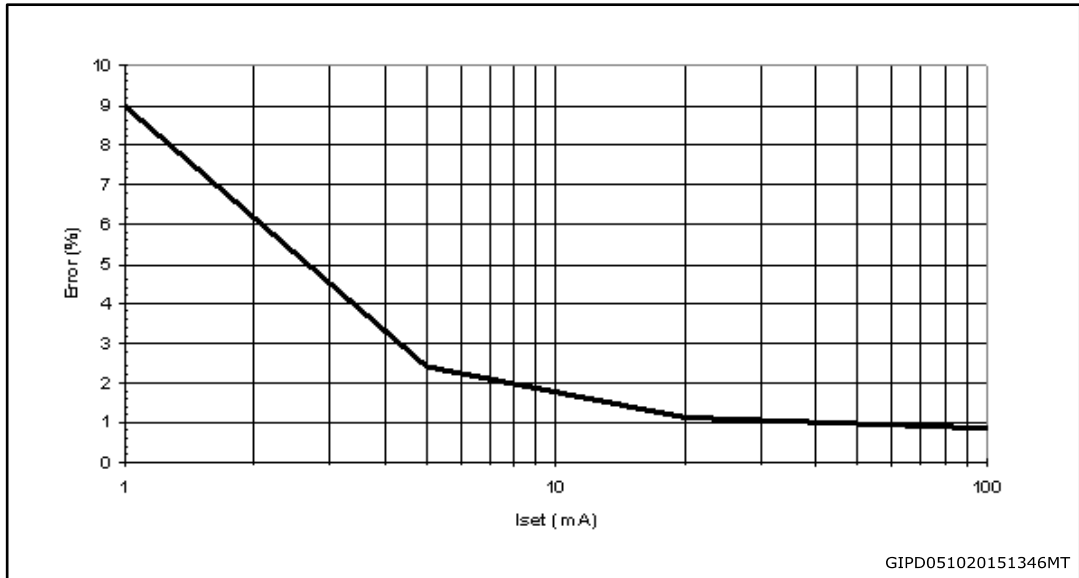


Figure 13:  $I_{SET}$  vs drop out voltage ( $V_{drop}$ )  $T_A = 25^\circ C$

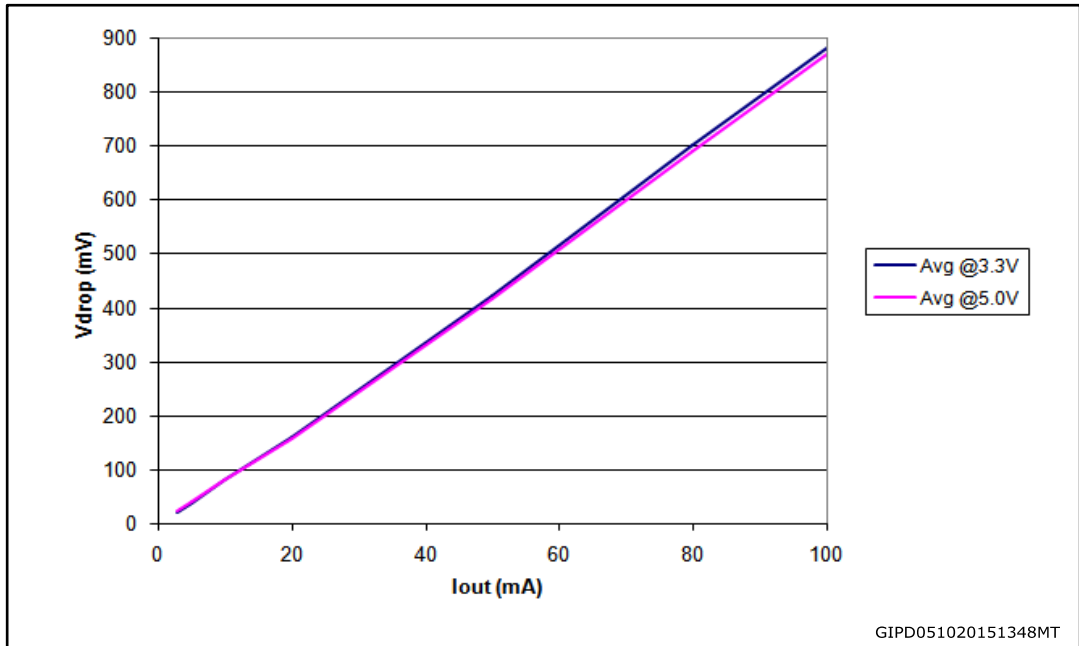


Table 11:  $I_{SET}$  vs dropout voltage ( $V_{drop}$ )

Iout (mA)	Avg @ 3.3 V	Avg @ 5.0 V
3	20	22
5	37	40
10	79	79
20	160	158
50	422	415
80	700	690
100	880	870

Figure 14:  $I_{DD}$  ON/OFF,  $T_A = 25\text{ }^\circ\text{C}$





# 7 Test circuits

Figure 15: DC characteristic

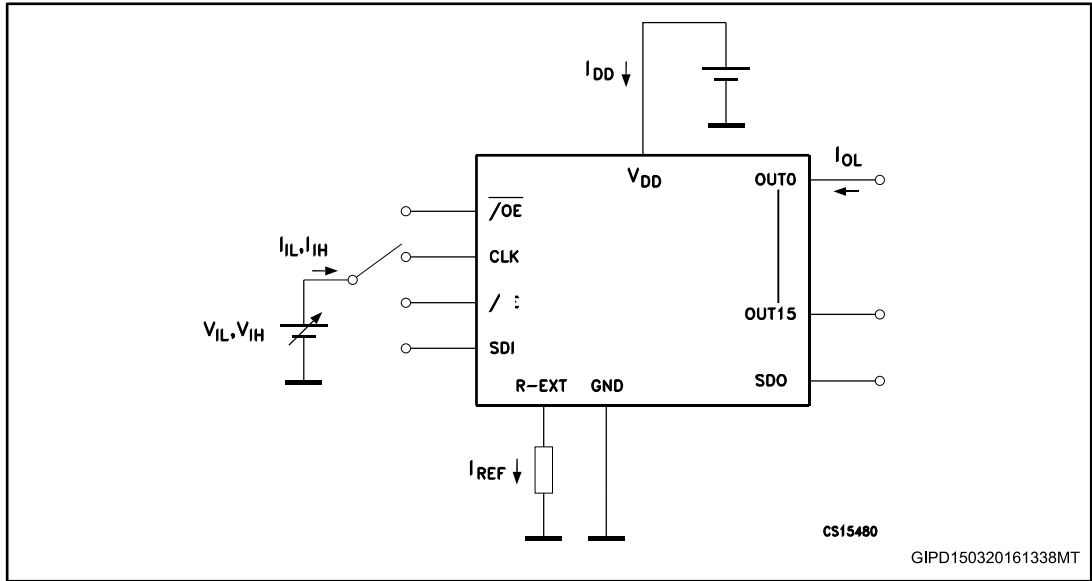


Figure 16: AC characteristic

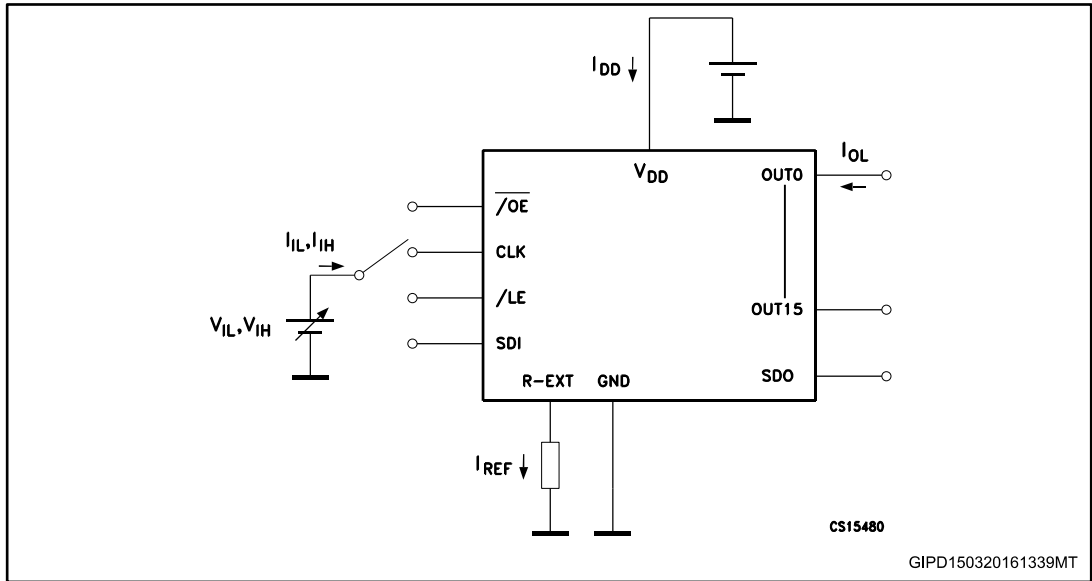
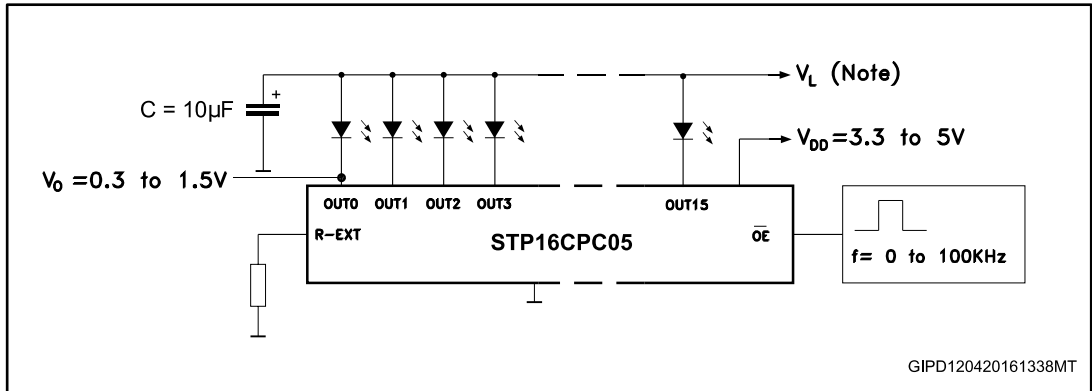


Figure 17: Typical application schematic



$V_L$  will be determined by the  $V_F$  of the LEDs.

Test condition: temp. = 25 °C,  $V_{DD} = 3.0 \text{ V}$ ,  $C_L = 10 \text{ pF}$ , freq. = 1 MHz.

Figure 18: Turn ON output current setup

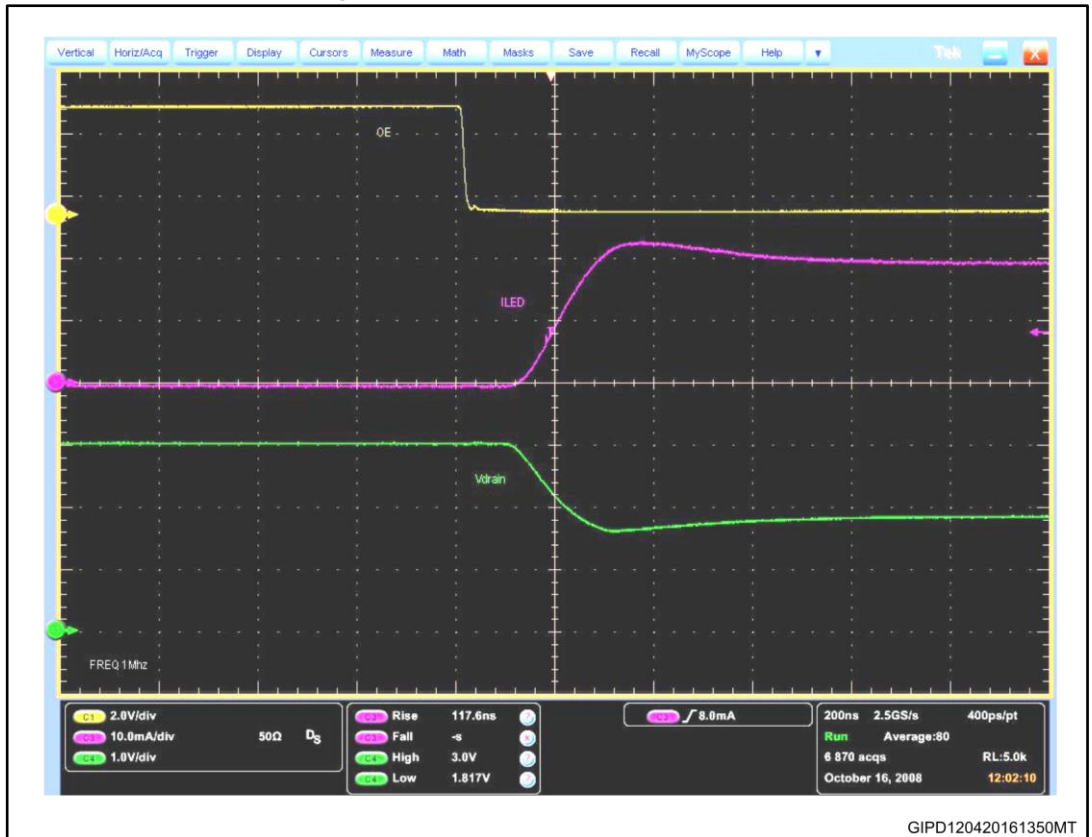
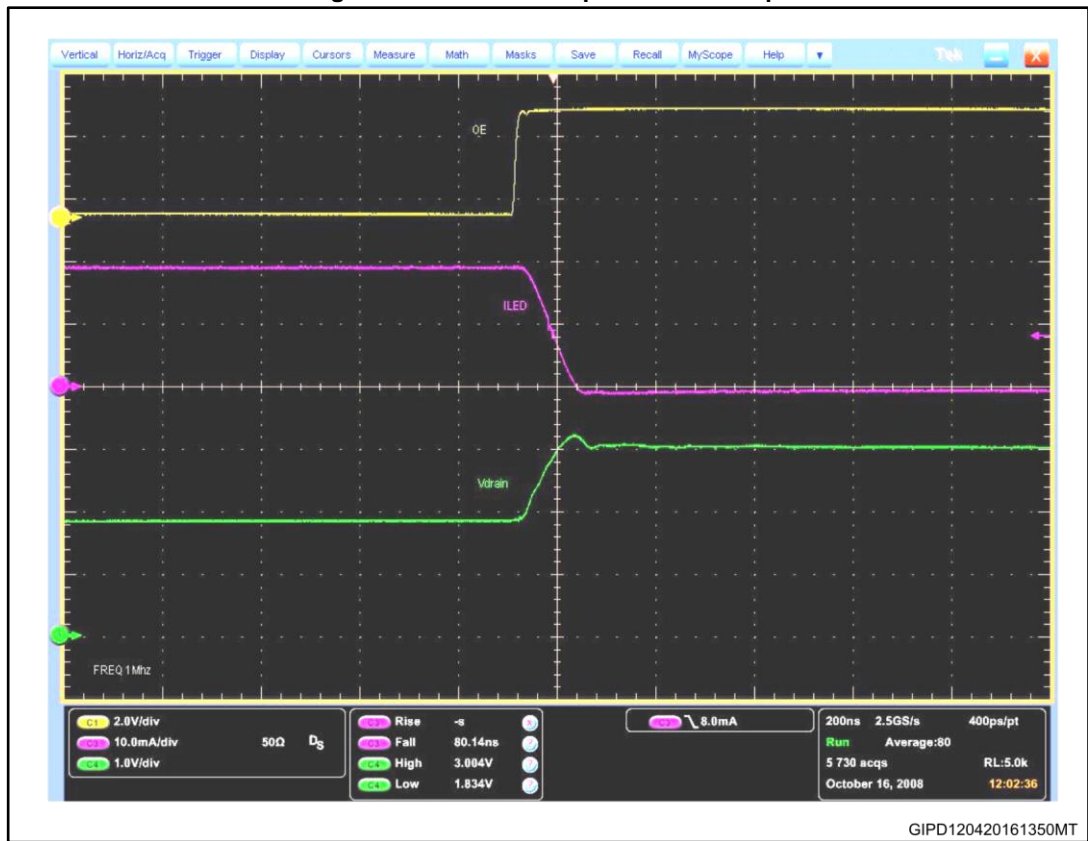


Figure 19: Turn OFF output current setup



## 8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 8.1 QSOP-24 package information

Figure 20: QSOP-24 package outline

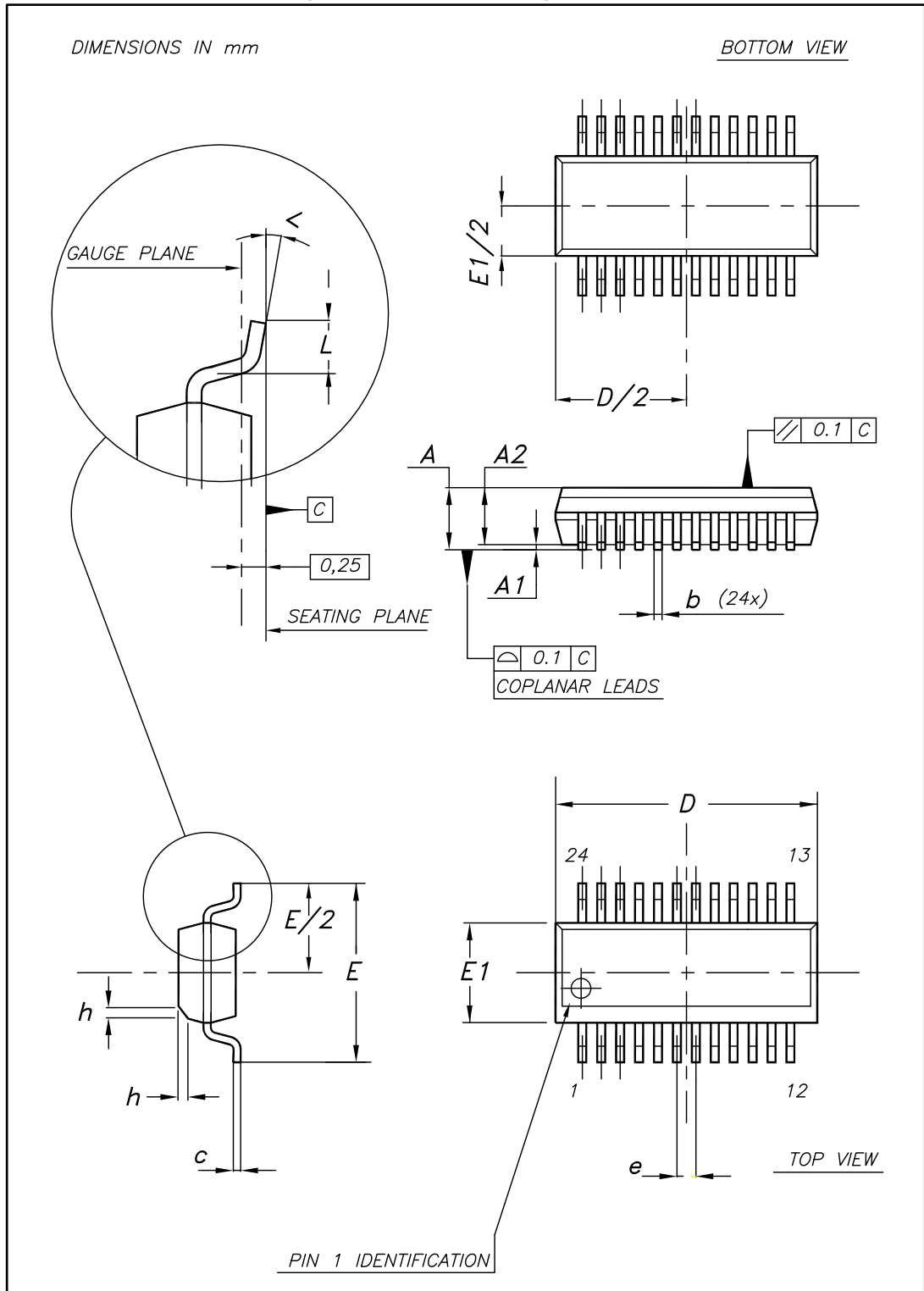


Table 12: QSOP-24 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	1.54	1.62	1.73
A1	0.10	0.15	0.25
A2		1.47	
b	0.20		0.31
c	0.17		0.254
D	8.56	8.66	8.76
E	5.80	6.00	6.20
E1	3.80	3.91	4.01
e		0.635	
L	0.40	0.635	0.89
h	0.25	0.33	0.41
<	0°		8°

### 8.2 SO-24 package information

Figure 21: SO-24 package outline



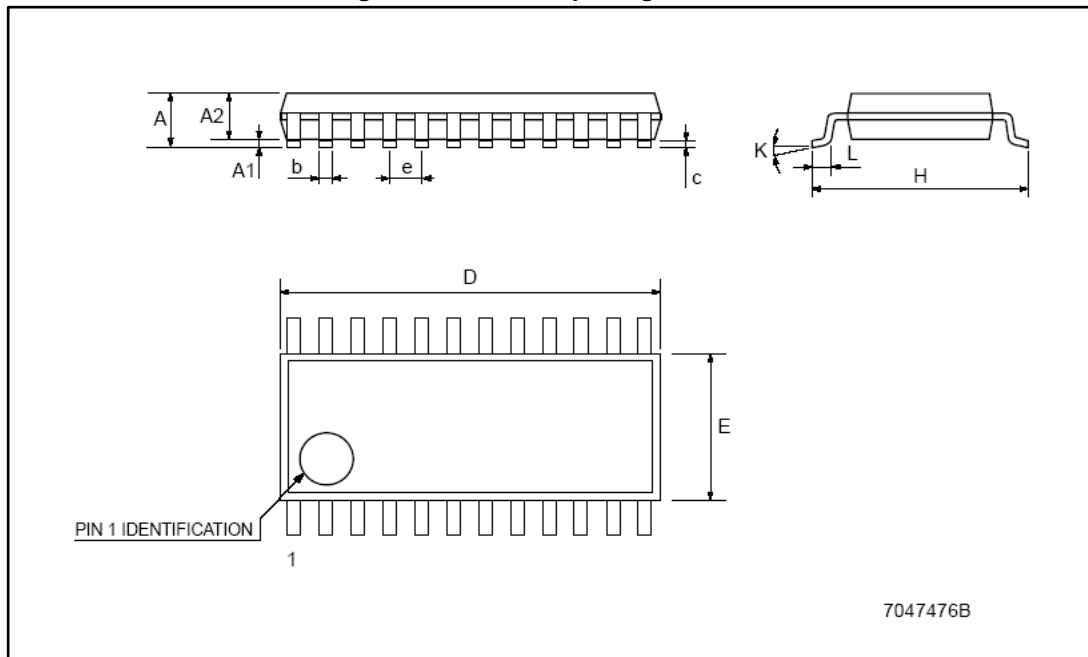
0070769

Table 13: SO-24 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.35		2.65
A1	0.10		0.30
B	0.33		0.51
C	0.23		0.32
D	15.20		15.60
E	7.40		7.60
e		1.27	
H	10.00		10.65
h	0.25		0.75
L	0.40		1.27
k	0		8
ddd			0.10

### 8.3 TSSOP24 package information

Figure 22: TSSOP24 package outline



7047476B



Table 14: TSSOP24 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.1
A1	0.05		0.15
A2		0.9	
b	0.19		0.30
c	0.09		0.20
D	7.7		7.9
E	4.3		4.5
e		0.65 BSC	
H	6.25		6.5
K	0°		8°
L	0.50		0.70

### 8.4 TSSOP24 exposed pad package information

Figure 23: TSSOP24 exposed pad package outline

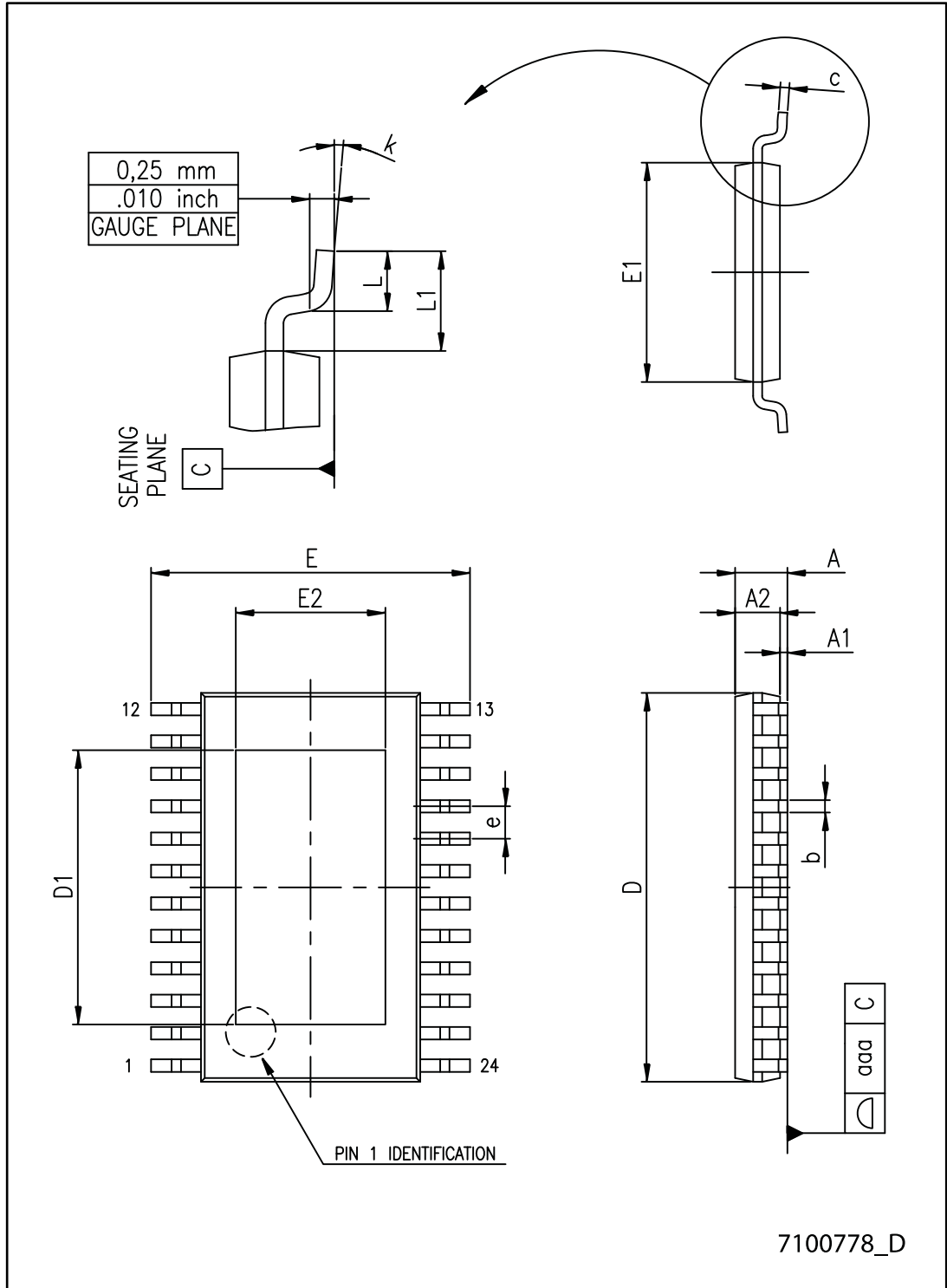


Table 15: TSSOP24 exposed pad mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.20
A1			0.15
A2	0.80	1.00	1.05
b	0.19		0.30
c	0.09		0.20
D	7.70	7.80	7.90
D1	4.80	5.00	5.2
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
E2	3.00	3.20	3.40
e		0.65	
L	0.45	060	075
L1		1.00	
k	0°		8°
aaa			0.10

### 8.5 TSSOP24, TSSOP24 exposed pad and SO-24 packing information

Figure 24: TSSOP24, TSSOP24 exposed pad and SO-24 reel outline



Table 16: TSSOP24 and TSSOP24 exposed pad tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A		-	330
C	12.8	-	13.2
D	20.2	-	
N	60	-	
T		-	22.4
Ao	6.8	-	7
Bo	8.2	-	8.4
Ko	1.7	-	1.9
Po	3.9	-	4.1
P	11.9	-	12.1

Table 17: SO-24 tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A		-	330
C	12.8	-	13.2
D	20.2	-	
N	60	-	
T		-	30.4
Ao	10.8	-	11.0
Bo	15.7	-	15.9
Ko	2.9	-	3.1
Po	3.9	-	4.1
P	11.9	-	12.1

## 9 Revision history

**Table 18: Document revision history**

Date	Revision	Changes
30-Jan-2009	1	First release
12-May-2009	2	Updated Table 6 on page 6
29-Oct-2009	3	Updated Note: on page 3
16-Jun-2014	4	Updated <i>Section 8: Package mechanical data</i> . Added <i>Section 9: Packaging mechanical data</i> . Minor text changes.
08-Mar-2017	5	Updated <i>Table 5: "Thermal data"</i> , <i>Figure 5: "SDO terminal"</i> , <i>Figure 8: "Clock, serial-in, serial-out"</i> , <i>Figure 9: "Clock, serial-in, latch, enable, outputs"</i> and <i>Section 8: "Package information"</i> . Minor text changes.

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[WS9620BDP](#) [FM6126QC](#) [TC7559C](#) [FM6565QB](#) [LYT3315D](#) [SCT2001ASIG](#) [SCT2024CSOG](#) [SCT2024CSSG](#) [SCT2024CSTG](#)  
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[DLD101Q-7](#) [WS2818B](#) [SCT2004CSOG](#) [SCT2026CSOG](#) [SCT2026CSSG](#) [SCT2026CSTG](#) [SCT2110CSSG](#) [SCT2932F](#) [SCT2932J](#) [PR4101A](#)  
[PR4404](#) [AS1130-BSST](#) [CP2155DN10-A1](#) [BCT3220ELA-TR](#) [AW2013DNR](#) [AW3641EDNR](#) [AW2023DNR](#) [WD3153D-10/TR](#) [LP3321QVF](#)  
[AW36404DNR](#) [AL8400SE-7](#) [CD4511BE](#)