



STP180N10F3

N-channel 100 V, 4.5 mΩ, 120 A STripFET™III Power MOSFET
TO-220

Features

Order codes	V _{DSS}	R _{DS(on)} max.	I _D
STP180N10F3	100 V	5.1 mΩ	120 A

- Ultra low on-resistance
- 100% avalanche tested

Applications

- High current switching applications

Description

This device is an N-channel enhancement mode Power MOSFET produced using STMicroelectronics' STripFET™ III technology, which is specifically designed to minimize on-resistance and gate charge to provide superior switching performance.

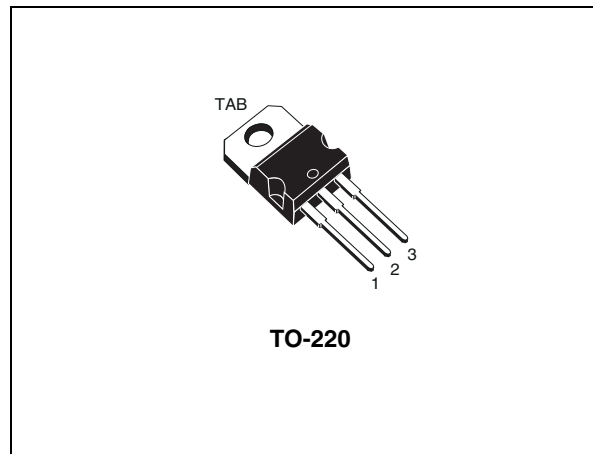


Figure 1. Internal schematic diagram

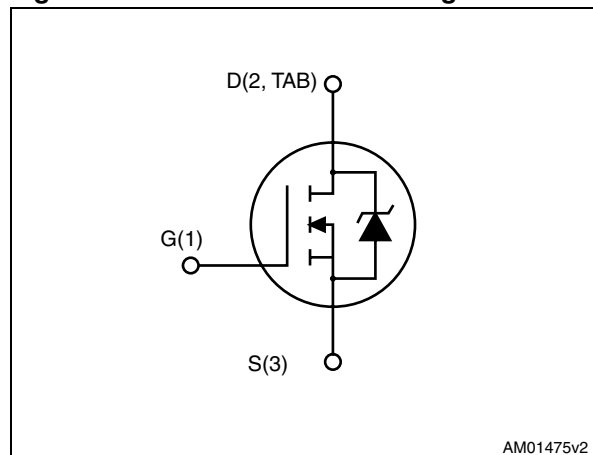


Table 1. Device summary

Order codes	Marking	Package	Packaging
STP180N10F3	180N10F3	TO-220	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS}=0$)	100	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	120	A
$I_D^{(1)}$	Drain current (continuous) at $T_C=100^\circ\text{C}$	110	A
$I_{DM}^{(2)}$	Drain current (pulsed)	480	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	315	W
	Derating factor	2.1	W/ $^\circ\text{C}$
dv/dt	Peak diode recovery voltage slope	20	V/ns
$E_{AS}^{(3)}$	Single pulse avalanche energy	350	mJ
T_j T_{stg}	Operating junction temperature storage temperature	- 55 to 175	$^\circ\text{C}$

1. Current limited by package.
2. Pulse width limited by safe operating area.
3. Starting $T_j = 25^\circ\text{C}$, $I_D = 80\text{ A}$, $V_{DD} = 50\text{ V}$.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case	0.48	$^\circ\text{C}/\text{W}$
Rthj-a	Thermal resistance junction-ambient max	62.5	$^\circ\text{C}/\text{W}$
T_l	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage ($V_{GS} = 0$)	$I_D = 250\ \mu\text{A}$	100			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 100\ \text{V}$ $V_{DS} = 100\ \text{V}, T_C = 125\text{ °C}$			10 100	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\ \text{V}$			± 200	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\ \text{V}, I_D = 60\ \text{A}$		4.5	5.1	m Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\ \text{V}, f = 1\ \text{MHz},$ $V_{GS} = 0$	-	6665	-	pF
C_{oss}	Output capacitance			786		pF
C_{rss}	Reverse transfer capacitance			49		pF
Q_g	Total gate charge	$V_{DD} = 50\ \text{V}, I_D = 120\ \text{A},$ $V_{GS} = 10\ \text{V}$ (see Figure 14)	-	114.6	-	nC
Q_{gs}	Gate-source charge			38.8		nC
Q_{gd}	Gate-drain charge			31.9		nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 50\ \text{V}, I_D = 60\ \text{A}$ $R_G = 4.7\ \Omega, V_{GS} = 10\ \text{V}$ (see Figure 13 , Figure 18)	-	25.6	-	ns
t_r	Rise time			97.1		ns
$t_{d(off)}$	Turn-off delay time			99.9		ns
t_f	Fall time			6.9		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)		-		120 480	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=120\text{ A}$, $V_{GS}=0$	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=120\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD}=80\text{ V}$, $T_j=150^\circ\text{C}$ (see Figure 15)	-	83.4 295.7 7.1		ns nC A

1. Pulse width limited by safe operating area.
2. Pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

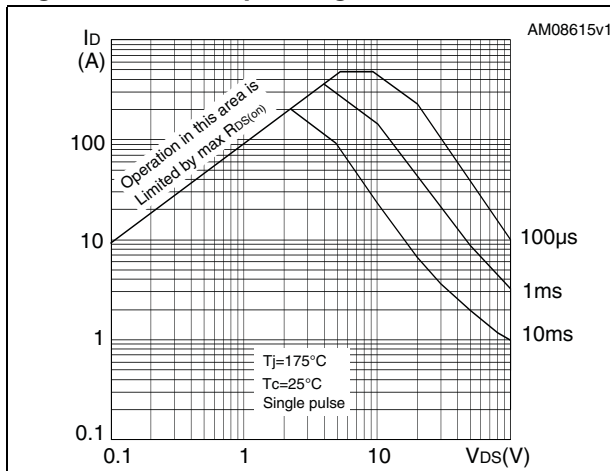


Figure 3. Thermal impedance

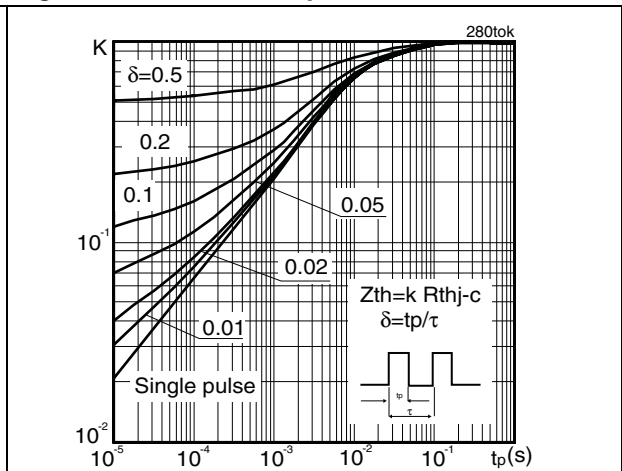


Figure 4. Output characteristics

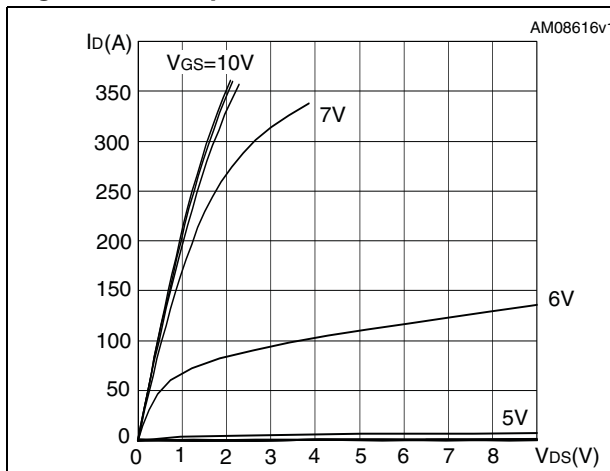


Figure 5. Transfer characteristics

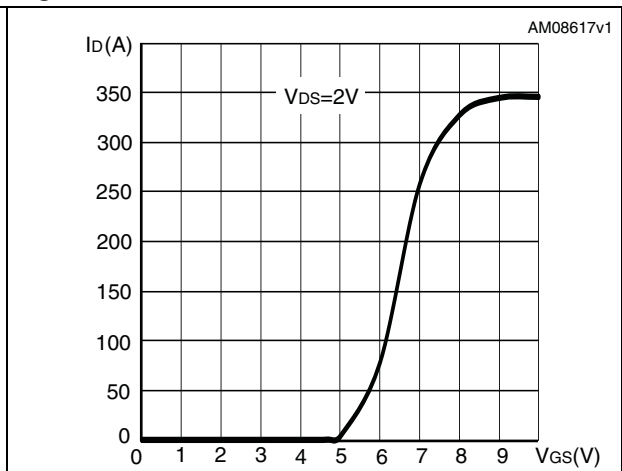


Figure 6. Static drain-source on resistance

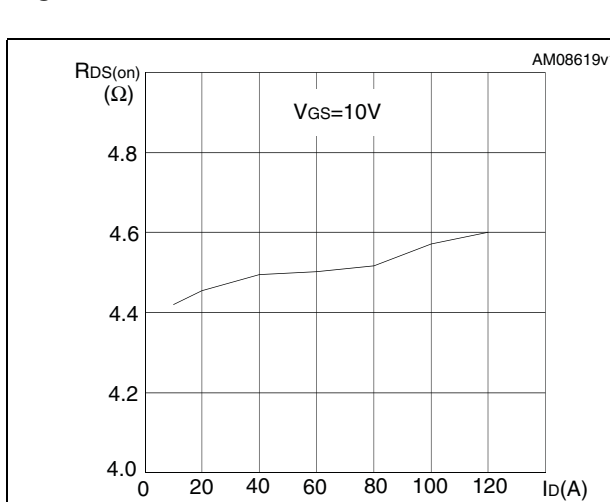


Figure 7. Source-drain diode forward characteristics

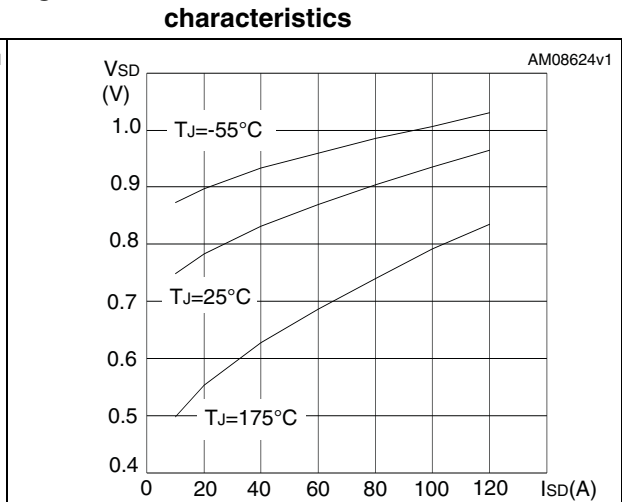


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

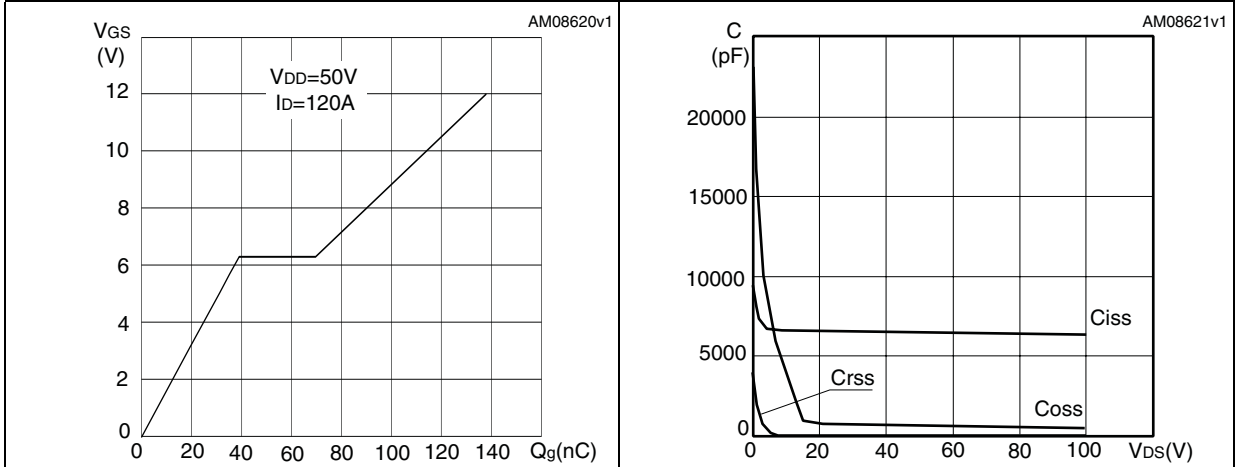


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

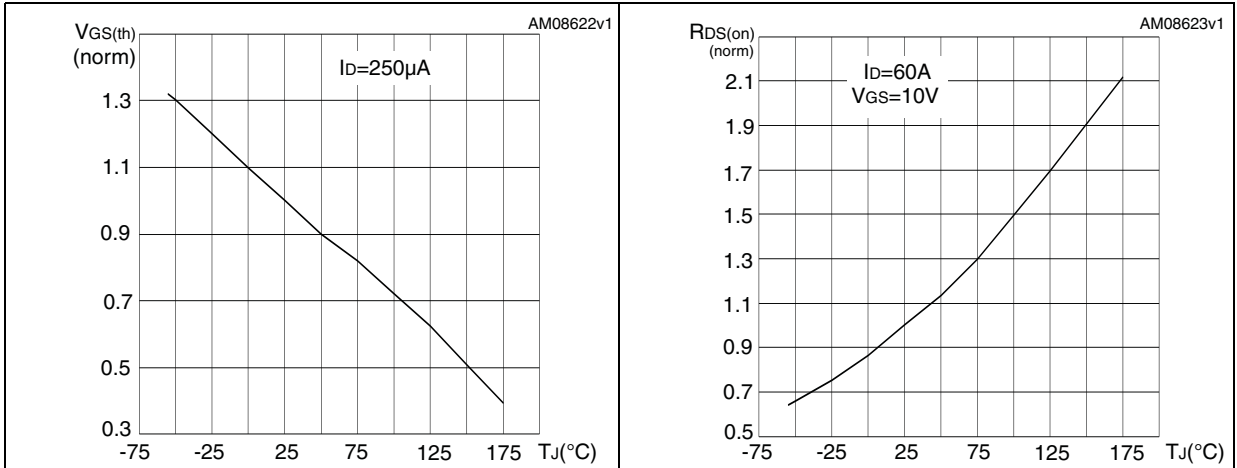
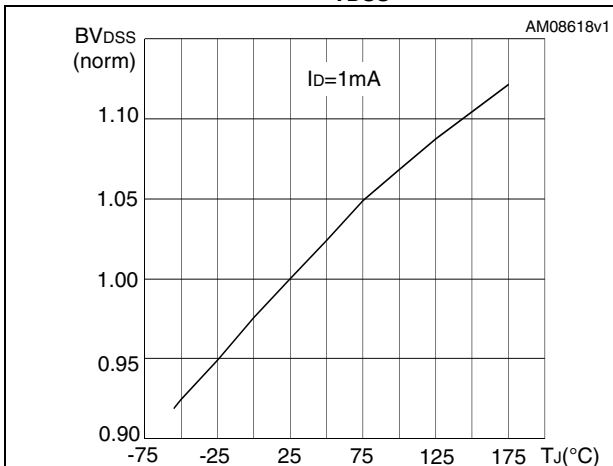


Figure 12. Normalized B_{VDSS} vs temperature



3 Test circuits

Figure 13. Switching times test circuit for resistive load



Figure 14. Gate charge test circuit

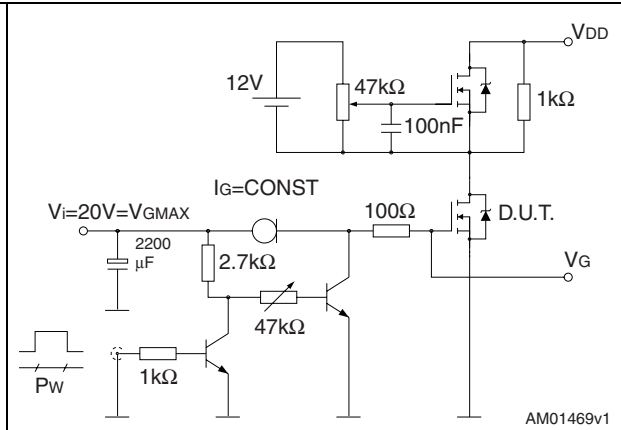


Figure 15. Test circuit for inductive load switching and diode recovery times

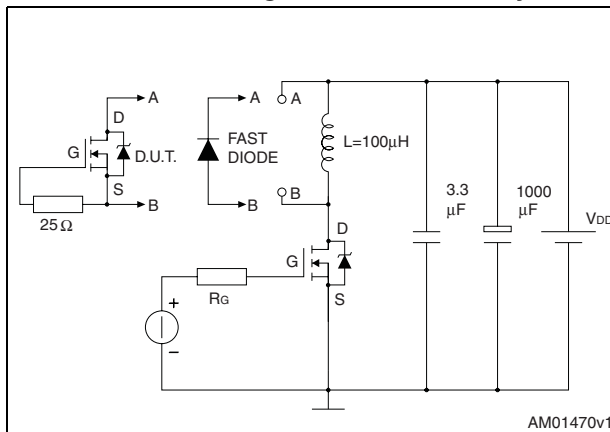


Figure 16. Unclamped inductive load test circuit

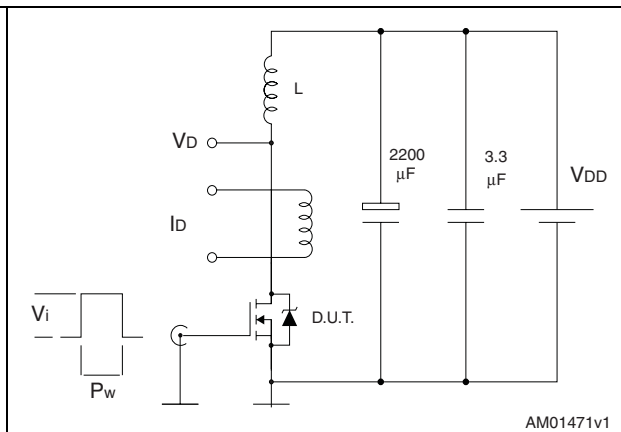


Figure 17. Unclamped inductive waveform

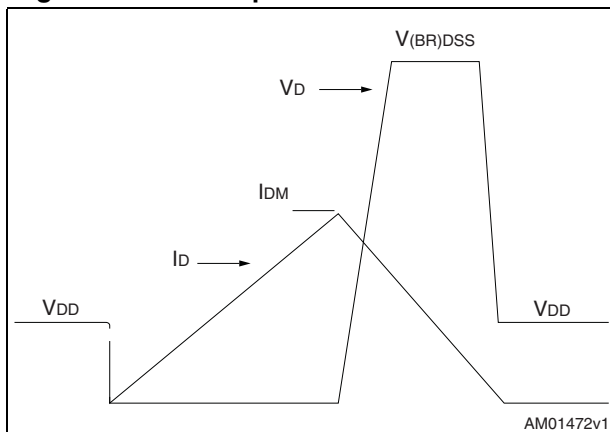
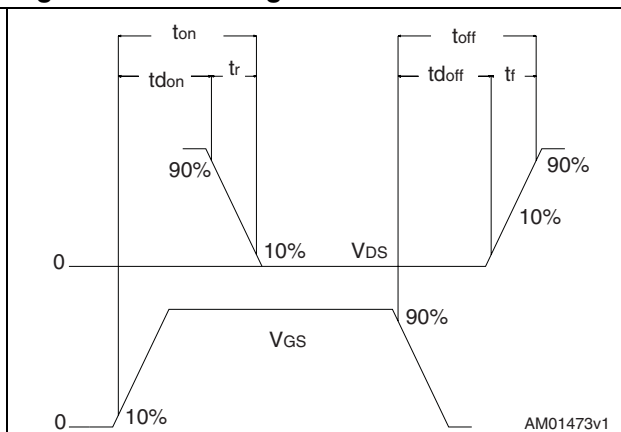


Figure 18. Switching time waveform



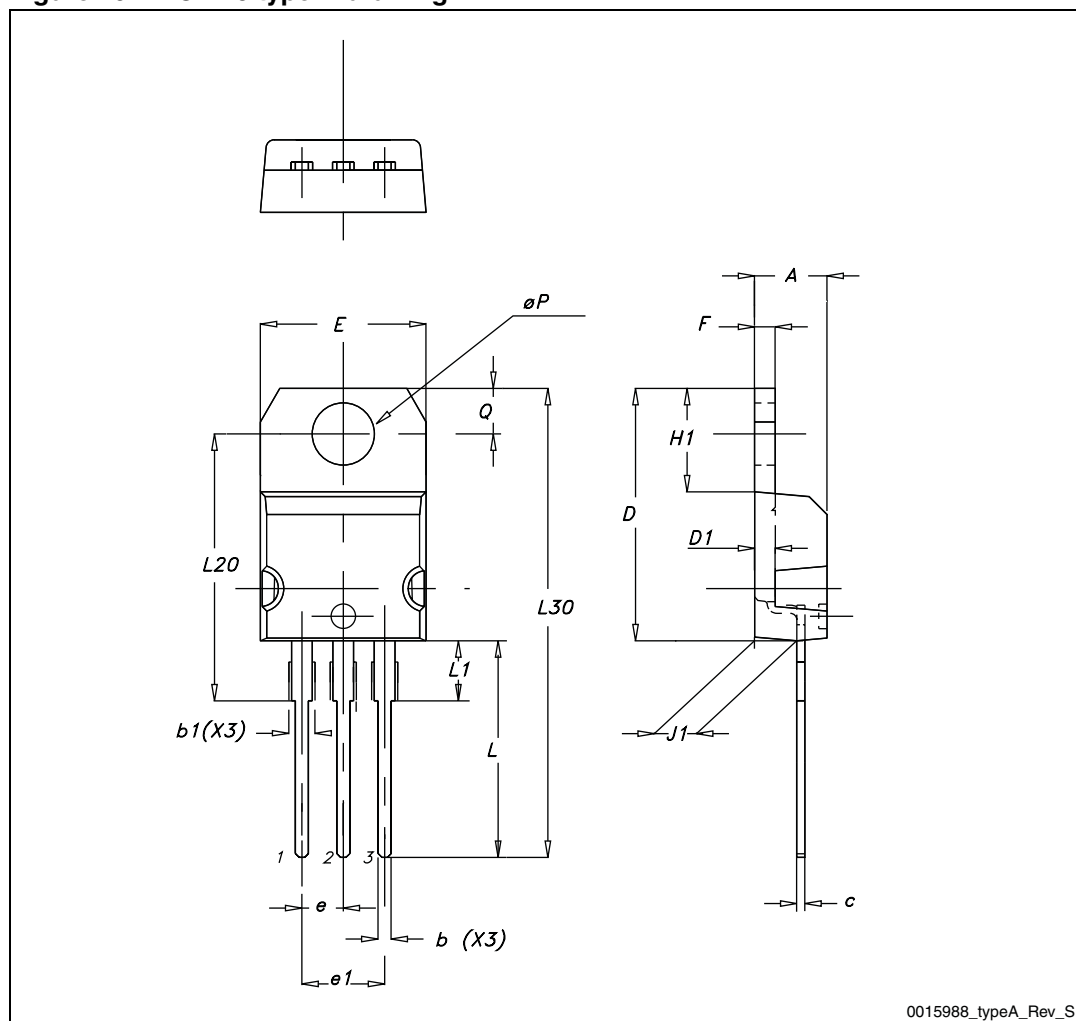
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

Figure 19. TO-220 type A drawing



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
01-Aug-2008	1	First version
03-Jun-2010	2	– Removed package, mechanical data: D ² PAK – Added new package mechanical data: H ² PAK
10-Mar-2011	3	Document status promoted from preliminary data to datasheet.
11-Jul-2011	4	Removed part number in H ² PAK.

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