



STP190N55LF3

N-channel 55 V, 2.9 mΩ, 120 A, TO-220
STripFET™ Power MOSFET

Features

Type	V _{DSS}	R _{DS(on)} max	I _D	P _D
STP190N55LF3	55 V	< 3.7 mΩ	120 A	312 W

- Logic level drive
- 100% avalanche tested

Application

- Switching applications
 - Automotive

Description

This n-channel enhancement mode Power MOSFET is the latest refinement of STMicroelectronics' unique "single feature size" strip-based process, which has decreased the critical alignment steps, offering remarkable manufacturing reproducibility. The outcome is a transistor with extremely high packing density for low on resistance, rugged avalanche characteristics and low gate charge.

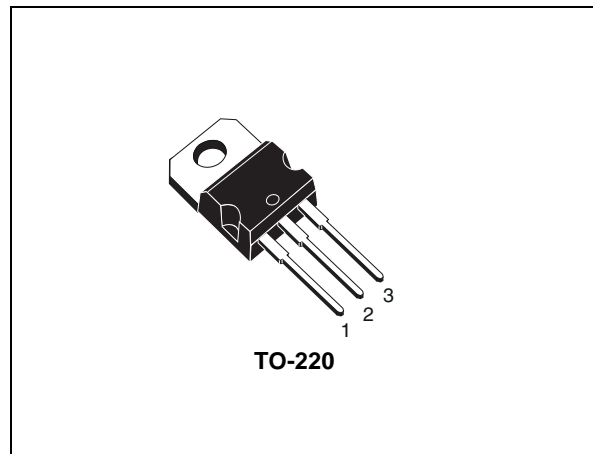


Figure 1. Internal schematic diagram

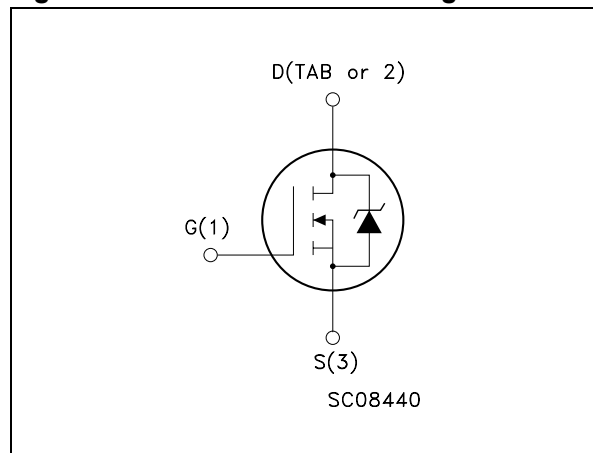


Table 1. Device summary

Order code	Marking	Package	Packaging
STP190N55LF3	190N55LF3	TO-220	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS}=0$)	55	V
V_{GS}	Gate-Source voltage	± 18	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	120	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	120	A
$I_{DM}^{(2)}$	Drain current (pulsed)	480	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	312	W
	Derating factor	2.08	W/ $^\circ\text{C}$
$E_{AS}^{(3)}$	Single pulse avalanche energy	1000	mJ
T_{stg}	Storage temperature	-55 to 175	$^\circ\text{C}$
T_j	Max. operating junction temperature	175	$^\circ\text{C}$

1. Current limited by package
2. Pulse width limited by safe operating area
3. Starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = 60\text{ A}$, $V_{DD} = 40\text{ V}$

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.48	$^\circ\text{C}/\text{W}$
R_{thj-a}	Thermal resistance junction-ambient max	62.5	$^\circ\text{C}/\text{W}$
T_L	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown Voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0$	55			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$, $V_{DS} = \text{Max rating}$, $T_c = 125\text{ °C}$			10 100	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 18\text{ V}$			± 200	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	1		2.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 30\text{ A}$ $V_{GS} = 5\text{ V}$, $I_D = 30\text{ A}$		2.9 3.3	3.7 4.5	$\text{m}\Omega$ $\text{m}\Omega$

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15\text{ V}$, $I_D = 60\text{ A}$		250		S
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$		6200		pF
C_{oss}	Output capacitance			1450		pF
C_{rss}	Reverse transfer capacitance			80		pF
Q_g	Total gate charge	$V_{DD} = 44\text{ V}$, $I_D = 120\text{ A}$ $V_{GS} = 5\text{ V}$ <i>(see Figure 16)</i>		60	80	nC
Q_{gs}	Gate-source charge			20		nC
Q_{gd}	Gate-drain charge			30		nC

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 6. Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	$V_{DD}=27.5\text{ V}$, $I_D=60\text{ A}$, $R_G=4.7\ \Omega$, $V_{GS}=10\text{ V}$ (see Figure 15), (see Figure 18)		20 40		ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	$V_{DD}=27.5\text{ V}$, $I_D=60\text{ A}$, $R_G=4.7\ \Omega$, $V_{GS}=10\text{ V}$ (see Figure 15), (see Figure 18)		160 40		ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current				120	A
I_{SDM}	Source-drain current (pulsed) ⁽¹⁾				480	A
V_{SD}	Forward on voltage	$I_{SD}=120\text{ A}$, $V_{GS}=0$			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=120\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD}=35\text{ V}$, $T_j=150\text{ }^\circ\text{C}$ (see Figure 17)		50 90 3.6		ns nC A

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

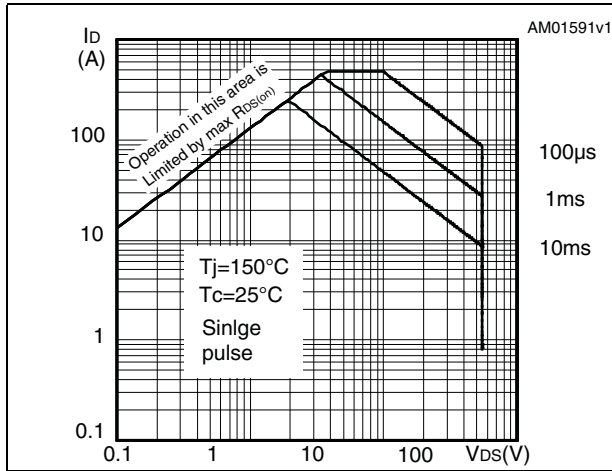


Figure 3. Thermal impedance

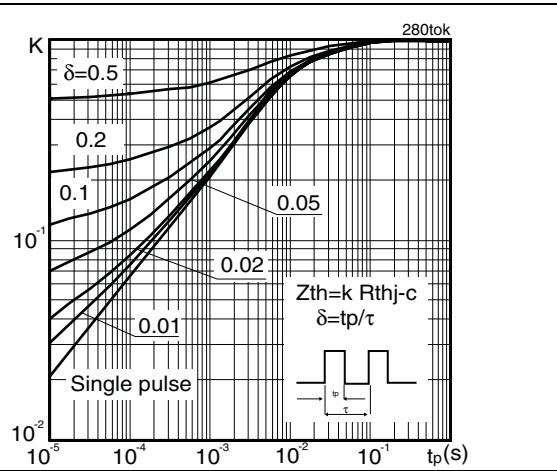


Figure 4. Output characteristics

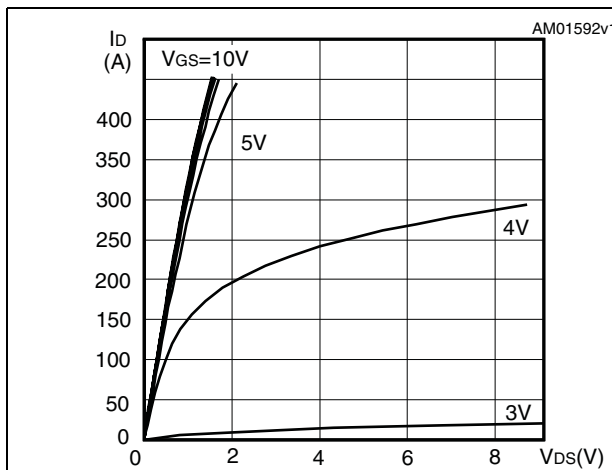


Figure 5. Transfer characteristics

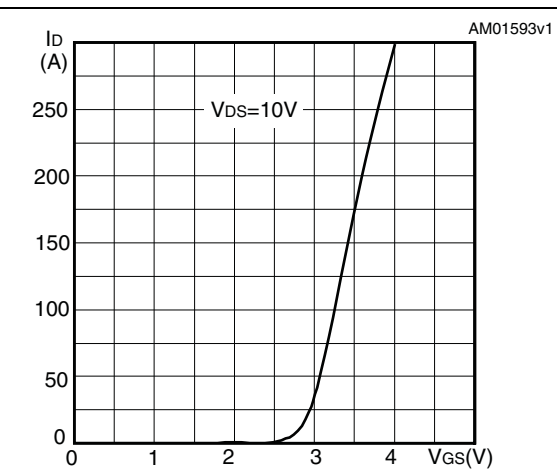


Figure 6. Normalized $B_{V_{DS}}$ vs temperature

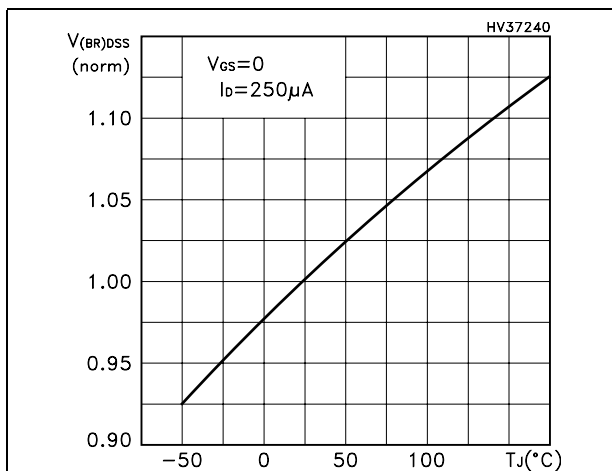


Figure 7. Static drain-source on resistance

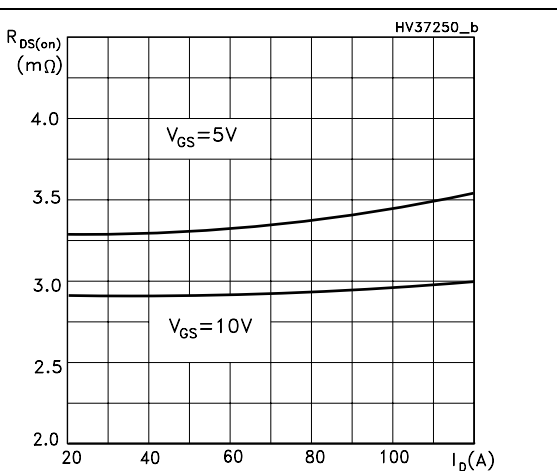


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

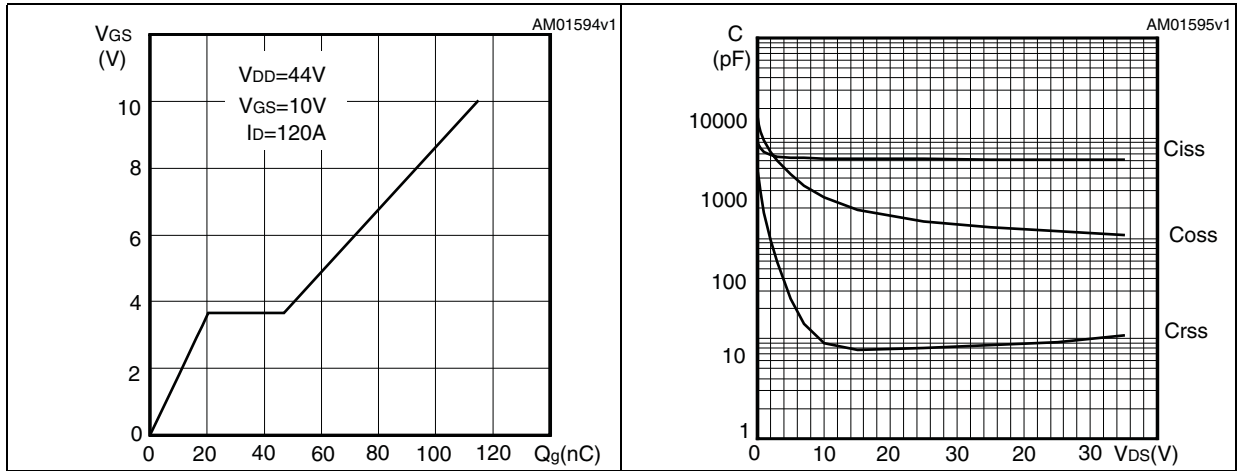


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

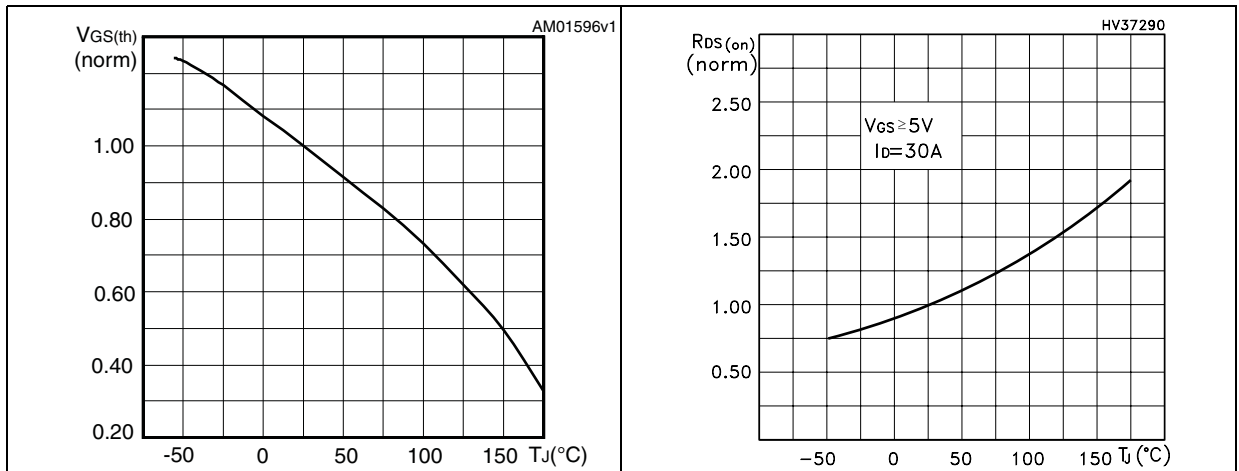
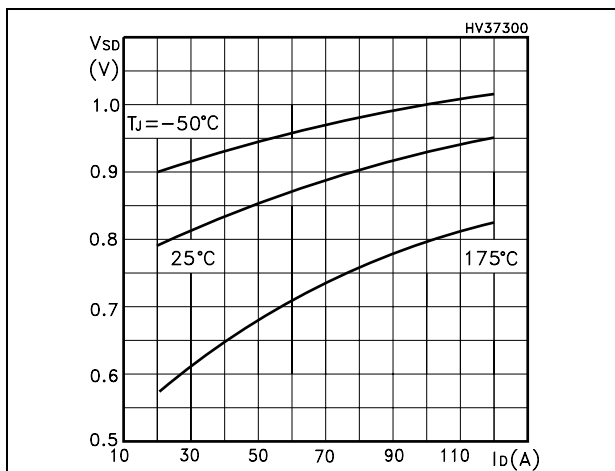


Figure 12. Source-drain diode forward characteristics



3 Test circuit

Figure 13. Unclamped inductive load test circuit



Figure 14. Unclamped inductive waveform

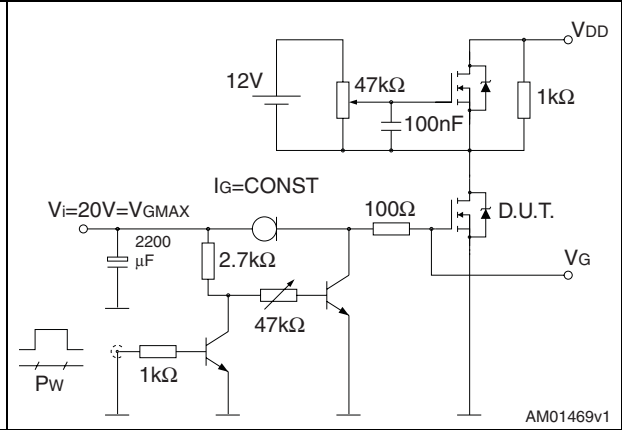


Figure 15. Switching times test circuit for resistive load

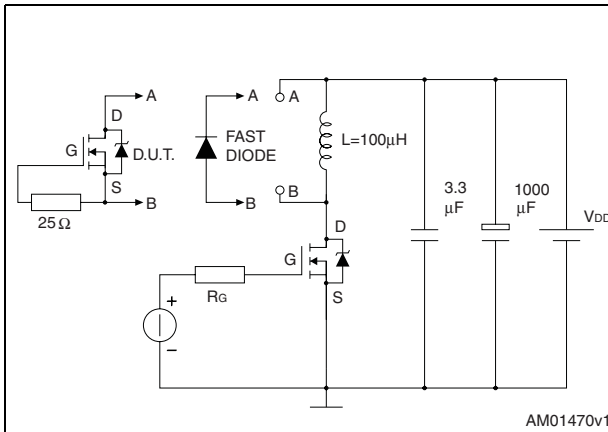


Figure 16. Gate charge test circuit

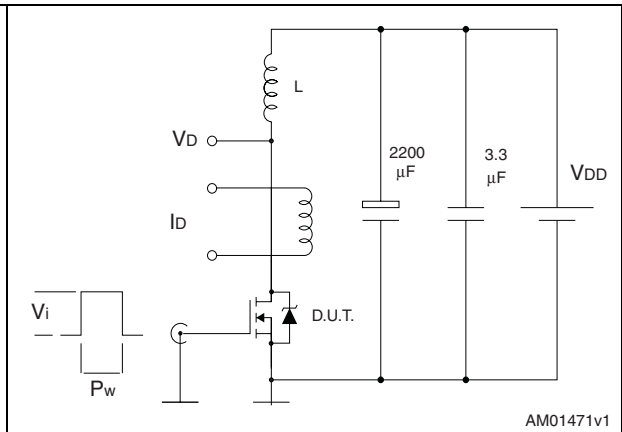


Figure 17. Test circuit for inductive load switching and diode recovery times

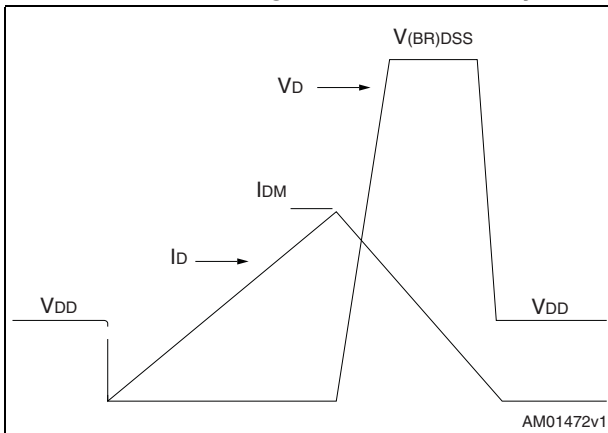
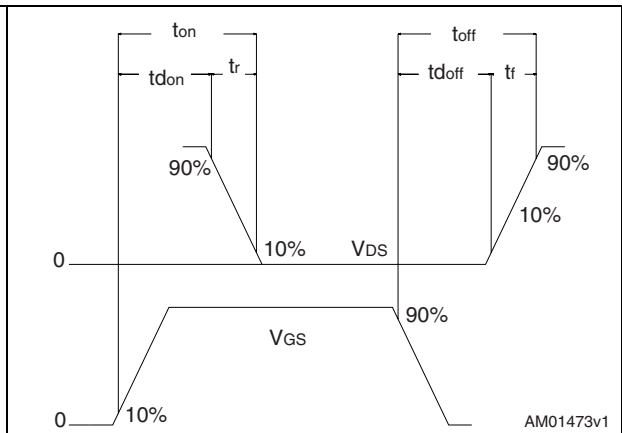


Figure 18. Switching time waveform

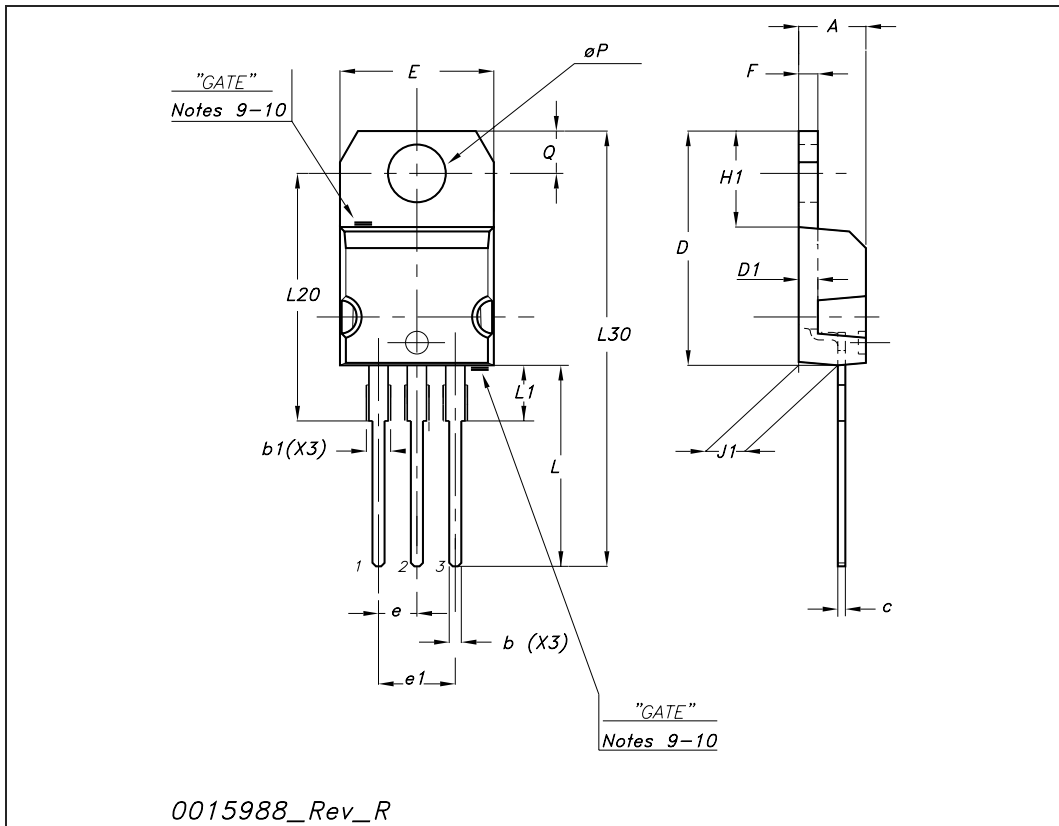


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

TO-220 mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.48		0.70	0.019		0.027
D	15.25		15.75	0.6		0.62
D1		1.27			0.050	
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.051
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
∅P	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



5 Revision history

Table 8. Document revision history

Date	Revision	Changes
05-Nov-2008	1	First release

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