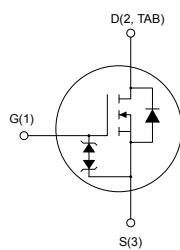
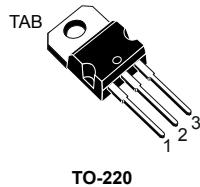


## N-channel 600 V, 165 mΩ typ., 18 A, MDmesh DM6 Power MOSFET in a TO-220 package

### Features



Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STP26N60DM6	600 V	195 mΩ	18 A

- Fast-recovery body diode
- Lower R<sub>DS(on)</sub> per area vs previous generation
- Low gate charge, input capacitance and resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

### Applications

- Switching applications

### Description

This high-voltage N-channel Power MOSFET is part of the MDmesh DM6 fast-recovery diode series. Compared with the previous MDmesh fast generation, DM6 combines very low recovery charge (Q<sub>rr</sub>), recovery time (t<sub>rr</sub>) and excellent improvement in R<sub>DS(on)</sub> per area with one of the most effective switching behaviors available in the market for the most demanding high-efficiency bridge topologies and ZVS phase-shift converters.



#### Product status link

[STP26N60DM6](#)

#### Product summary

Order code	STP26N60DM6
Marking	26N60DM6
Package	TO-220
Packing	Tube

## 1 Electrical ratings

**Table 1.** Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	18	A
	Drain current (continuous) at $T_C = 100^\circ\text{C}$	11	A
$I_{DM}^{(1)}$	Drain current (pulsed)	60	A
$P_{TOT}$	Total power dissipation at $T_C = 25^\circ\text{C}$	130	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	100	V/ns
$di/dt^{(2)}$	Peak diode recovery current slope	1000	A/ $\mu\text{s}$
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	100	V/ns
$T_{stg}$	Storage temperature range	-55 to 150	$^\circ\text{C}$
$T_j$	Operating junction temperature range		

1. Pulse width is limited by safe operating area.
2.  $I_{SD} \leq 18 \text{ A}$ ,  $V_{DS}$  (peak) <  $V_{(BR)DSS}$ ,  $V_{DD} = 400 \text{ V}$ .
3.  $V_{DS} \leq 480 \text{ V}$

**Table 2.** Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.96	$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	62.5	$^\circ\text{C/W}$

**Table 3.** Avalanche characteristics

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax}$ )	4	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50 \text{ V}$ )	360	mJ

## 2 Electrical characteristics

$T_C = 25^\circ\text{C}$  unless otherwise specified

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}$	600			V
$I_{\text{DSS}}$	Zero gate voltage drain current	$V_{GS} = 0 \text{ V}, V_{DS} = 600 \text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0 \text{ V}, V_{DS} = 600 \text{ V}, T_C = 125^\circ\text{C}$ <sup>(1)</sup>			100	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 25 \text{ V}$			$\pm 5$	$\mu\text{A}$
$V_{GS(\text{th})}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	3.25	4	4.75	V
$R_{\text{DS(on)}}$	Static drain-source on-resistance	$V_{GS} = 10 \text{ V}, I_D = 9 \text{ A}$		165	195	$\text{m}\Omega$

1. Defined by design, not subject to production test.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100 \text{ V}, f = 1 \text{ MHz}, V_{GS} = 0 \text{ V}$	-	940	-	pF
$C_{oss}$	Output capacitance		-	75	-	pF
$C_{rss}$	Reverse transfer capacitance		-	4	-	pF
$C_{oss \text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0 \text{ to } 480 \text{ V}, V_{GS} = 0 \text{ V}$	-	157	-	pF
$R_G$	Intrinsic gate resistance	$f = 1 \text{ MHz}, I_D = 0 \text{ A}$	-	4.8	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 480 \text{ V}, I_D = 18 \text{ A}, V_{GS} = 0 \text{ to } 10 \text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	24	-	nC
$Q_{gs}$	Gate-source charge		-	6	-	nC
$Q_{gd}$	Gate-drain charge		-	11.5	-	nC

1.  $C_{oss \text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

**Table 6. Switching times**

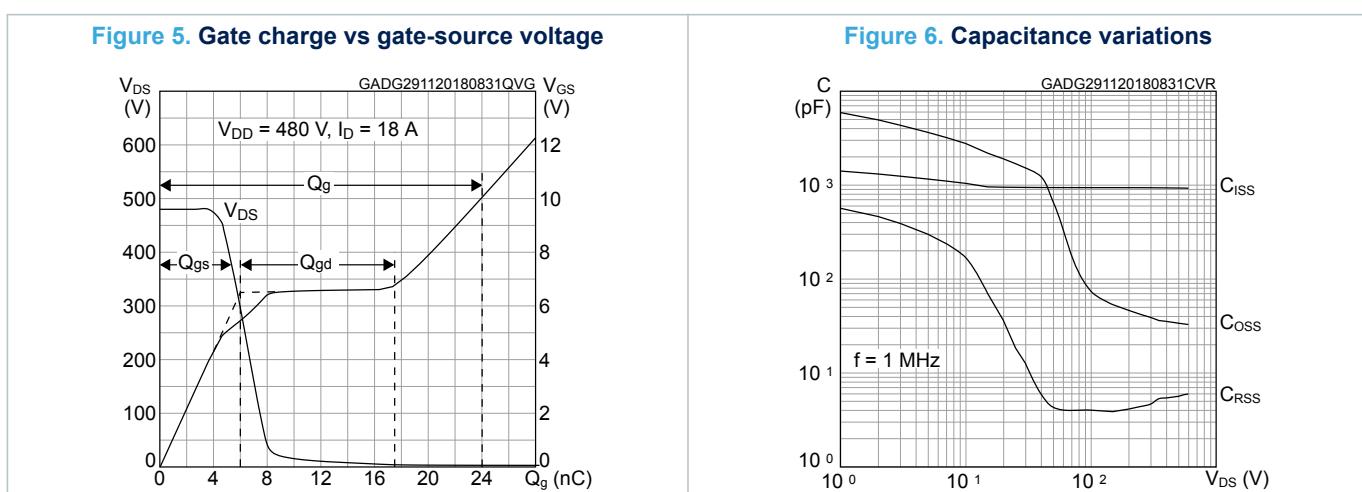
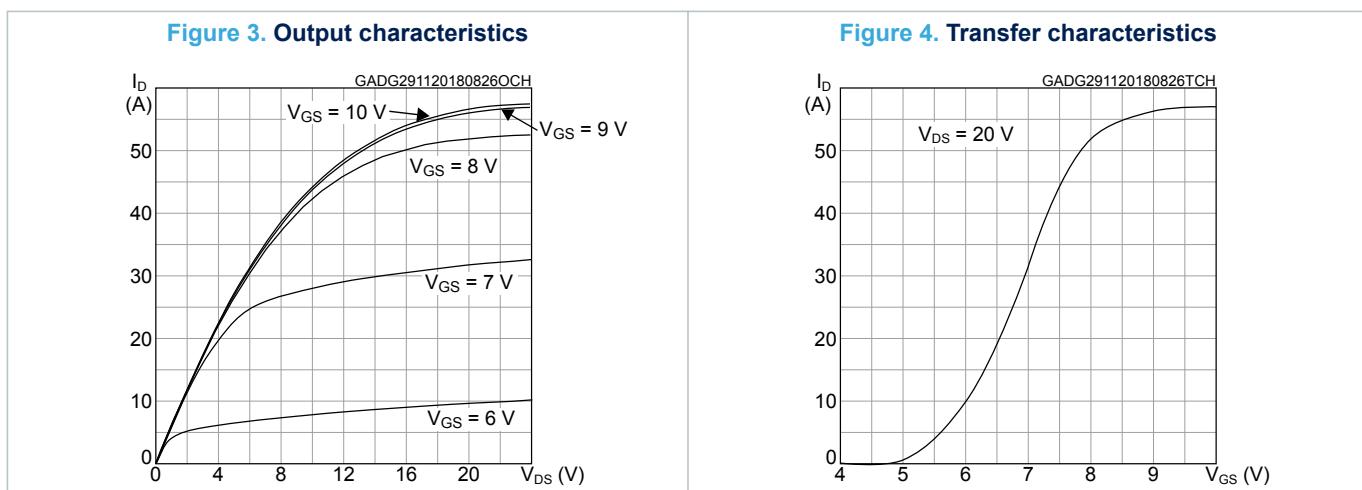
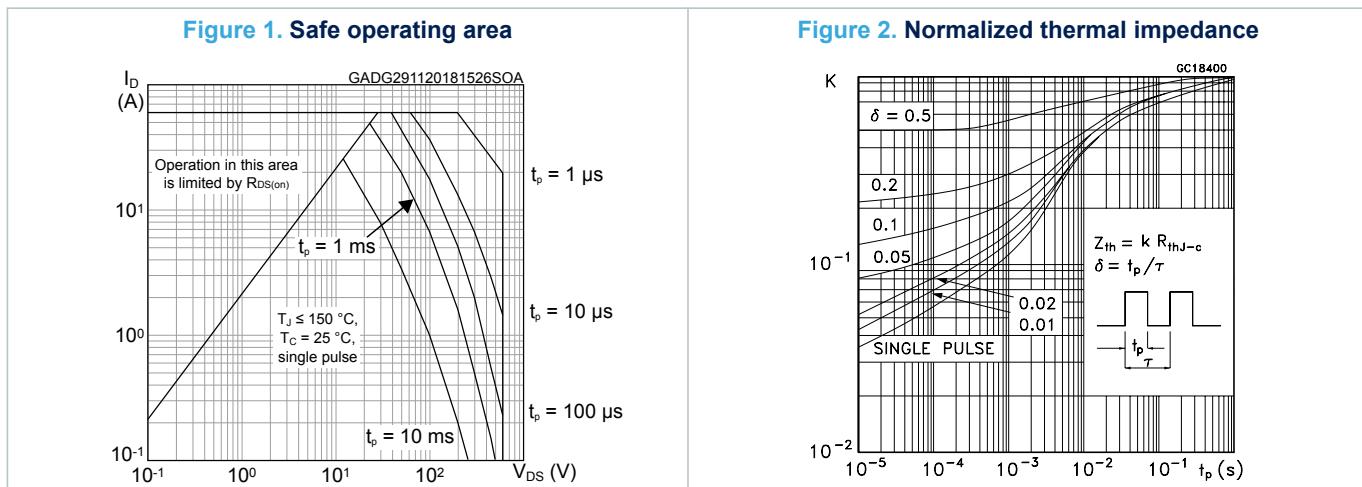
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(\text{on})}$	Turn-on delay time	$V_{DD} = 300 \text{ V}, I_D = 9 \text{ A}, R_G = 4.7 \Omega, V_{GS} = 10 \text{ V}$	-	13	-	ns
$t_r$	Rise time		-	11	-	ns
$t_{d(\text{off})}$	Turn-off delay time	(see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	39	-	ns
$t_f$	Fall time		-	8	-	ns

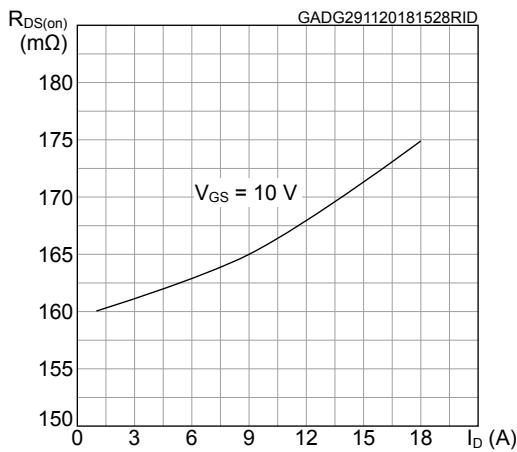
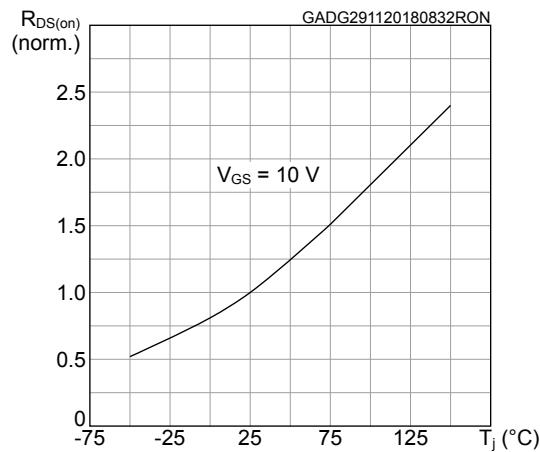
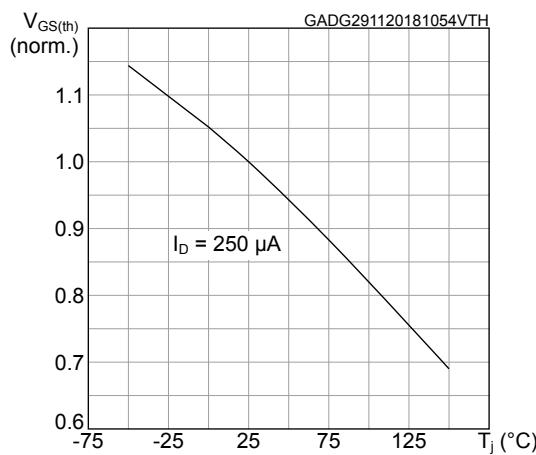
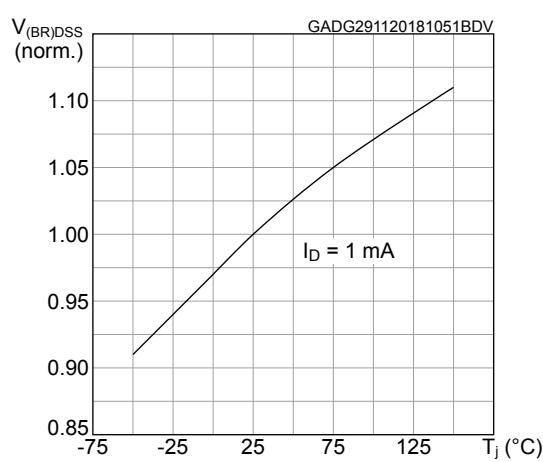
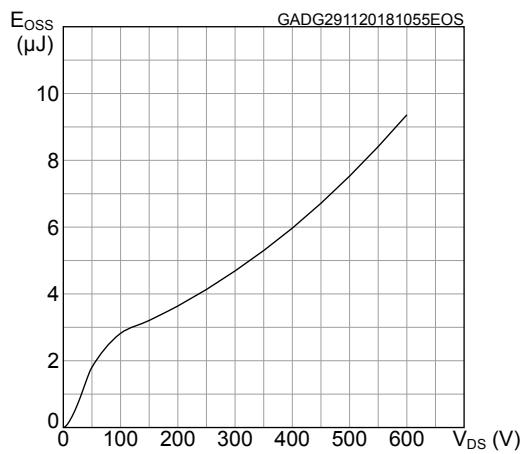
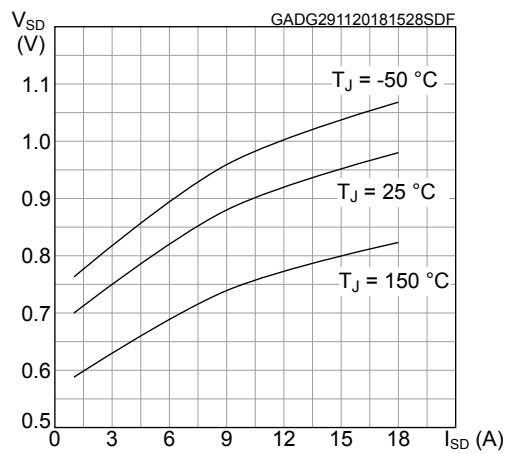
**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		18	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		60	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0 \text{ V}$ , $I_{SD} = 18 \text{ A}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 18 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ ,	-	100		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60 \text{ V}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	0.35		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	7		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 18 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ ,	-	170		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60 \text{ V}$ , $T_j = 150 \text{ }^\circ\text{C}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	1.02		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	12		A

1. Pulse width is limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %.

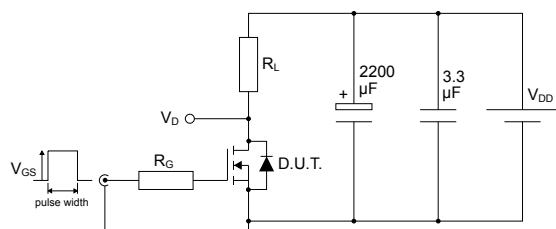
## 2.1 Electrical characteristics (curves)



**Figure 7. Static drain-source on-resistance**

**Figure 8. Normalized on-resistance vs temperature**

**Figure 9. Normalized gate threshold voltage vs temperature**

**Figure 10. Normalized  $V_{(BR)DSS}$  vs temperature**

**Figure 11. Output capacitance stored energy**

**Figure 12. Source-drain diode forward characteristics**


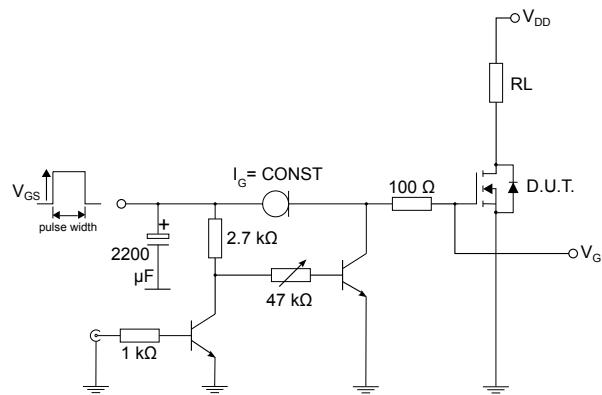
### 3 Test circuits

**Figure 13.** Test circuit for resistive load switching times



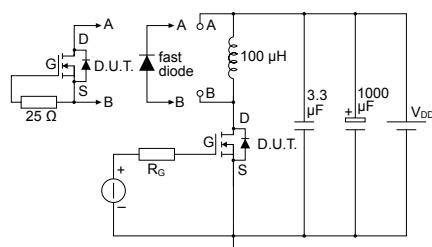
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**Figure 14.** Test circuit for gate charge behavior



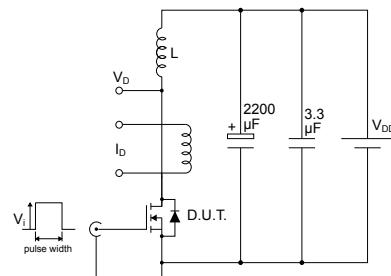
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**Figure 15.** Test circuit for inductive load switching and diode recovery times



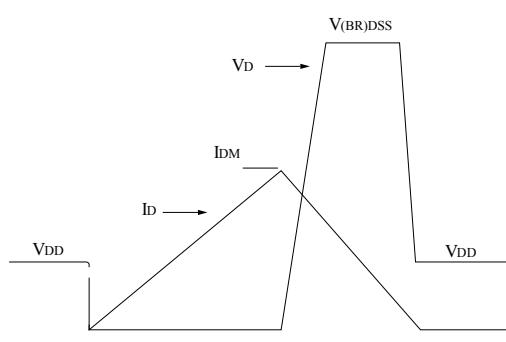
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**Figure 16.** Unclamped inductive load test circuit



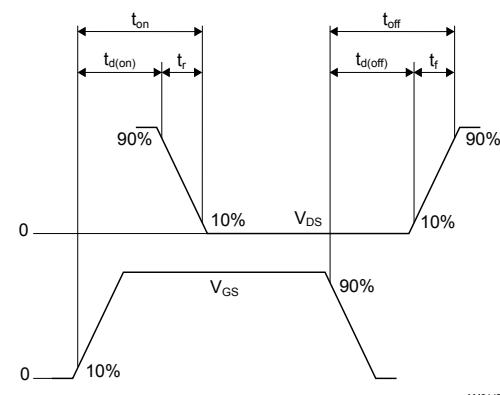
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**Figure 17.** Unclamped inductive waveform



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**Figure 18.** Switching time waveform



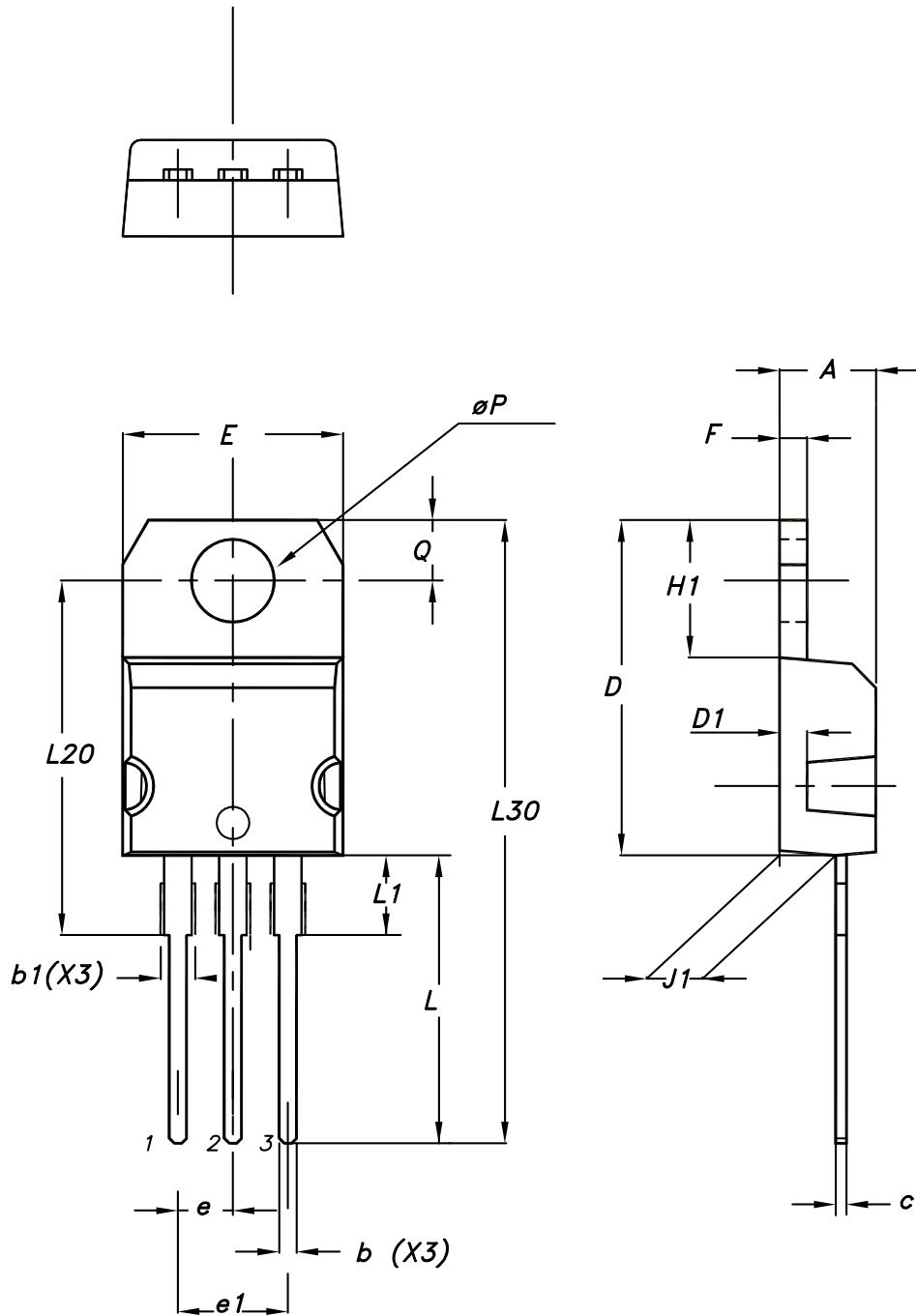
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## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 TO-220 type A package information

Figure 19. TO-220 type A package outline



0015988\_typeA\_Rev\_23

**Table 8. TO-220 type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

## Revision history

**Table 9. Document revision history**

Date	Version	Changes
06-Dec-2018	1	First release.
18-Mar-2020	2	Modified <a href="#">Table 2</a> . Thermal data and <a href="#">Table 4</a> . On/off states.
10-Sep-2020	3	Updated <a href="#">Table 1</a> .

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