STP30N10F7



N-channel 100 V, 0.02 Ω typ., 32 A STripFET™ F7 Power MOSFET in a TO-220 package

Datasheet - production data

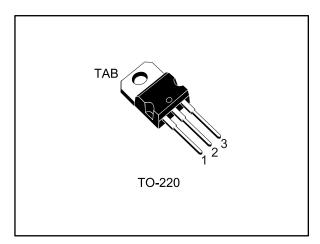
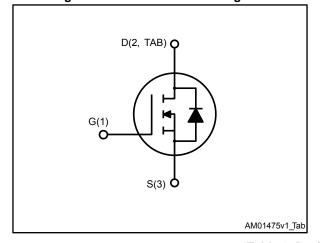


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STP30N10F7	100 V	0.024 Ω	32 A	50 W

- Among the lowest R_{DS(on)} on the market
- Excellent figure of merit (FOM)
- Low C_{rss} /C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low onstate resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

Order code	Marking	Package	Packing
STP30N10F7	30N10F7	TO-220	Tube

Contents STP30N10F7

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STP30N10F7 Electrical ratings

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit	
V_{DS}	Drain-source voltage	100	V	
V_{GS}	Gate source voltage	± 20	V	
I _D	Drain current (continuous) at T _C = 25 °C	32	Α	
I _D	Drain current (continuous) at T _C = 100 °C	23	Α	
I _{DM} ⁽¹⁾	Drain current (pulsed)	132	Α	
Ртот	Total dissipation at T _C = 25 °C 50		W	
TJ	Operating junction temperature range	55 to 175	°C	
T _{stg}	Storage temperature range -55 to 175			

Notes:

Table 3: Thermal data

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal resistance junction-case	3	°C/W
R _{thj-amb}	Thermal resistance junction-ambient	62.5	°C/W

 $^{^{(1)}\!\}text{Pulse}$ width limited by safe operating area.

Electrical characteristics STP30N10F7

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0 V, I _D = 250 μA	100			٧
	Zoro goto voltago drain	V _{GS} = 0 V, V _{DS} =100 V			1	μA
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0 V, V _{DS} =100 V,T _C = 125 °C			100	μΑ
I _{GSS}	Gate-body leakage current	V _{DS} = 0 V, V _{GS} = +20 V			100	nA
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2.5		4.5	V
R _{DS(on)}	Static drain-source on- resistance	V _{GS} = 10 V, I _D = 16 A		0.02	0.024	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions		Тур.	Max.	Unit
C _{iss}	Input capacitance		i	1270	ı	pF
Coss	Output capacitance	V _{DS} = 50 V, f = 1 MHz,V _{GS} = 0 V	ı	290	1	pF
C _{rss}	Reverse transfer capacitance	753 00 V, 1 111112, VGS 0 V	-	24	-	pF
Q_g	Total gate charge	V _{DD} = 50 V, I _D = 32 A,	-	19	-	nC
Q_{gs}	Gate-source charge	V _{GS} = 10 V	-	9	-	nC
Q _{gd}	Gate-drain charge	(see Figure 14: "Test circuit for gate charge behavior")	-	4.5	-	nC

Table 6: Switching times

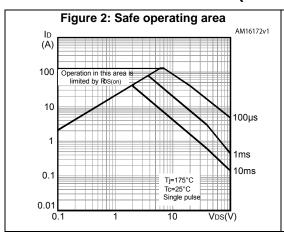
Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 50 V, I _D =16 A,	-	12	-	ns
t _r	Rise time	$R_{G} = 4.7 \Omega, V_{GS} = 10 V$	ı	17.5	ı	ns
t _{d(off)}	Turn-off delay time	(see Figure 13: "Test circuit for resistive load switching times")	1	22	1	ns
t _f	Fall time		-	5.6	-	ns

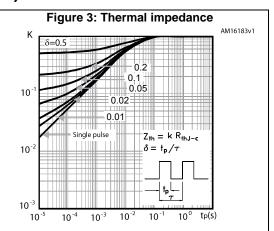
Table 7: Source-drain diode

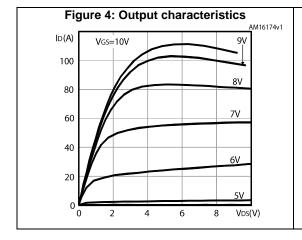
Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{SD} ⁽¹⁾	Forward on voltage	I _{SD} = 32 A, V _{GS} = 0 V	-		1.1	٧
t _{rr}	Reverse recovery time		1	41		ns
Qrr	Reverse recovery charge	I _{SD} = 32 A, di/dt = 100 A/µs V _{DD} = 80 V, T _J = 150 °C, Figure 15: "Test circuit for inductive load switching and	ı	47		nC
I _{RRM}	Reverse recovery current	diode recovery times"	ı	2.3		Α

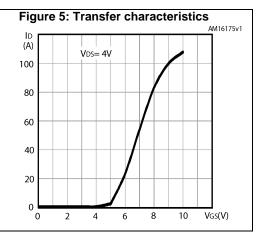
Notes:

2.1 Electrical characteristics (curves)









 $^{^{(1)}\}text{Pulsed:}$ pulse duration = 300 $\mu\text{s},$ duty cycle 1.5%.

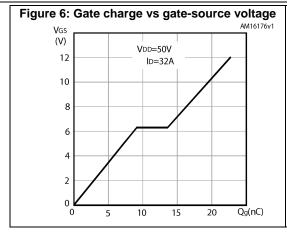


Figure 7: Static drain-source on-resistance

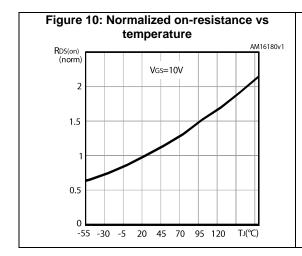
(mΩ)
21.50
21.00
20.50
20.00
19.50
19.00
18.50
18.00
0 10 20 30 ID(A)

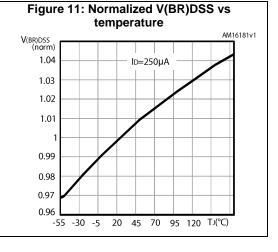
Figure 8: Capacitance variations

(pF)
1400
1200
1000
800
400
200
0 10 20 30 40 50 60 70 80 Vbs(V)

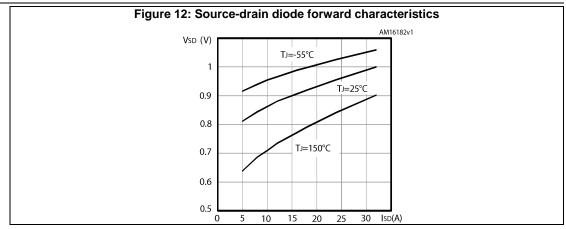
Figure 9: Normalized gate threshold voltage vs temperature

VGS(th) (norm)
1.2
1
0.8
0.6
0.4
0.2
0
-55 -30 -5 20 45 70 95 120 145 TJ(℃)





essaggio



Test circuits STP30N10F7

3 Test circuits

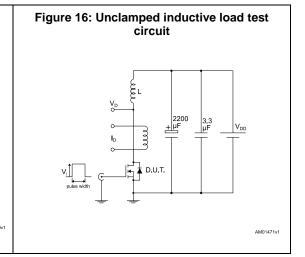
Figure 13: Test circuit for resistive load switching times

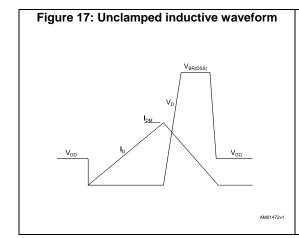
Figure 14: Test circuit for gate charge behavior

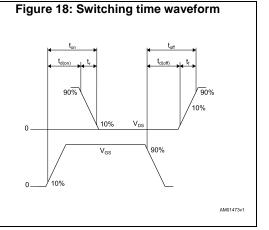
12 V 47 KΩ 100 N D.U.T.

Vos 1 1 KΩ 100 N D.U.T.

AM01489v1







STP30N10F7 Package information

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.

4.1 TO-220 type A package information

Figure 19: TO-220 type A package outline

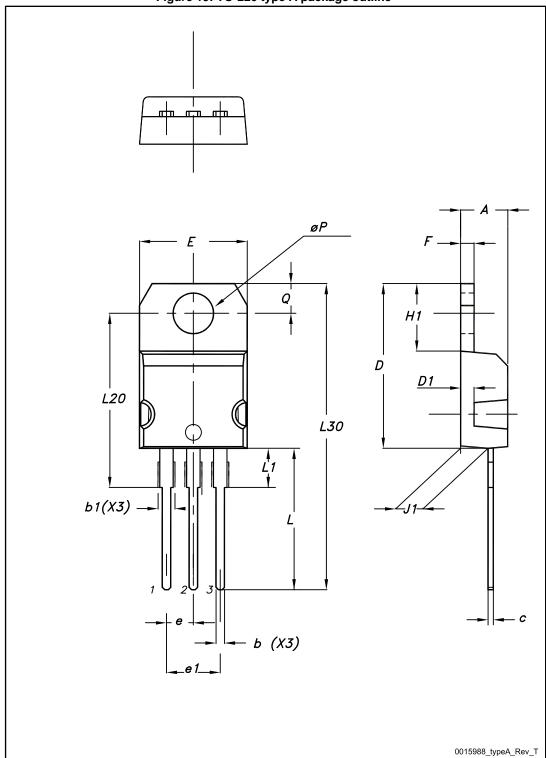


Table 8: TO-220 type A mechanical data

Dim	mm		
Dim.	Min.	Тур.	Max.
А	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
С	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
е	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
øΡ	3.75		3.85
Q	2.65		2.95

Revision history STP30N10F7

5 Revision history

Table 9: Document revision history

Date	Revision	Changes
01-Feb-2016	1	First release.

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