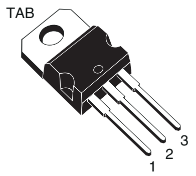
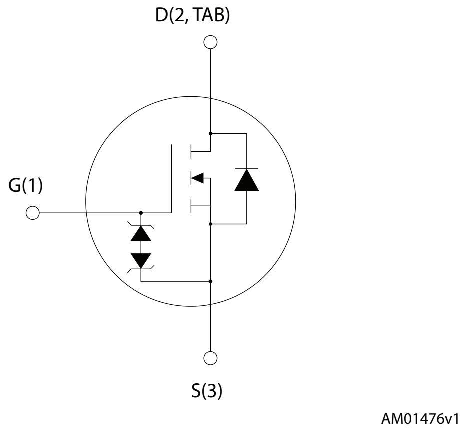
N-channel 500 V, 2.8 Ω typ., 2.3 A Zener-protected SuperMESH™ Power MOSFET in a TO-220 package

Datasheet - production data



TO-220

Figure 1. Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)max.}$	I_D	P_{TOT}
STP3NK50Z	500 V	3.3 Ω	2.3 A	45 W

- Extremely high dv/dt capability
- ESD improved capability
- 100% avalanche tested
- Gate charge minimized
- Zener-protected

Applications

- Switching applications

Description

This device is an N-channel Zener-protected Power MOSFET developed using STMicroelectronics' SuperMESH™ technology, achieved through optimization of ST's well established strip-based PowerMESH™ layout. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

Table 1. Device summary

Order code	Marking	Packages	Packaging
STP3NK50Z	P3NK50Z	TO-220	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	500	V
V_{DGR}	Drain-gate voltage (R_{GS}=20 kΩ)	500	V
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at T_C = 25 °C	2.3	A
I_D	Drain current (continuous) at T_C = 100 °C	1.45	A
I_{DM} (1)	Drain current (pulsed)	9.2	A
P_{TOT}	Total dissipation at T_C = 25 °C	45	W
	Derating factor	0.36	W/°C
ESD	Gate-source human body model (C = 100 pF, R = 1.5 kΩ)	2	kV
dv/dt (2)	Peak diode recovery voltage slope	4.5	V/ns
T_{stg}	Storage temperature	-55 to 150	°C
T_j	Operating junction temperature		°C

1. Pulse width limited by safe operating area.
2. $I_D \leq 2$ A, di/dt ≤ 200 A/µs, $V_{DD} \leq V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	2.78	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	°C/W

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Max current during repetitive or single pulse avalanche (pulse width limited by T_{jmax})	2.3	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D=I_{AS}, V_{DD}= 50 V)	120	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified).

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage (V_{GS}= 0)	I_D = 1 mA	500			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 500 V V_{DS} = 500 V, Tc=125 °C			1 50	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			±10	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 50 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D= 1.15 A		2.8	3.3	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g^{(1)}$	Forward transconductance	V_{DS} =15 V, I_D=1.15 A	-	1.5		S
C_{iss}	Input capacitance	V_{DS} =25 V, f=1 MHz, V_{GS}=0	-	280		pF
C_{oss}	Output capacitance		-	42		pF
C_{rss}	Reverse transfer capacitance		-	8		pF
$C_{oss\ eq.}^{(2)}$	Equivalent capacitance time related	V_{GS} = 0, V_{DS} = 0 to 400 V	-	27.5		pF
$t_{d(on)}$	Turn-on delay time	V_{DD} = 250 V, I_D = 1.15 A, R_G=4.7 Ω, V_{GS}=10 V *(see Figure 19 and 15)*	-	8		ns
t_r	Rise time		-	13		ns
$t_{d(off)}$	Turn-off delay time		-	24		ns
t_f	Fall time		-	14		ns
Q_g	Total gate charge	V_{DD} = 400 V, I_D = 2.3 A V_{GS} =10 V *(see Figure 16)*	-	11	15	nC
Q_{gs}	Gate-source charge		-	2.5		nC
Q_{gd}	Gate-drain charge		-	5.6		nC

1. Pulsed: Pulse duration = 300 ìs, duty cycle 1.5 %.
2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		2.3	A
I_{SDM} [(1)]	Source-drain current (pulsed)		-		9.2	A
V_{SD} [(2)]	Forward on voltage	I_{SD}= 2.3 A, V_{GS}=0	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD}= 2.3 A, V_{DD}= 40 V di/dt = 100 A/µs, *(see Figure 17)*	-	250		ns
Q_{rr}	Reverse recovery charge		-	745		nC
I_{RRM}	Reverse recovery current		-	6		A
t_{rr}	Reverse recovery time	I_{SD}= 12 A,V_{DD}= 40 V di/dt=100 A/µs, T_j=150 °C *(see Figure 17)*	-	300		ns
Q_{rr}	Reverse recovery charge		-	960		nC
I_{RRM}	Reverse recovery current		-	6.2		A

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%
2. Pulse width limited by safe operating area

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS} = ± 1mA, I_D=0	30	-	-	V

The built-in back-to-back Zener diodes have been specifically designed to enhance not only the device's ESD capability, but also to make them capable of safely absorbing any voltage transients that may occasionally be applied from gate to source. In this respect, the Zener voltage is appropriate to achieve efficient and cost-effective protection of device integrity. The integrated Zener diodes thus eliminate the need for external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

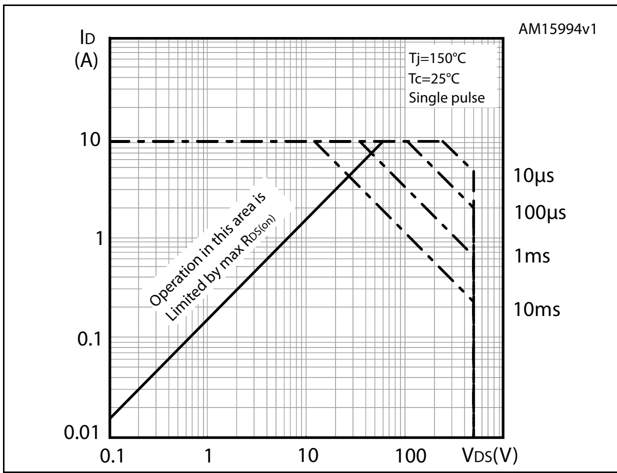


Figure 3. Thermal impedance

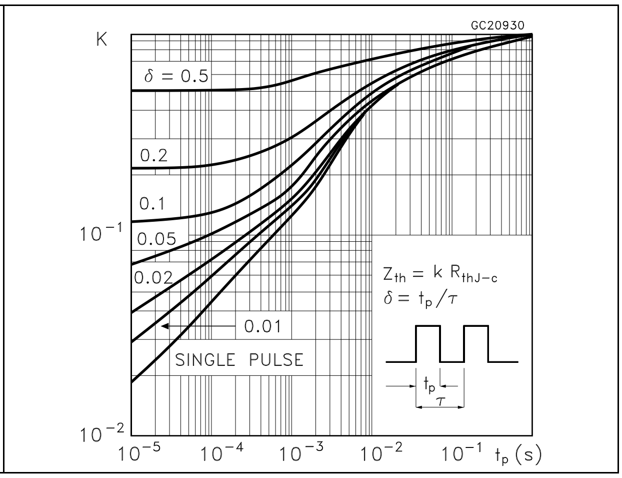


Figure 4. Output characteristics

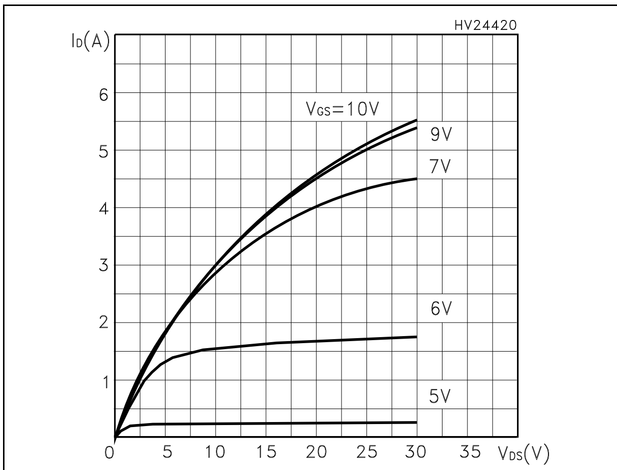


Figure 5. Transfer characteristics

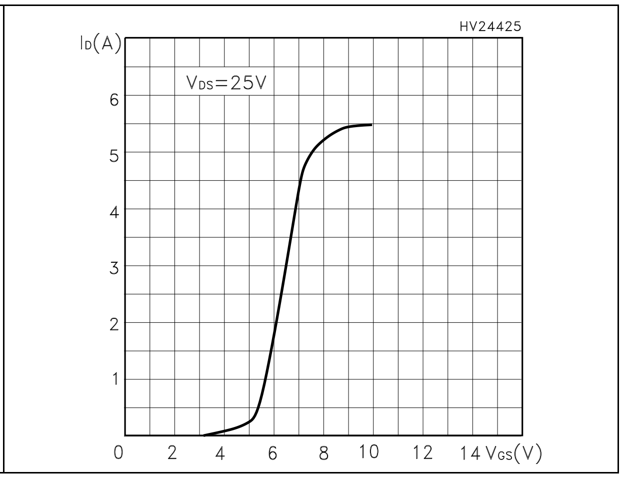


Figure 6. Transconductance

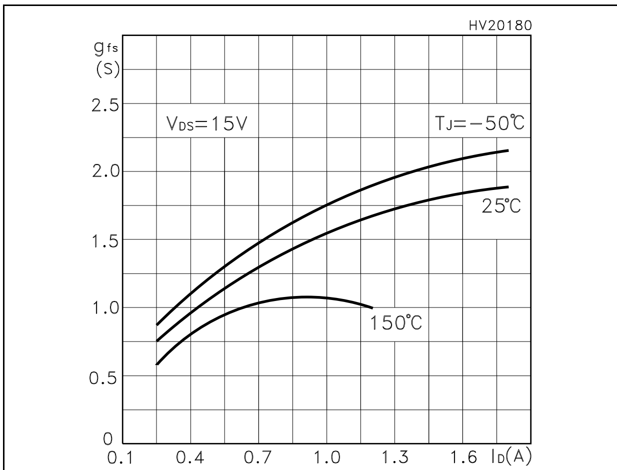


Figure 7. Capacitance variations

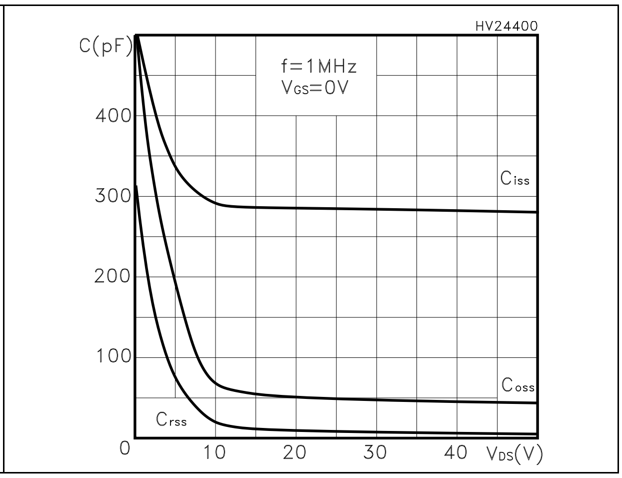


Figure 8. Gate charge vs gate-source voltage

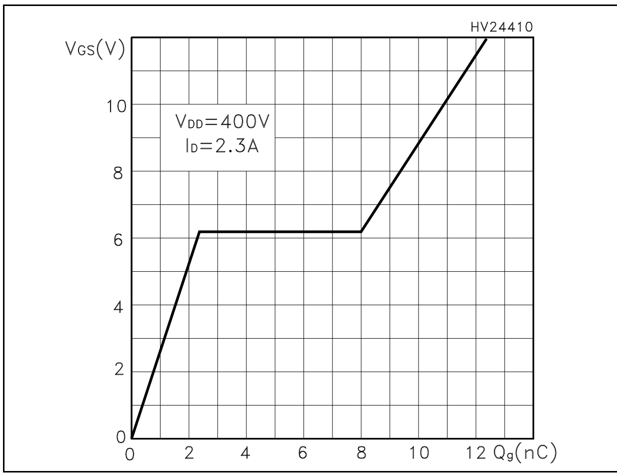


Figure 9. Normalized gate threshold voltage vs temperature

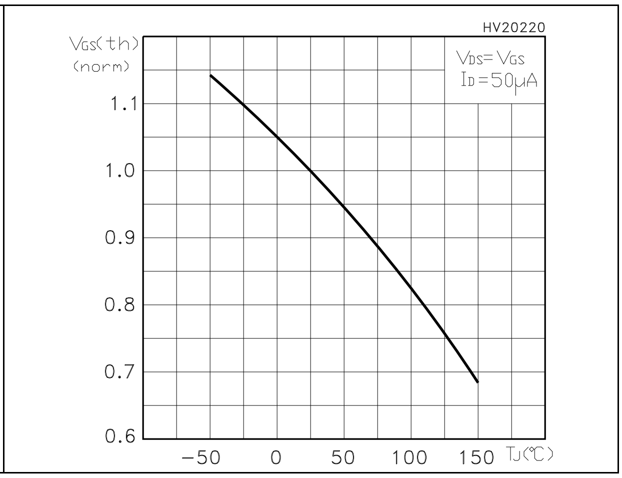


Figure 10. Static drain-source on-resistance

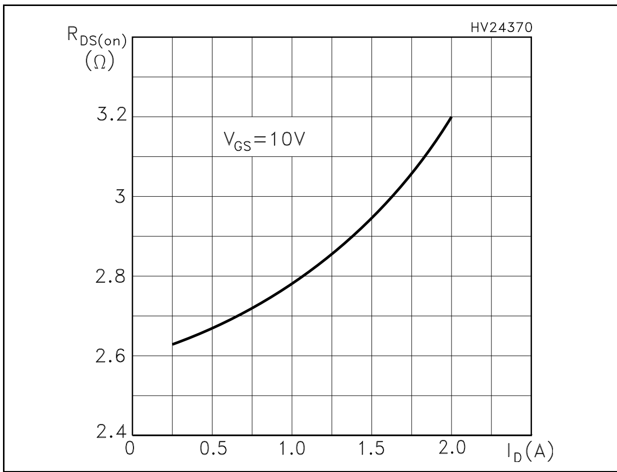


Figure 11. Source-drain forward characteristics

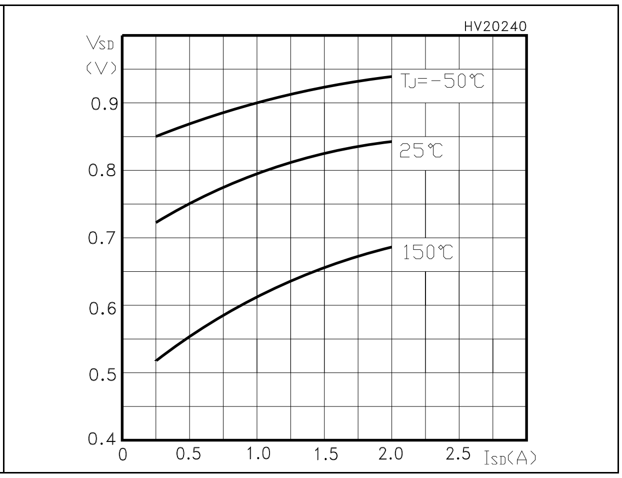


Figure 12. Maximum avalanche energy vs temperature

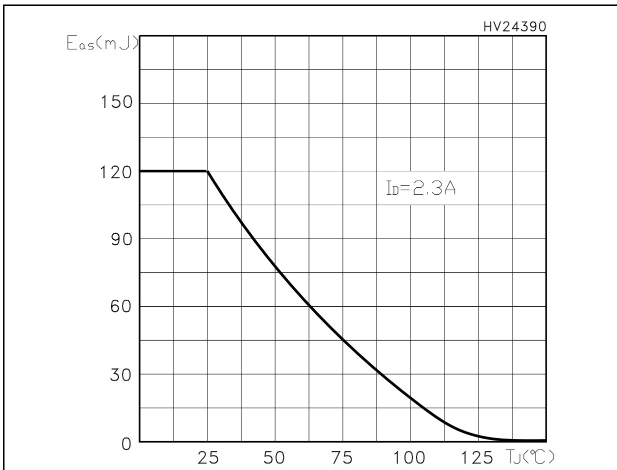


Figure 13. Normalized BV_{DSS} vs temperature

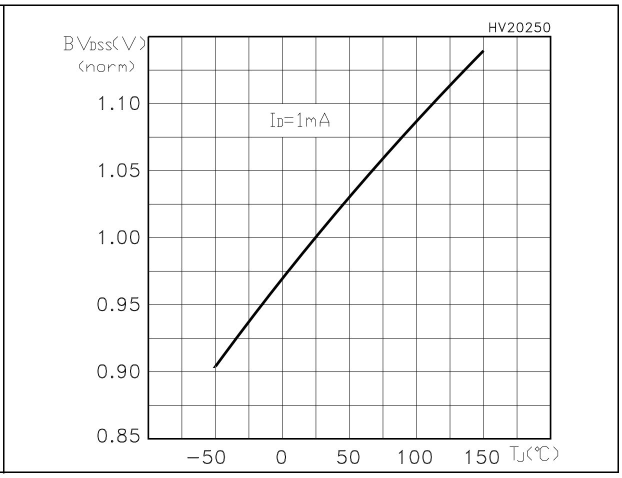
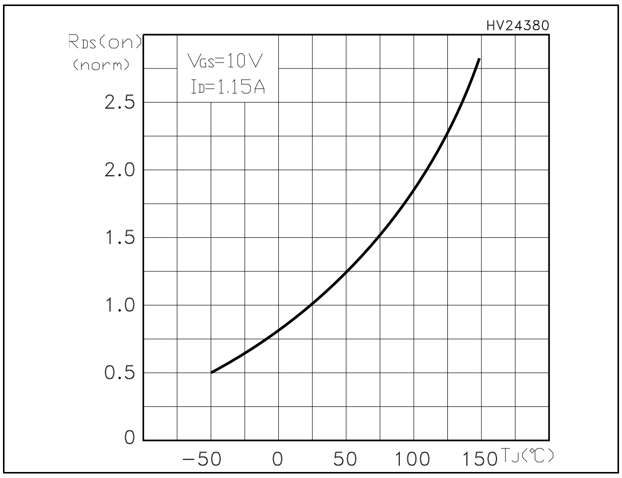


Figure 14. Normalized on-resistance vs temperature



3 Test circuits

Figure 15. Switching times test circuit for resistive load

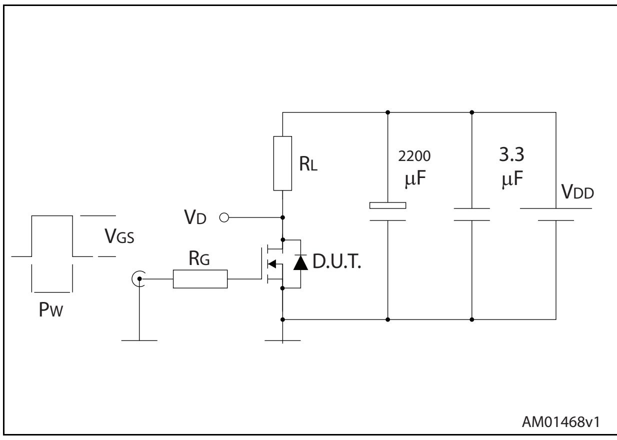


Figure 16. Gate charge test circuit

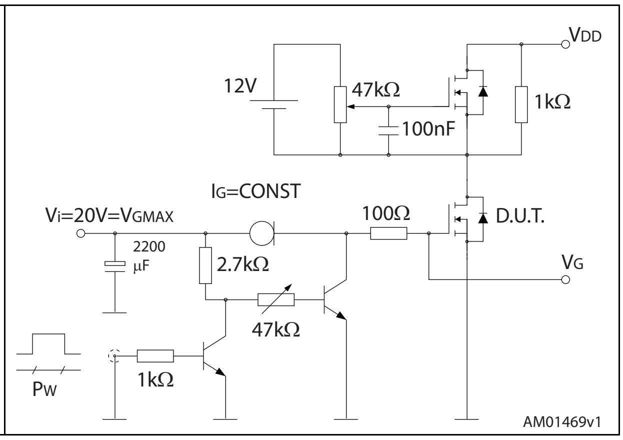


Figure 17. Test circuit for inductive load switching and diode recovery times

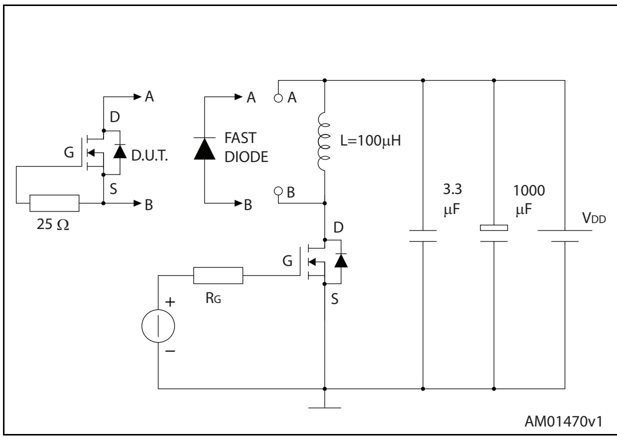


Figure 18. Unclamped inductive load test circuit

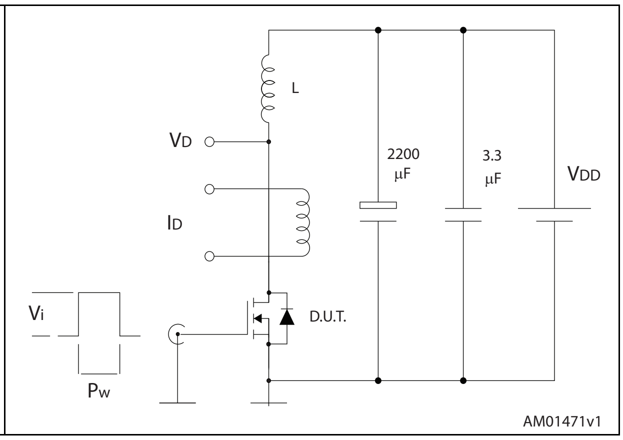


Figure 19. Unclamped inductive waveform

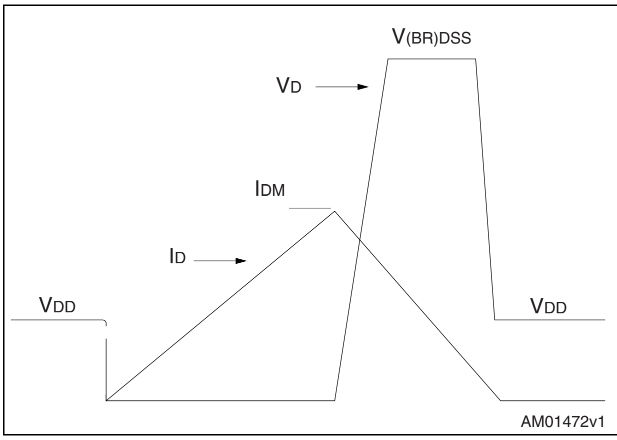
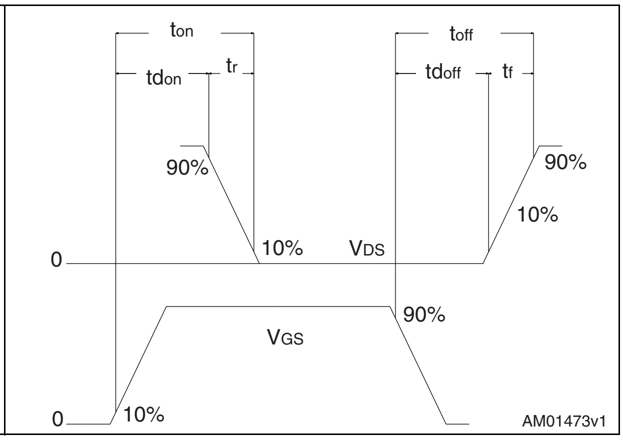


Figure 20. Switching time waveform



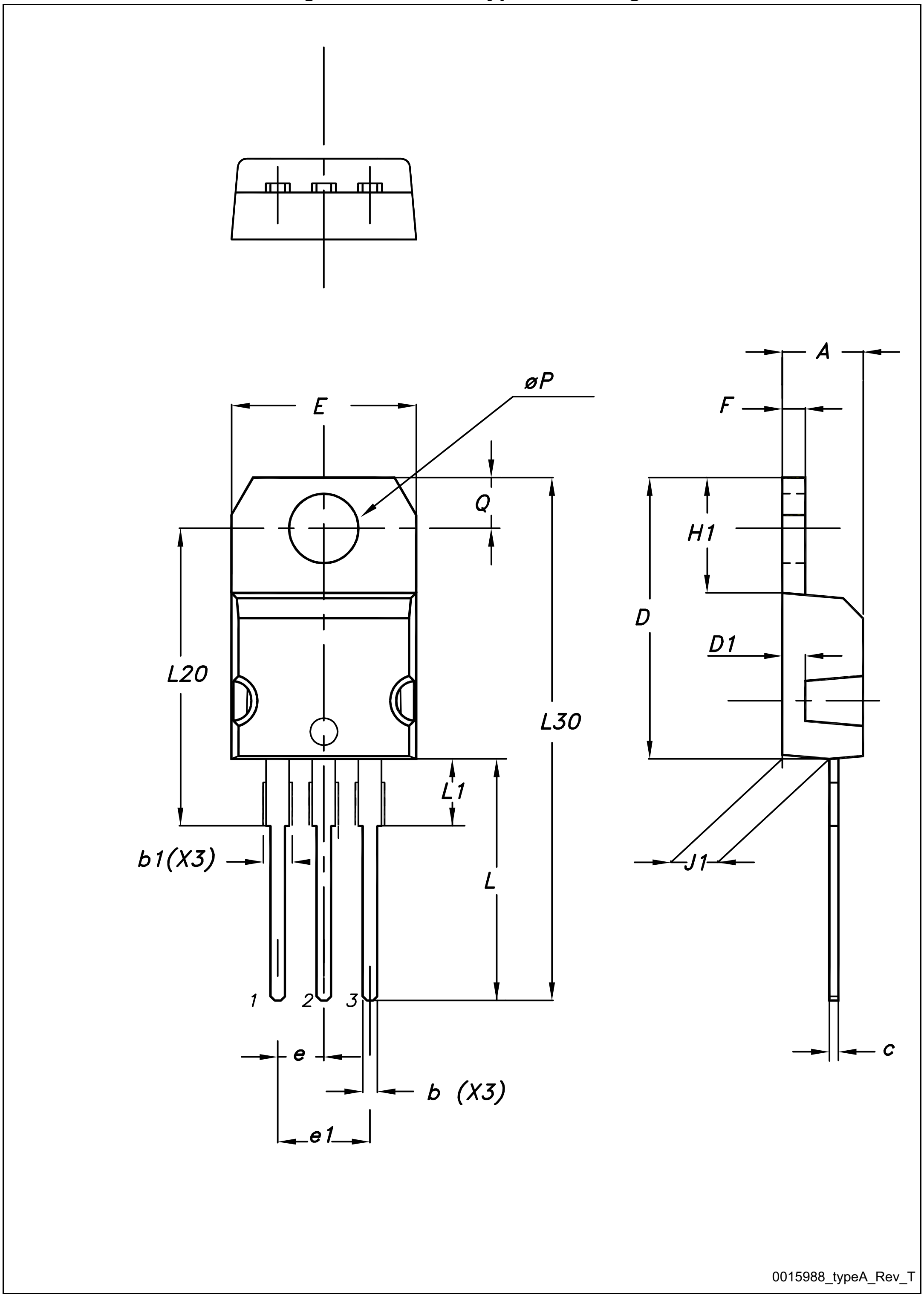
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Table 9. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
∅P	3.75		3.85
Q	2.65		2.95

Figure 21. TO-220 type A drawing



5 Revision history

Table 10. Document revision history

Date	Revision	Changes
13-Aug-2013	1	First release.