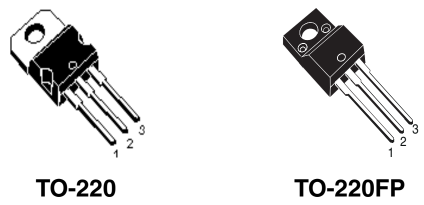
STP5NK80Z
STP5NK80ZFP

N-channel 800V - 1.9Ω - 4.3A - TO-220/TO-220FP Zener-protected SuperMESH™ Power MOSFET

General features

Type	V_{DSS} (@Tjmax)	$R_{DS(on)}$	I_D
STP5NK80Z	800 V	< 2.4 Ω	4.3 A
STP5NK80ZFP	800 V	< 2.4 Ω	4.3 A

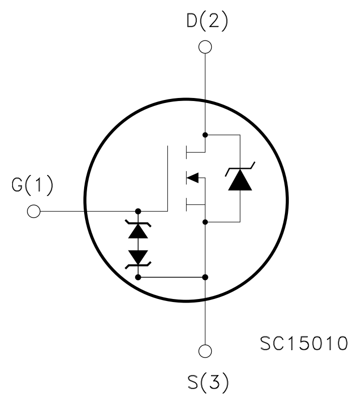
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatibility



Description

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

Internal schematic diagram



Applications

- Switching application

Order codes

Part number	Marking	Package	Packaging
STP5NK80Z	P5NK80Z	TO-220	Tube
STP5NK80ZFP	P5NK80ZFP	TO-220FP	Tube

Contents

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220	**TO-220FP**	
V_{DS}	Drain-source voltage (V_{GS} = 0)	800		V
V_{GS}	Gate-source voltage	± 30		V
I_D	Drain current (continuous) at T_C = 25°C	4.3	4.3 (1)	A
I_D	Drain current (continuous) at T_C=100°C	2.7	2.7 (1)	A
I_{DM}(2)	Drain current (pulsed)	17.2	17.2 (1)	A
P_{TOT}	Total dissipation at T_C = 25°C	110	30	W
	Derating factor	0.88	0.24	W/°C
$V_{ESD(G-S)}$	Gate source ESD (HBM-C=100pF, R=1.5KΩ)	3500		V
dv/dt (3)	Peak diode recovery voltage slope	4.5		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1s; T_c= 25°C)	-	2500	V
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150		°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 4.3A$, di/dt ≤200A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$.

Table 2. Thermal data

Symbol	Parameter	Value		Unit
		TO-220	**TO-220FP**	
$R_{thj-case}$	Thermal resistance junction-case max	1.14	4.2	°C/W
R_{thj-a}	Thermal resistance junction-ambient max	62.5		°C/W
T_l	Maximum lead temperature for soldering purpose	300		°C

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj Max)	4.3	A
E_{AS}	Single pulse avalanche energy (starting Tj=25°C, Id=Iar, Vdd=50V)	190	mJ

Table 4. Gate-source zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-source breakdown voltage	Igs=± 1mA (Open Drain)	30			V

1.1 Protection features of gate-to-source zener diodes

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1mA, V_{GS}= 0	800			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating, V_{DS} = Max rating, Tc = 125°C			1 50	µA µA
I_{GSS}	Gate body leakage current (V_{GS} = 0)	V_{GS} = ± 20V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10V, I_D = 2.15 A		1.9	2.4	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} =15V, I_D = 2.15A		4.25		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =25V, f=1 MHz, V_{GS}=0		910 98 20		pF pF pF
C_{osseq}(2).	Equivalent output capacitance	V_{GS}=0, V_{DS} =0V to 400V		40		pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_r	Turn-on delay time Rise time Turn-on delay time fall time	V_{DD}=400 V, I_D= 2 A, R_G=4.7Ω, V_{GS}=10V (see *Figure 18*)		18 25 45 30		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}=640V, I_D = 4.3A V_{GS} =10V		32.4 5 18.5	45.5	nC nC nC
$t_{d(Voff)}$ t_r	Off-voltage rise time Fall time Cross-over time	V_{DD}=640 V, I_D= 4.3 A, R_G=4.7Ω, V_{GS}=10V (see *Figure 20*)		22 10 32		ns ns ns

1. Pulsed: pulse duration=300µs, duty cycle 1.5%
2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				4.3 17.2	A A
V_{SD} (2)	Forward on voltage	I_{SD}= 4.3 A, V_{GS}=0			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}= 4.3 A, di/dt = 100A/µs, V_{DD}=40 V, Tj = 150°C (see *Figure 20*)		500 3 12		ns µC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for TO-220

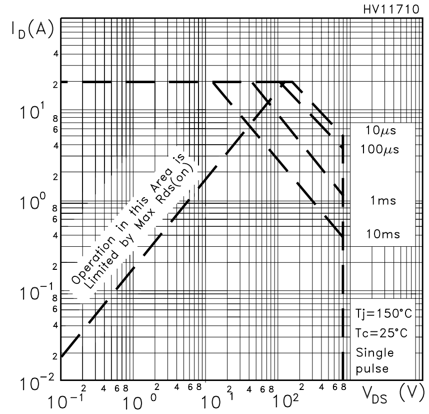


Figure 2. Thermal impedance for TO-220

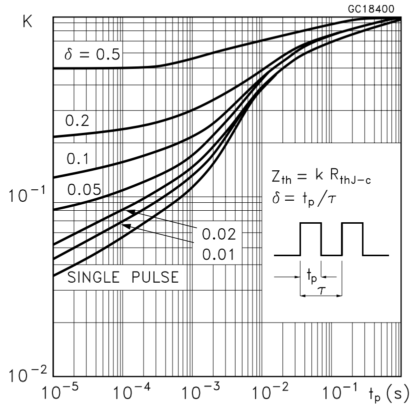


Figure 3. Safe operating area for TO-220FP (HV11720)

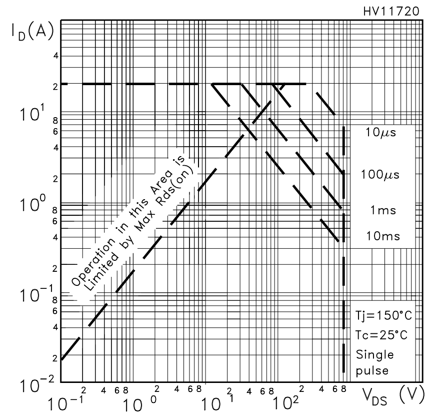


Figure 4. Thermal impedance for TO-220FP

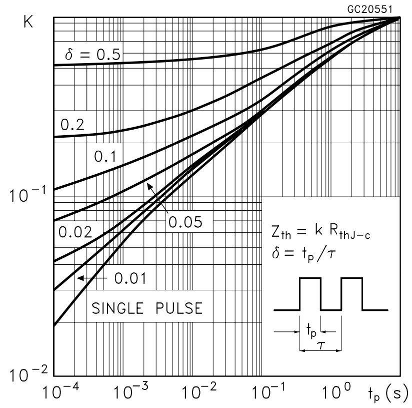


Figure 5. Output characterisics

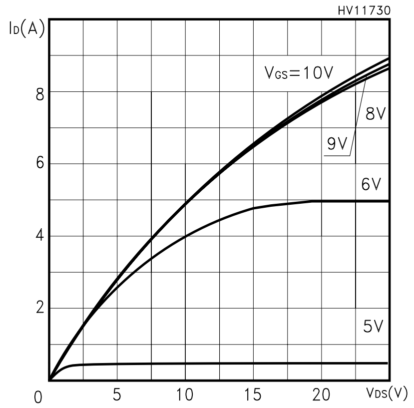


Figure 6. Transfer characteristics

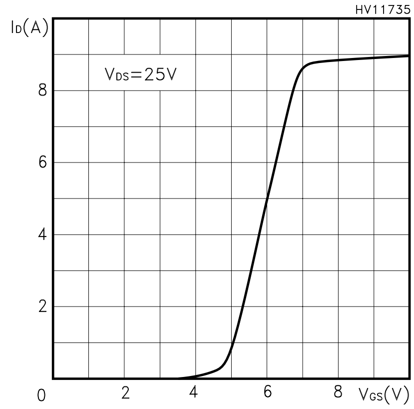


Figure 7. Transconductance

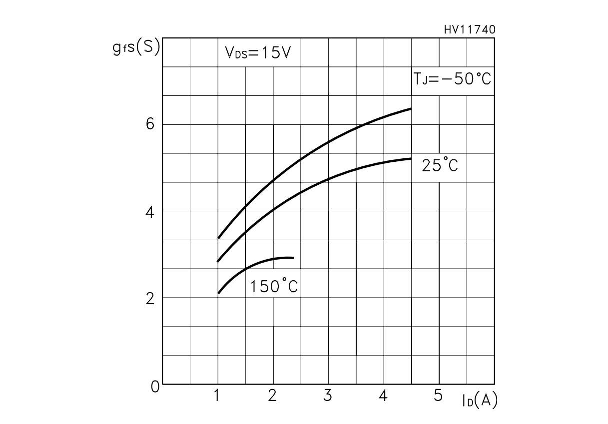


Figure 8. Static drain-source on resistance

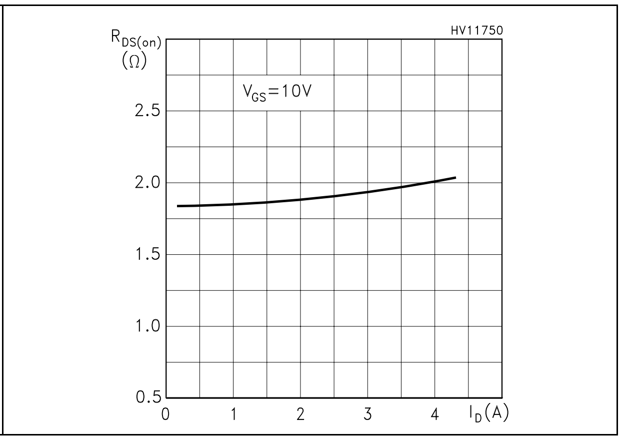


Figure 9. Gate charge vs gate-source voltage

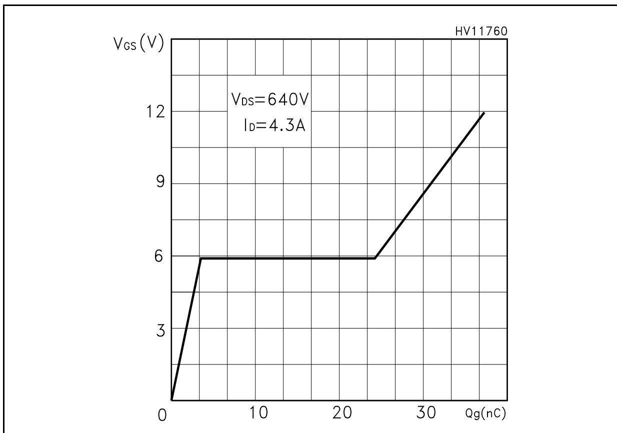


Figure 10. Capacitance variations

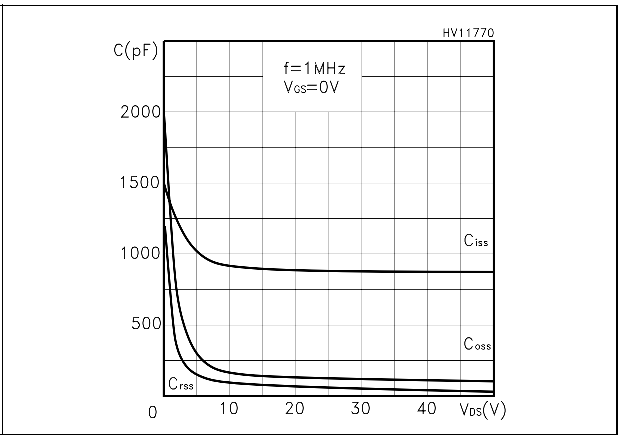


Figure 11. Normalized gate threshold voltage vs temperature

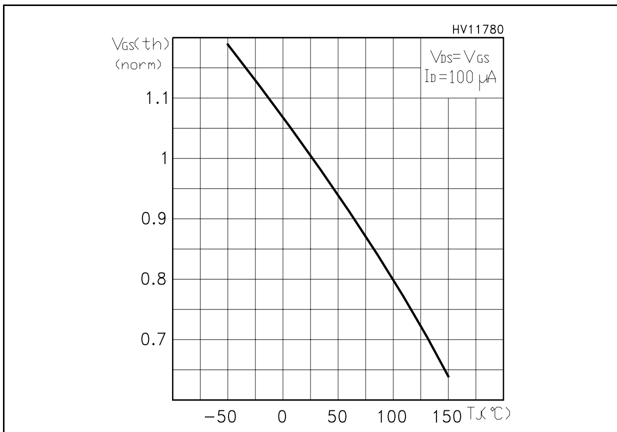


Figure 12. Normalized on resistance vs temperature

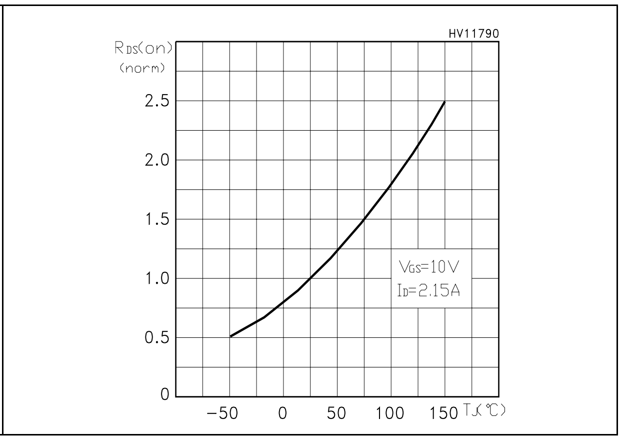


Figure 13. Source-drain diode forward characteristics

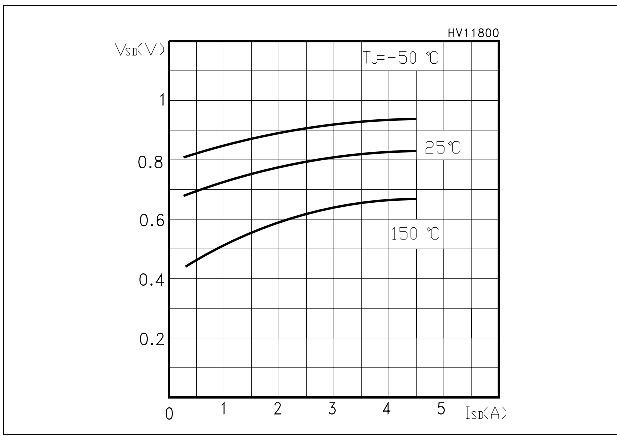


Figure 14. Normalized BVdss vs temperature

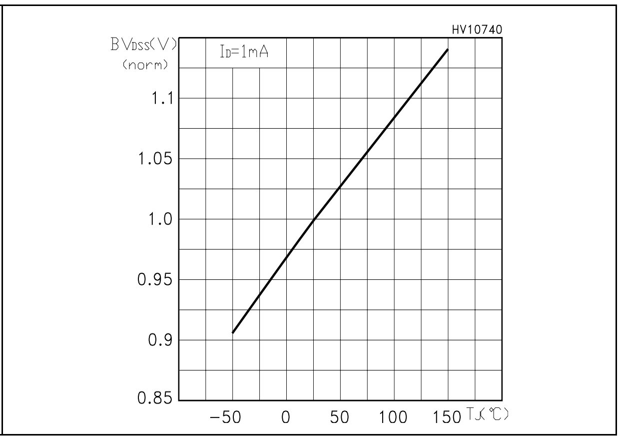
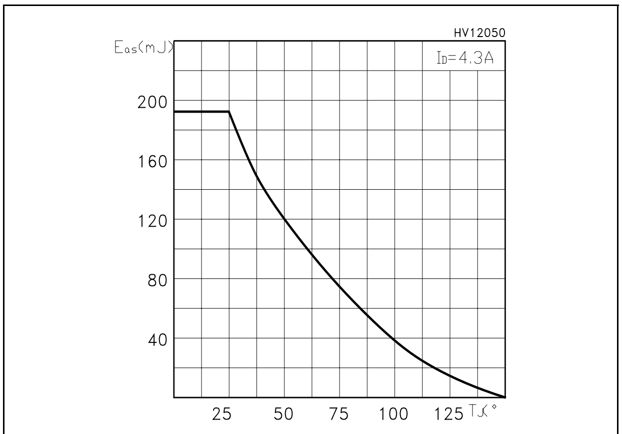


Figure 15. Avalanche energy vs temperature



3 Test circuit

Figure 16. Unclamped Inductive load test circuit

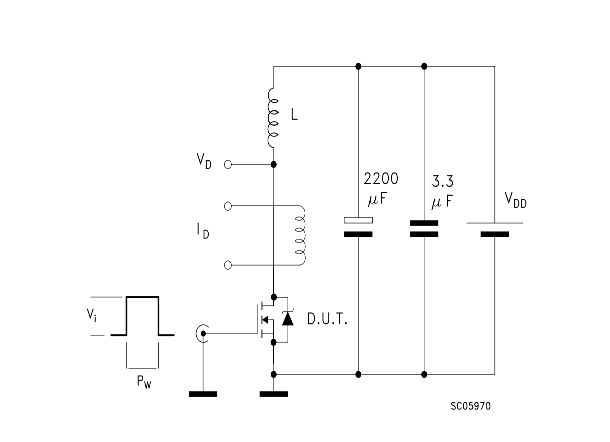


Figure 17. Unclamped Inductive waveform

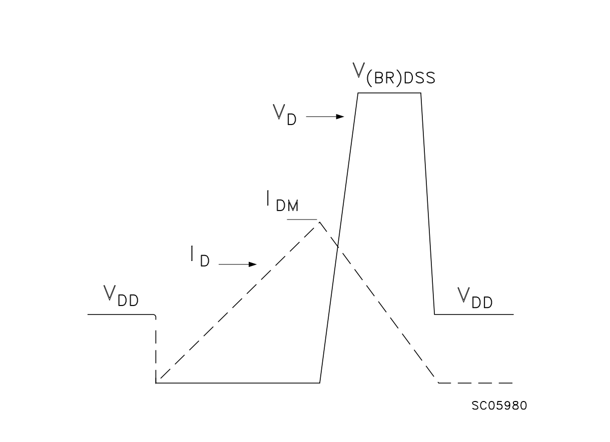


Figure 18. Switching times test circuit for resistive load

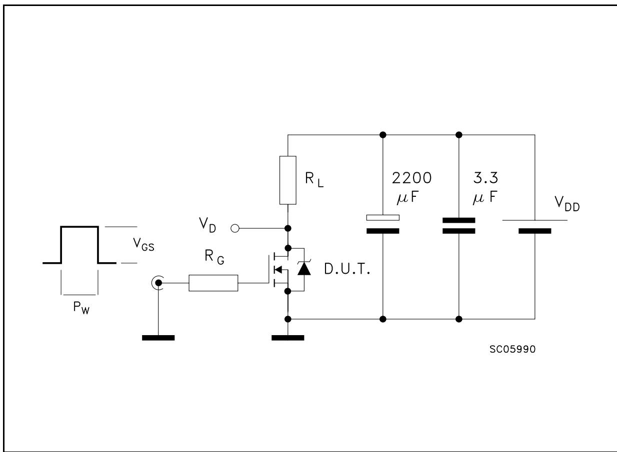


Figure 19. Gate charge test circuit

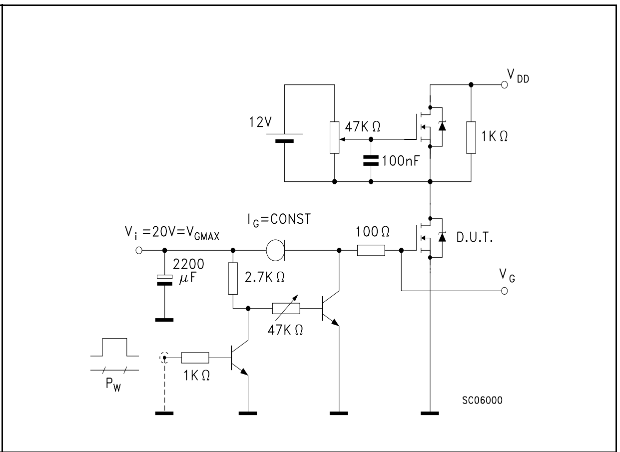
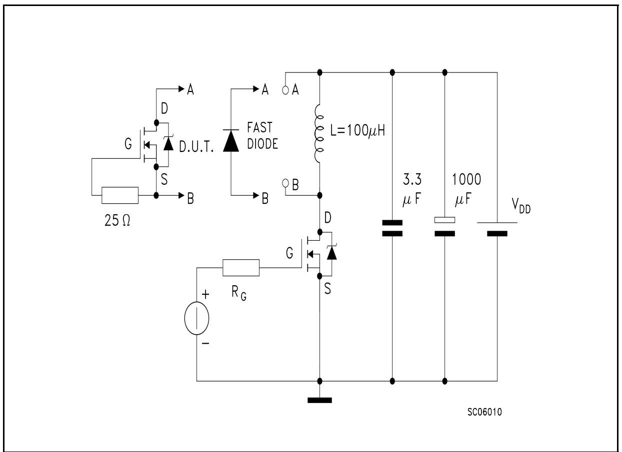


Figure 20. Test circuit for inductive load switching and diode recovery times

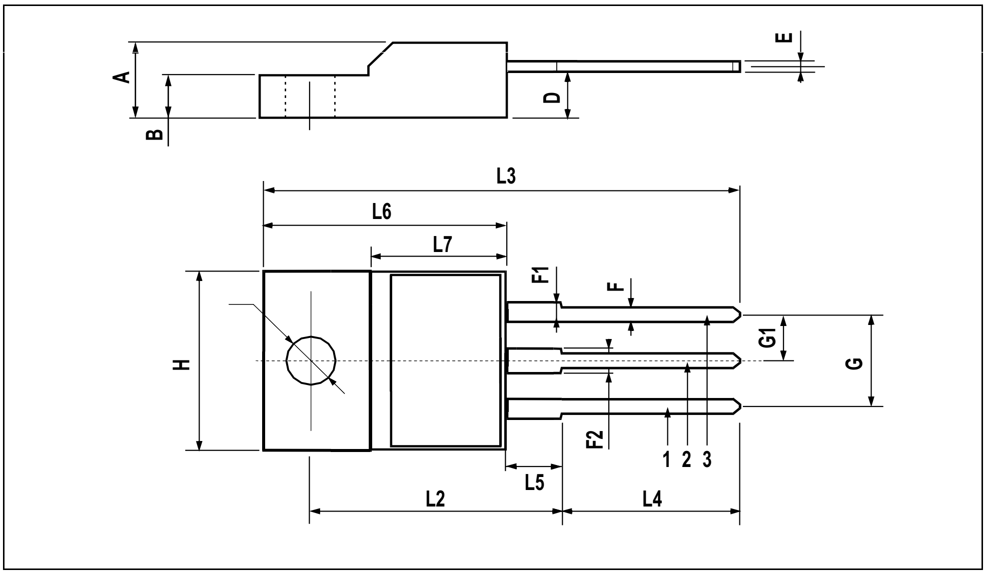


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

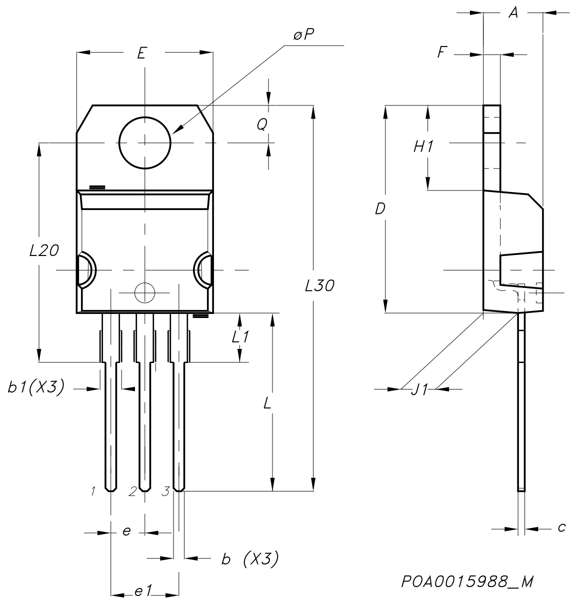
TO-220FP MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



5 Revision history

Table 8. Revision history

Date	Revision	Changes
09-Sep-2004	2	Preliminary version
06-Sep-2005	3	Final version
16-Aug-2006	4	New template, no content change