

STP60NF06FP

General features

Туре	V _{DSS}	R _{DS(on)}	I _D
STP60NF06FP	60V	<0.016Ω	30A

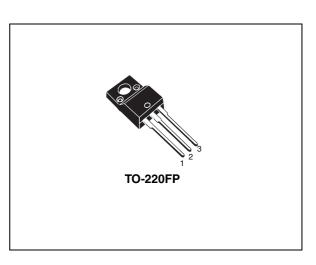
- Exceptional dv/dt capability
- 100% avalanche tested
- Application oriented characterization

Description

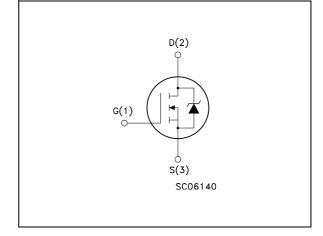
This Power MOSFET series realized with STMicroelectronics unique STripFET process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced highefficiency isolated DC-DC converters for Telecom and Computer application. It is also intended for any application with low gate charge drive requirements.

Applications

Switching application



Internal schematic diagram



Order code

Part number	Marking	Package	Packaging
STP60NF06FP	P60NF06	TO-220FP	Tube

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1 Electrical ratings

Table 1.	Absolute	maximum	ratings
	Abounde	maximum	ruungo

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source voltage (V _{GS} = 0)	60	V
V _{GS}	Gate- source voltage	±20	V
I _D	Drain current (continuos) at T _C = 25°C	30	Α
I _D	Drain current (continuos) at T _C = 100°C	21	Α
I _{DM} ⁽¹⁾	Drain current (pulsed)	120	Α
P _{TOT}	Total dissipation at $T_{C} = 25^{\circ}C$	30	W
	Derating factor	0.2	W/°C
dv/dt ⁽²⁾	Peak diode recovery voltage slope	4	V/ns
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1s; Tc= 25°C)	2500	V
T _{stg}	Storage temperature	- 55 to 175	٦°
Тj	Max. operating junction temperature	- 55 10 175	

1. Pulse width limited by safe operating area

2. $I_{SD} \leq 60A$, di/dt $\leq 400 A/\mu s$, $V_{DD} \leq 24V$, $Tj \leq T_{jmax}$

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal resistance junction-case max	5	°C/W
R _{thj-a}	Thermal resistance junction-ambient max	62.5	°C/W
Τ _Ι	Maximum lead temperature for soldering purpose	300	°C

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj Max)	30	А
E _{AS}	Single pulse avalanche energy (starting Tj=25°C, Id=Ias, Vdd=30V)	370	mJ



2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

	On/on States					
Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown voltage	I _D = 250 μA, V _{GS} = 0	60			V
1	Zero gate voltage	V _{DS} = Max rating			1	μA
I _{DSS} Drain	Drain current ($V_{GS} = 0$)	V_{DS} =Max rating, T _C =125°C			10	μA
I _{GSS}	Gate-body leakage current (V _{DS} = 0)	$V_{GS} = \pm 20V$			±100	nA
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	2		4	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10V, I _D = 30A		0.014	0.016	Ω

Table 4. On/off states

Table 5. Dynamic

	2 y name					
Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
9 _{fs} ⁽¹⁾	Forward transconductance	V _{DS} = 15V _, I _D =30A		50		S
C _{iss}	Input capacitance			1810		pF
C _{oss}	Output capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		360		pF
C _{rss}	Reverse transfer capacitance	$V_{GS} = 0$		125		pF
Qg	Total gate charge	V _{DD} = 48V, I _D = 60A,		49	66	nC
Q _{gs}	Gate-source charge	$V_{\text{DD}} = 48\text{V}, \text{ I}_{\text{D}} = 60\text{A},$ $V_{\text{GS}} = 10\text{V}$		18		nC
Q _{gd}	Gate-drain charge	(see Figure 12)		14		nC

1. Pulsed: Pulse duration = 300 μ s, duty cycle 1.5%

Table 6.	Switching	times
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Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)} t _r	Turn-on delay time Rise time			16 108		ns ns
t _{d(off)} t _f	Turn-off-delay time Fall time	$V_{DD} = 30V, I_D = 30A,$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see Figure 13)		43 20		ns ns



Symbol	Parameter	Test conditions	Min	Тур.	Max	Unit
I _{SD}	Source-drain current				30	А
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				120	А
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 60A, V_{GS} = 0$			1.3	V
t _{rr} Q _{rr} I _{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I _{SD} = 60A, V _{DD} =25V di/dt = 100A/μs, Tj = 150°C <i>(see Figure 13)</i>		75 182 5		ns nC A

Table 7.Source drain diode

1. Pulse width limited by safe operating area

2. Pulsed: Pulse duration = 300 μ s, duty cycle 1.5%



TOFPD

 $Z_{th} = k R_{thJ-c}$

10⁰ tp(s)

 $\overline{I_{D}}(A)$

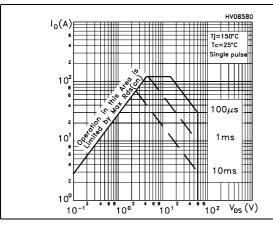
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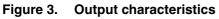
 $\delta=\,{\rm t_p}\,/\tau$

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Electrical characteristics (curves) 2.1

Figure 1. Safe operating area





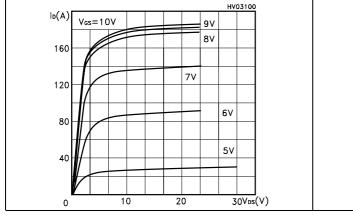
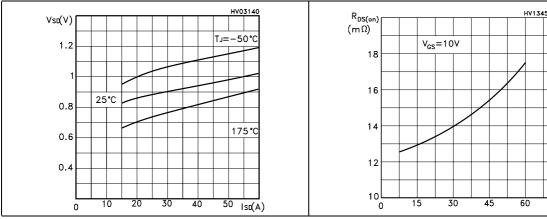


Figure 5. Source-drain diode forward characteristics





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SINGLE

Thermal impedance

0.05

0.01

10⁻²

PULSE

10-3

Figure 2.

10

10

10

10-

0.2

0.1

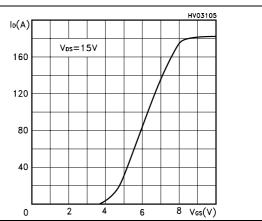
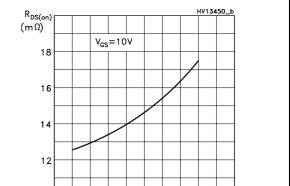
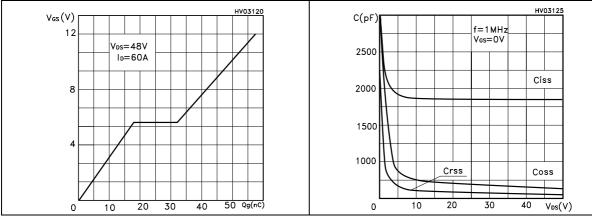


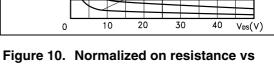
Figure 6. Static drain-source on resistance



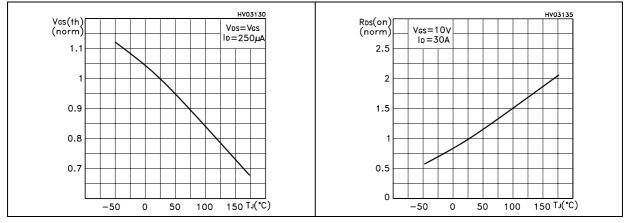


Gate charge vs gate-source voltage Figure 8. Capacitance variations Figure 7.

Figure 9. Normalized gate threshold voltage vs temperature



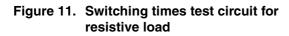
temperature





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3 Test circuit



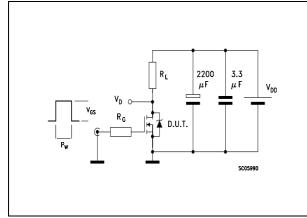
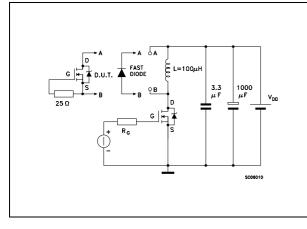
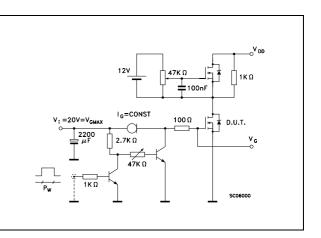


Figure 13. Test circuit for inductive load switching and diode recovery times









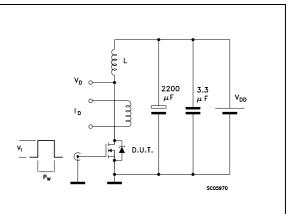
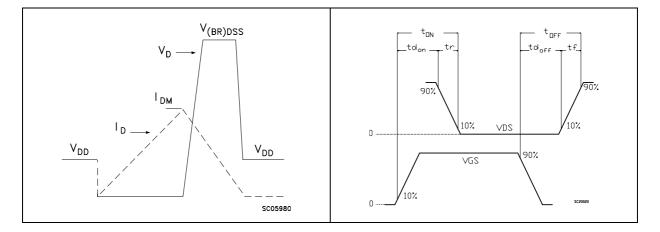


Figure 16. Switching time waveform



4 Package mechanical data

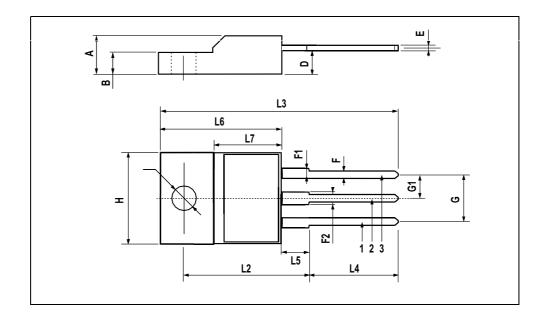
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*



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DIM.	mm.		inch			
DIN.	MIN.	ТҮР	MAX.	MIN.	TYP.	MAX.
А	4.4		4.6	0.173		0.181
В	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
Н	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126

TO-220FP MECHANICAL DATA



5 Revision history

Table 8. Revision history

Date	Revision	Changes
14-Mar-2007	1	First release



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