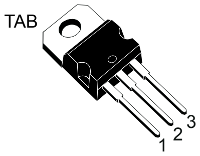
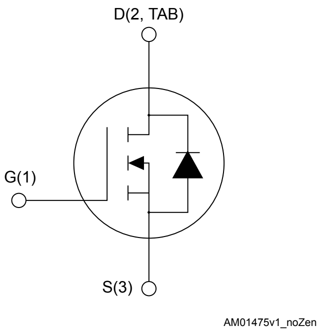
N-channel 650 V, 39 mΩ typ., 54 A MDmesh M9 Power MOSFET in a TO-220 package



TO-220



Product status link
STP65N045M9

Product summary	
Order code	STP65N045M9
Marking	65N045M9
Package	TO-220
Packing	Tube

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STP65N045M9	650 V	45 mΩ	54A

- Worldwide best FOM $R_{DS(on)}$*Q_g among silicon-based devices
- Higher V_{DSS} rating
- Higher dv/dt capability
- Excellent switching performance
- Easy to drive
- 100% avalanche tested

Applications

- High efficiency switching applications

Description

This N-channel Power MOSFET is based on the most innovative super-junction MDmesh M9 technology, suitable for medium/high voltage MOSFETs featuring very low $R_{DS(on)}$ per area. The silicon based M9 technology benefits from a multi-drain manufacturing process which allows an enhanced device structure. The resulting product has one of the lower on-resistance and reduced gate charge values, among all silicon based fast switching super-junction Power MOSFETs, making it particularly suitable for applications that require superior power density and outstanding efficiency.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±30	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	54	A
	Drain current (continuous) at T_C = 100 °C	34	
I_{DM} (2)	Drain current (pulsed)	170	A
P_{TOT}	Total power dissipation at T_C = 25 °C	245	W
dv/dt (3)	Peak diode recovery voltage slope	50	V/ns
di/dt (3)	Peak diode recovery current slope	900	A/µs
dv/dt (4)	MOSFET dv/dt ruggedness	120	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		°C

1. *Referred to TO-247 long leads package.*
2. *Pulse width is limited by safe operating area.*
3. *I_{SD} ≤ 28 A, V_{DS} (peak) < $V_{(BR)DSS}$, V_{DD} = 400 V.*
4. *V_{DS} (peak) < $V_{(BR)DSS}$, V_{DD} ≤ 400 V.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.51	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	62.5	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_J max.)	6	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	775	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. On-/off-states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	650			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V			1	µA
		V_{GS} = 0 V, V_{DS} = 650 V, T_C = 125 °C[(1)]			200	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3.2	3.7	4.2	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 28 A		39	45	mΩ

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 400 V, f = 1 MHz, V_{GS} = 0 V	-	4610	-	pF
C_{oss}	Output capacitance		-	76	-	pF
$C_{oss\ eq.}$[(1)]	Equivalent output capacitance	V_{DS} = 0 to 400 V, V_{GS} = 0 V	-	885	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	1	-	Ω
Q_g	Total gate charge	V_{DD} = 400 V, I_D = 28 A, V_{GS} = 0 to 10 V (see Figure 14. Test circuit for gate charge behavior)	-	80	-	nC
Q_{gs}	Gate-source charge		-	26.5	-	nC
Q_{gd}	Gate-drain charge		-	23.5	-	nC

1. *$C_{oss\ eq.}$ is a constant equivalent capacitance that provides the same charging time as C_{oss} while V_{DS} is rising from 0 V to the stated value.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}= 325 V, I_D = 28 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	25	-	ns
t_r	Rise time		-	26	-	ns
$t_{d(off)}$	Turn-off delay time		-	77	-	ns
t_f	Fall time		-	4	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} (1)	Source-drain current		-		54	A
I_{SDM} (2)	Source-drain current (pulsed)		-		170	A
V_{SD} (3)	Forward on voltage	I_{SD} = 55 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 55 A, di/dt = 100 A/µs, V_{DD} = 100 V (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	288		ns
Q_{rr}	Reverse recovery charge		-	4		µC
I_{RRM}	Reverse recovery current		-	26		A
t_{rr}	Reverse recovery time	I_{SD} = 55 A, di/dt = 100 A/µs, V_{DD} = 100 V, T_J = 150 °C (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	400		ns
Q_{rr}	Reverse recovery charge		-	7.5		µC
I_{RRM}	Reverse recovery current		-	34		A

1. *Referred to TO-247 long leads package.*
2. *Pulse width is limited by safe operating area.*
3. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

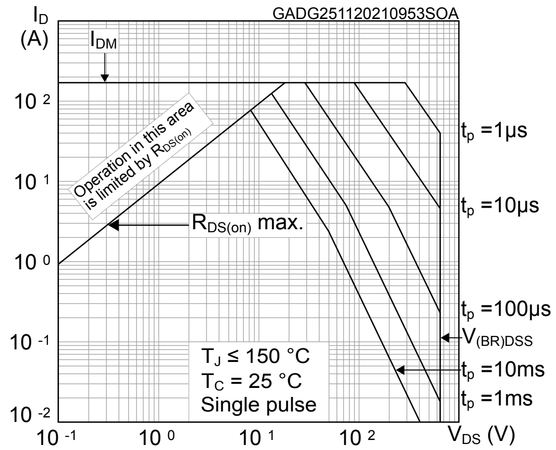


Figure 2. Maximum transient thermal impedance

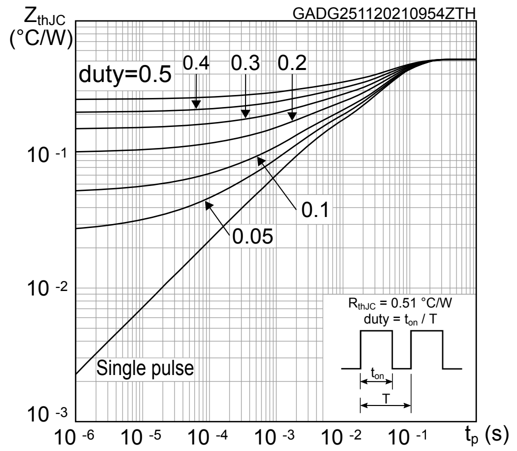


Figure 3. Typical output characteristics

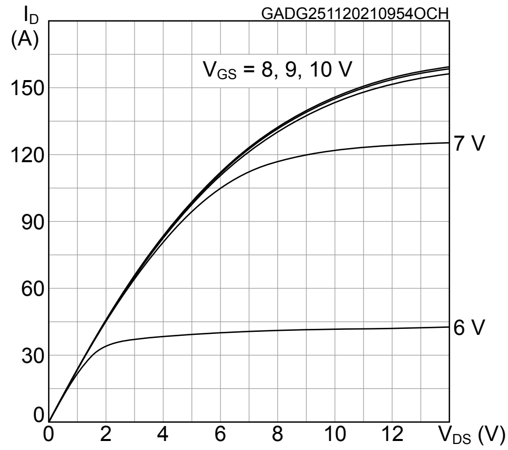


Figure 4. Typical transfer characteristics

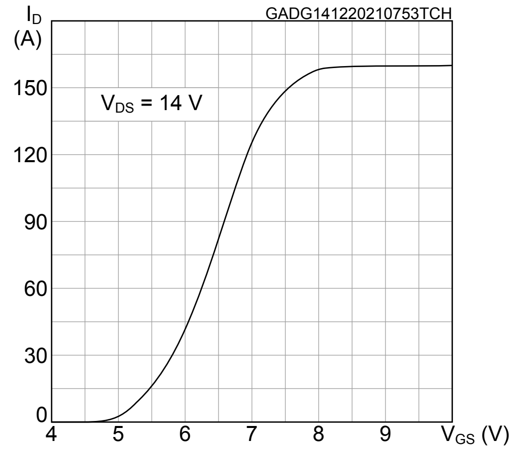


Figure 5. Typical gate charge characteristics

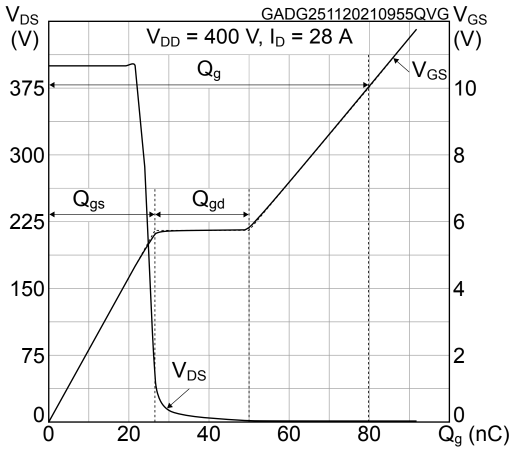


Figure 6. Typical drain-source on-resistance

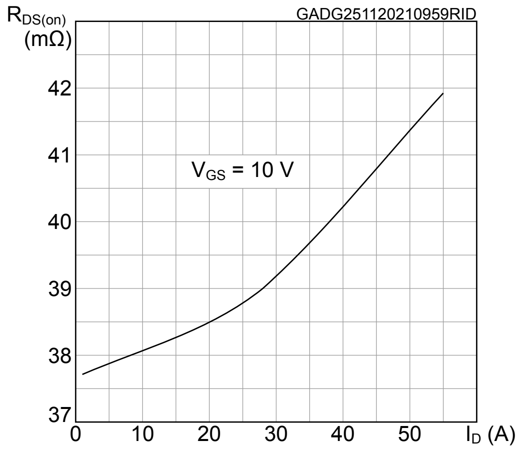


Figure 7. Typical capacitance characteristics

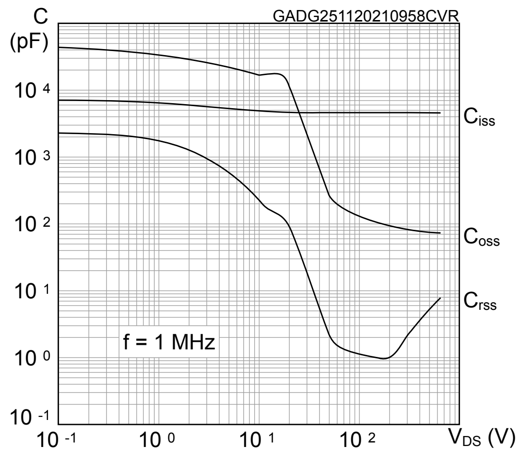


Figure 8. Typical output capacitance stored energy

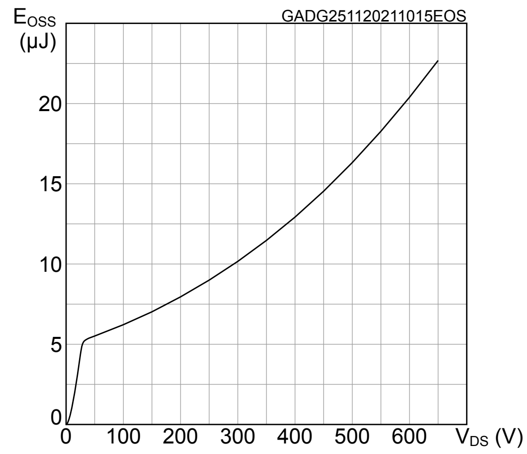


Figure 9. Normalized gate threshold vs temperature

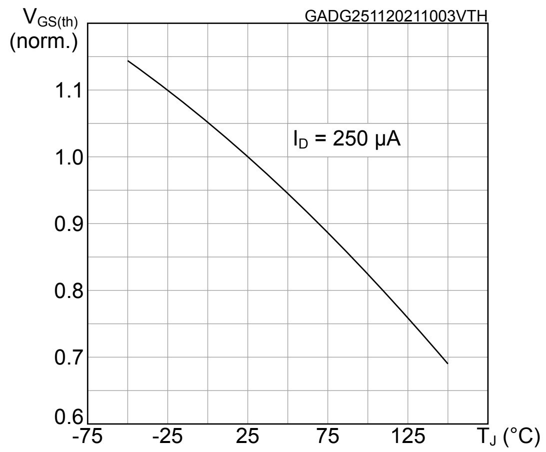


Figure 10. Normalized on-resistance vs temperature

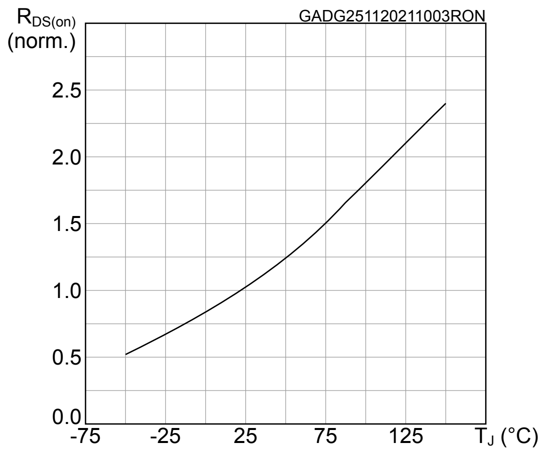


Figure 11. Normalized breakdown voltage vs temperature

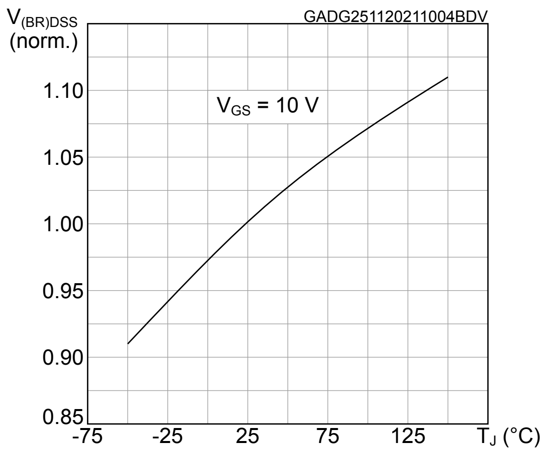
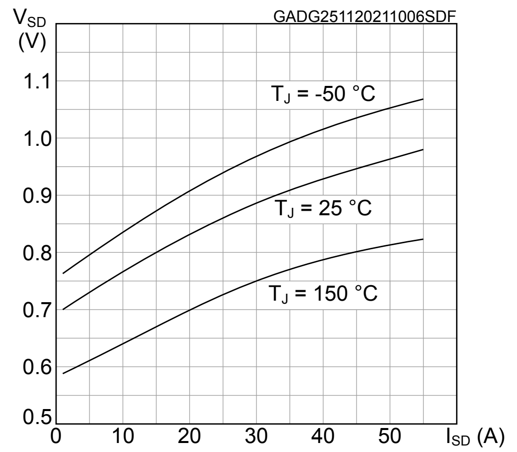


Figure 12. Typical reverse diode forward characteristics



3 Test circuits

Figure 13. Test circuit for resistive load switching times

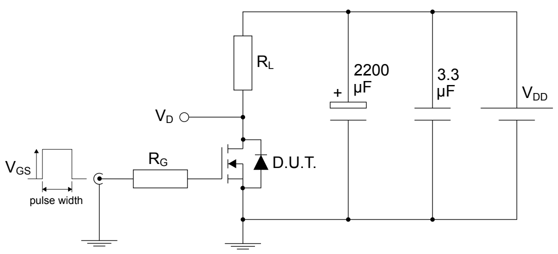


Figure 14. Test circuit for gate charge behavior

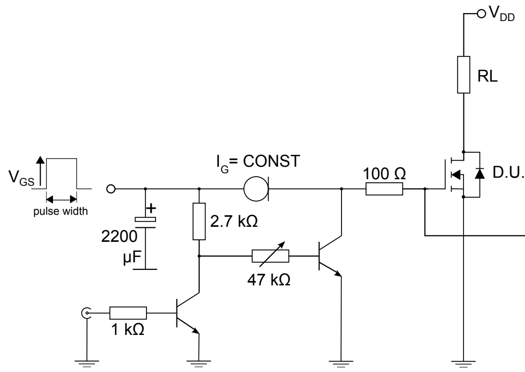


Figure 15. Test circuit for inductive load switching and diode recovery times

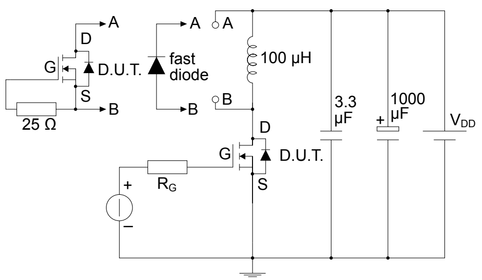


Figure 16. Unclamped inductive load test circuit

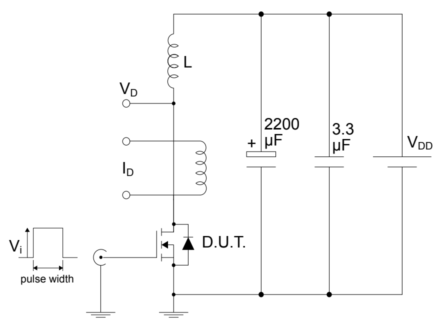


Figure 17. Unclamped inductive waveform

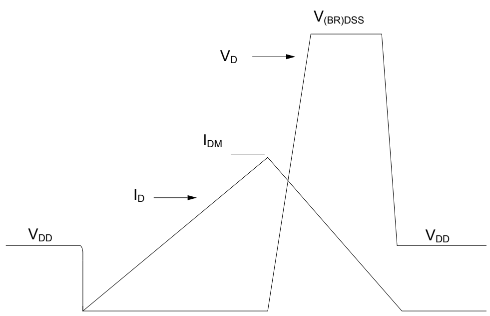
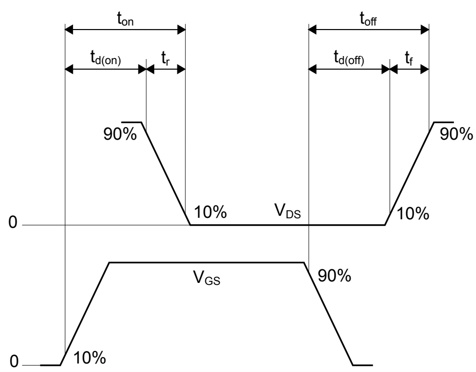


Figure 18. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220 type A package information

Figure 19. TO-220 type A package outline

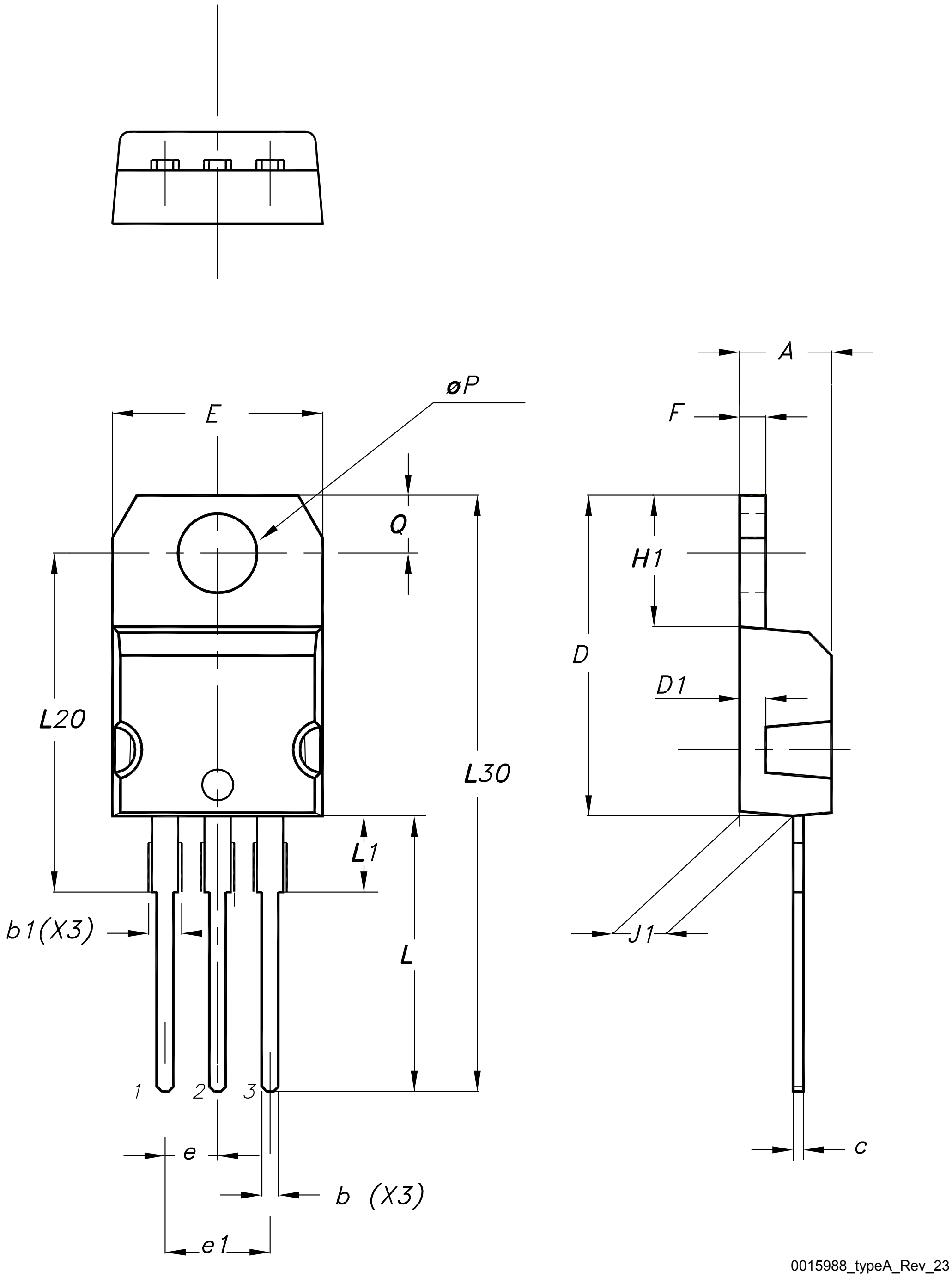


Table 8. **TO-220 type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

Revision history

Table 9. Document revision history

Date	Version	Changes
24-Feb-2021	1	First release.
16-Dec-2021	2	Updated title, *Features* and *Description* on cover page. Updated *Section 1 Electrical ratings.* Updated *Section 2 Electrical characteristics.* Added *Section 2.1 Electrical characteristics (curves).* Updated *Section 3 Test circuits.*
16-Feb-2022	3	Updated *Table 1. Absolute maximum ratings.* Updated *Table 5. Dynamic.* Minor text changes.
25-May-2022	4	Updated *Features* on cover page.
04-Sep-2023	5	Updated title and Features on cover page. Updated Table 1. Absolute maximum ratings. Updated Table 6. Switching times. Updated Table 7. Source-drain diode. Updated Section 3 Test circuits.

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