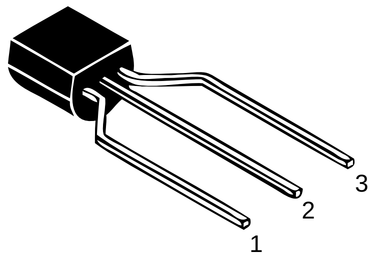
STQ2LN60K3-AP

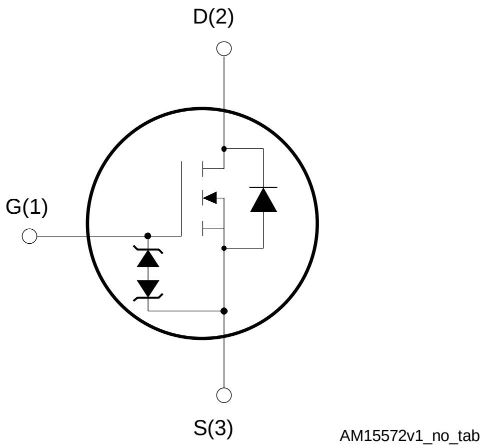
N-channel 600 V, 4 Ω typ., 0.6 A MDmesh™ K3 Power MOSFET in a TO-92 package

Datasheet - production data



TO-92 ammopack

Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max	I_D	P_{TOT}
STQ2LN60K3-AP	600 V	4.5 Ω	0.6 A	2.5 W

- 100% avalanche tested
- Extremely high dv/dt capability
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

Applications

- Switching applications

Description

This MDmesh™ K3 Power MOSFET is the result of improvements applied to STMicroelectronics' MDmesh™ technology, combined with a new optimized vertical structure. This device boasts an extremely low on-resistance, superior dynamic performance and high avalanche capability, rendering it suitable for the most demanding applications.

Table 1: Device summary

Order code	Marking	Package	Packaging
STQ2LN60K3-AP	2LN60K3	TO-92	Ammopack

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	600	V
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25 °C	0.6	A
I_D	Drain current (continuous) at T_C = 100 °C	0.38	A
I_{DM} (1)	Drain current (pulsed)	2.4	A
P_{TOT}	Total dissipation at T_C = 25 °C	2.5	W
dv/dt (2)	Peak diode recovery voltage slope	12	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_j	Operating junction temperature range		

Notes:

(1)Pulse width limited by safe operating area.

(2)I_{SD} ≤ 2 A, di/dt ≤ 400 A/µs, $V_{DS(peak)} < V_{(BR)DSS}$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	50	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient	120	°C/W

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AS}	Single pulse avalanche current (pulse width limited by T_{jmax})	2	A
E_{AS}	Single pulse avalanche energy (starting T_J=25 °C, I_D=I_{AR}, V_{DD}=50 V)	80	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 5: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_C= 125 °C (1)			50	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 50 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 1 A		4	4.5	Ω

Notes:

(1)Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0 V	-	235	-	pF
C_{oss}	Output capacitance		-	22	-	pF
C_{rss}	Reverse transfer capacitance		-	3.5	-	pF
$C_{o(tr)}$(1)	Eq. capacitance time related	V_{GS} = 0 V, V_{DS} = 0 to 480 V	-	14	-	pF
$C_{o(er)}$(2)	Eq. capacitance energy related		-	10		pF
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 1 A, V_{GS} = 0 to 10 V (see *Figure 16: "Test circuit for gate charge behavior"*)	-	12	-	nC
Q_{gs}	Gate-source charge		-	1.8	-	nC
Q_{gd}	Gate-drain charge		-	7.7	-	nC
R_G	Gate input resistance	f=1 MHz, I_D=0 A	-	7	-	Ω

Notes:

(1)$C_{oss\ eq.}$ time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

(2)$C_{oss\ eq.}$ energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 1 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 15: "Test circuit for resistive load switching times"* and *Figure 20: "Switching time waveform"*)	-	10	-	ns
t_r	Rise time		-	8.5	-	ns
$t_{d(off)}$	Turn-off delay time		-	23.5	-	ns
t_f	Fall time		-	21	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} (1)	Source-drain current		-		0.6	A
I_{SDM} (1)	Source-drain current (pulsed)		-		2.4	A
V_{SD} (2)	Forward on voltage	I_{SD} = 2 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 2 A, di/dt = 100 A/µs V_{DD} = 60 V (see *Figure 17: "Test circuit for inductive load switching and diode recovery times"*)	-	200		ns
Q_{rr}	Reverse recovery charge		-	800		nC
I_{RRM}	Reverse recovery current		-	8		A
t_{rr}	Reverse recovery time	I_{SD} = 2 A, di/dt = 100 A/µs V_{DD} = 60 V, T_j = 150 °C (see *Figure 17: "Test circuit for inductive load switching and diode recovery times"*)	-	230		ns
Q_{rr}	Reverse recovery charge		-	950		nC
I_{RRM}	Reverse recovery current		-	8.5		A

Notes:

(1)Pulse width limited by safe operating area.

(2)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS}= ±1 mA, I_D= 0 A	30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection,thus eliminating the need for additional external componentry.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

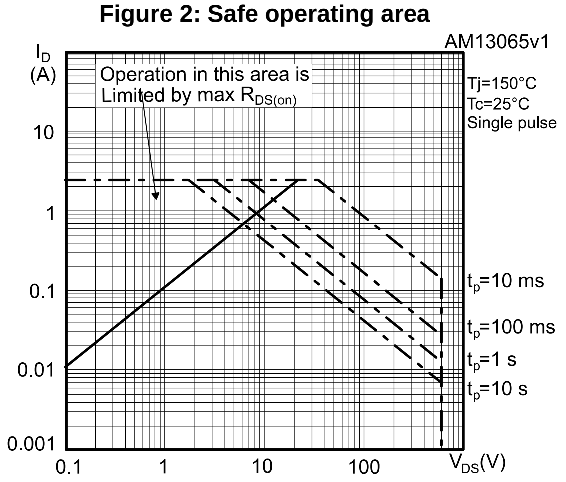


Figure 3: Thermal impedance

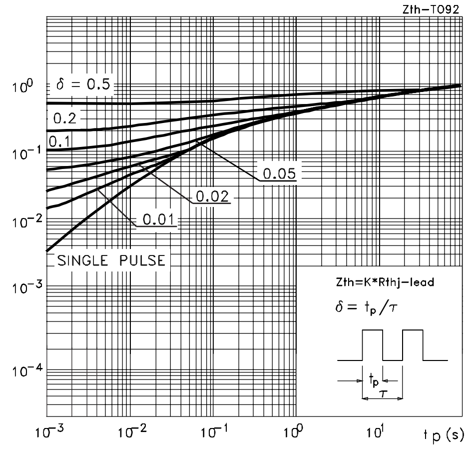


Figure 4: Output characteristics

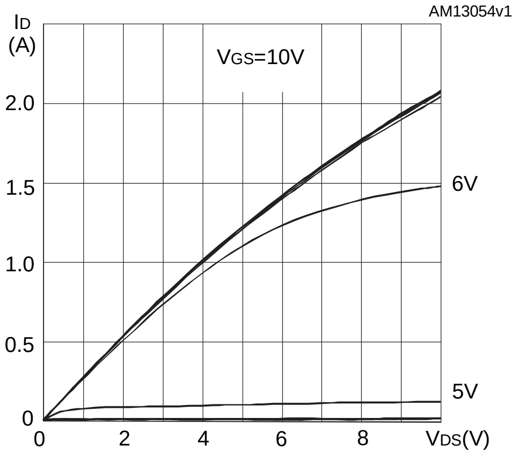


Figure 5: Transfer characteristics

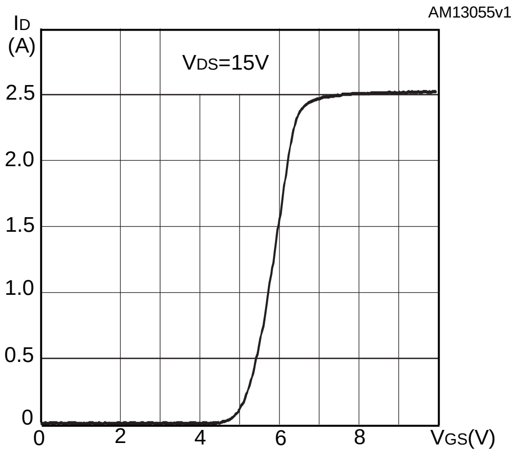


Figure 6: Gate charge vs gate-source voltage

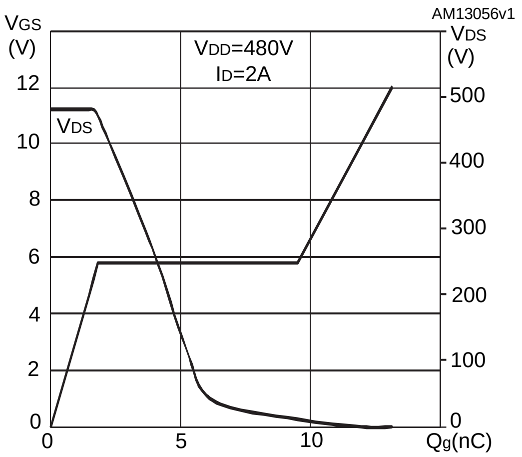


Figure 7: Static drain-source on-resistance

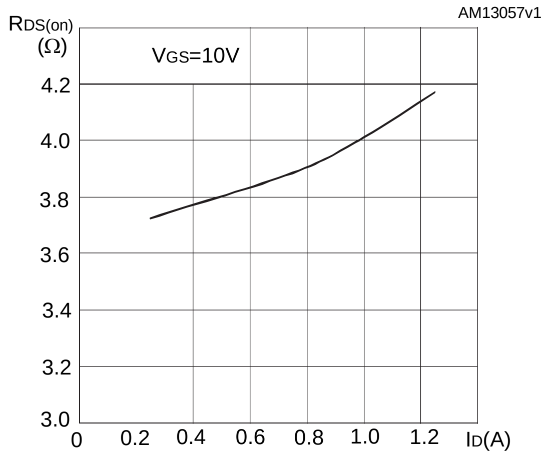


Figure 8: Capacitance variations

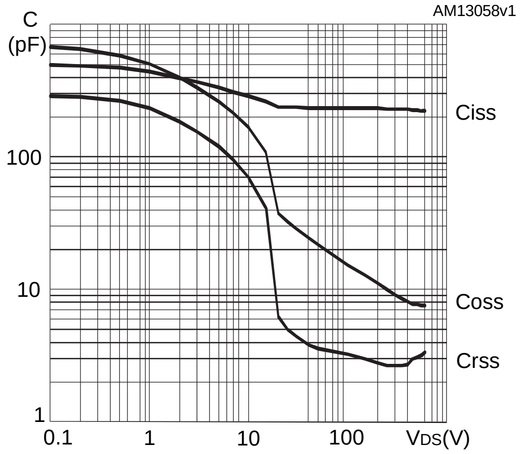


Figure 9: Source-drain diode forward characteristics

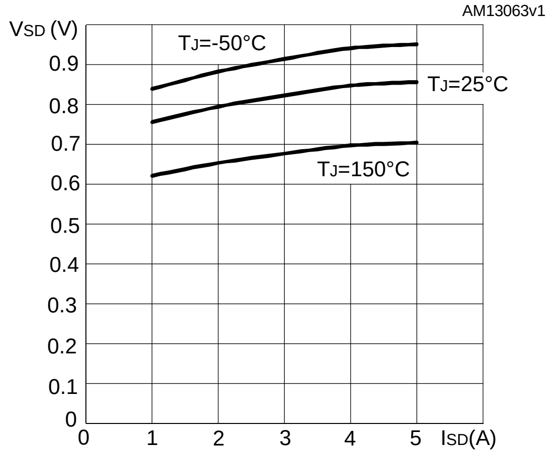


Figure 10: Normalized gate threshold voltage vs temperature

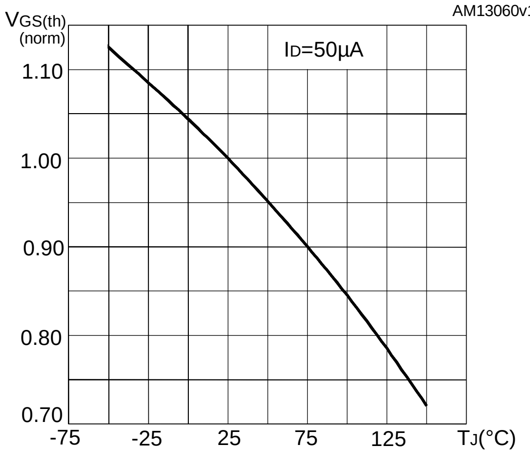


Figure 11: Normalized on-resistance vs temperature

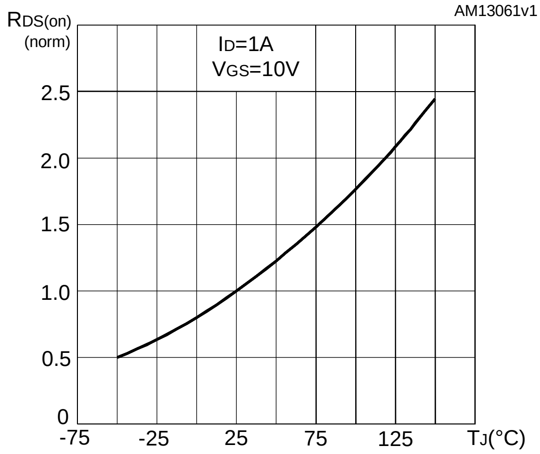


Figure 12: Normalized $V_{(BR)DSS}$ vs temperature

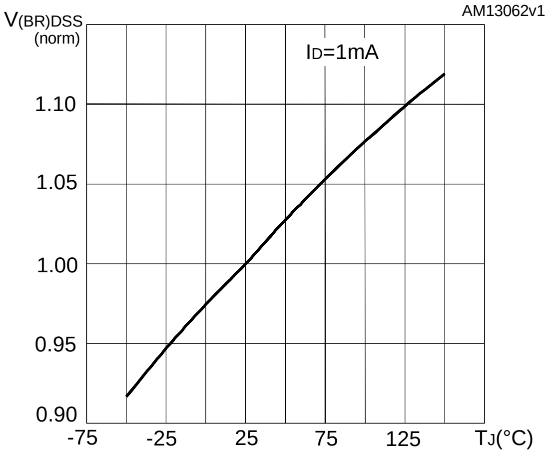


Figure 13: Output capacitance stored energy

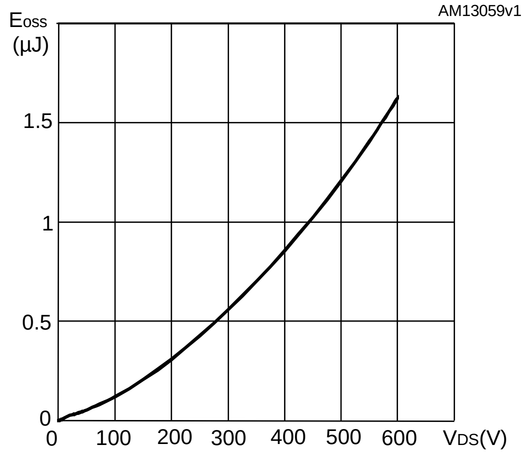
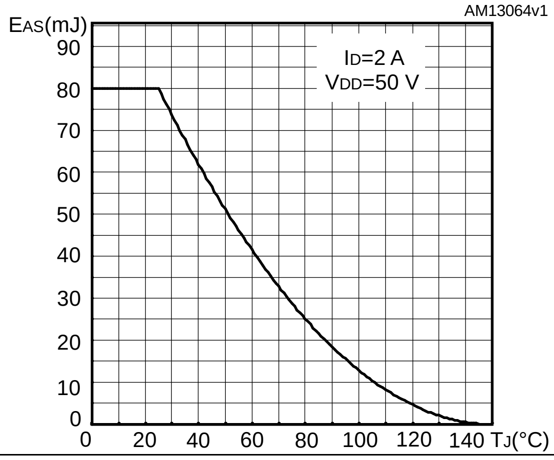


Figure 14: Maximum avalanche energy vs temperature



3 Test circuits

Figure 15: Test circuit for resistive load switching times

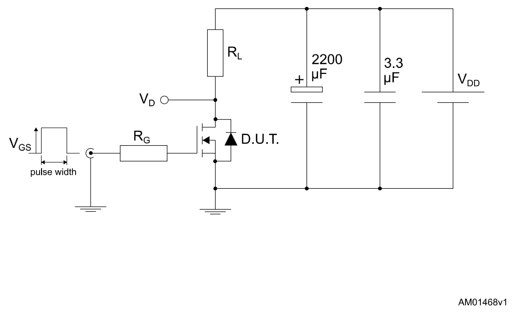


Figure 16: Test circuit for gate charge behavior

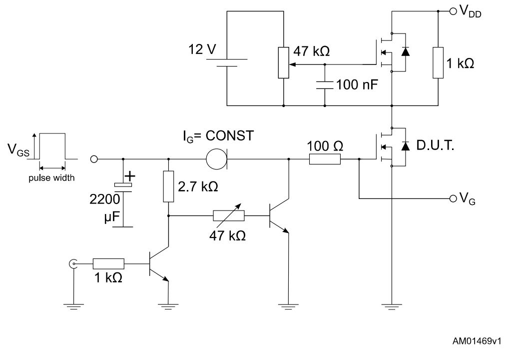


Figure 17: Test circuit for inductive load switching and diode recovery times

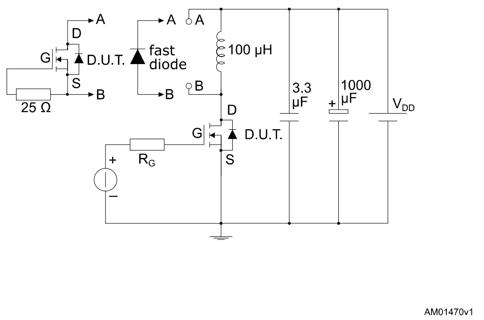


Figure 18: Unclamped inductive load test circuit

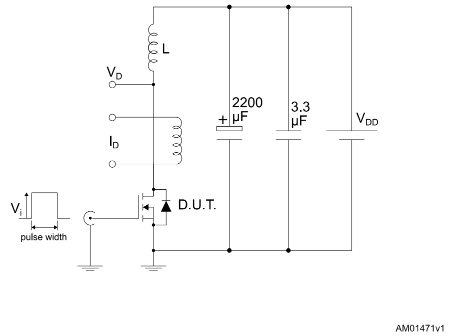


Figure 19: Unclamped inductive waveform

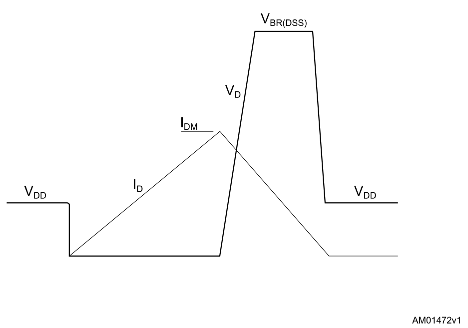
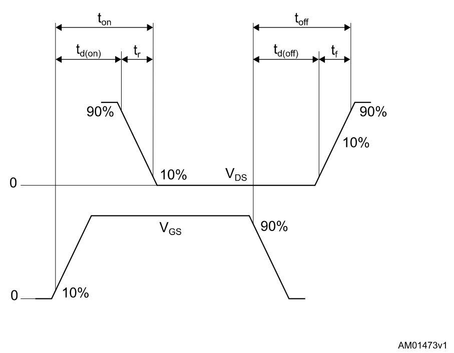


Figure 20: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 TO-92 ammopack package information

Figure 21: TO-92 ammopack package outline

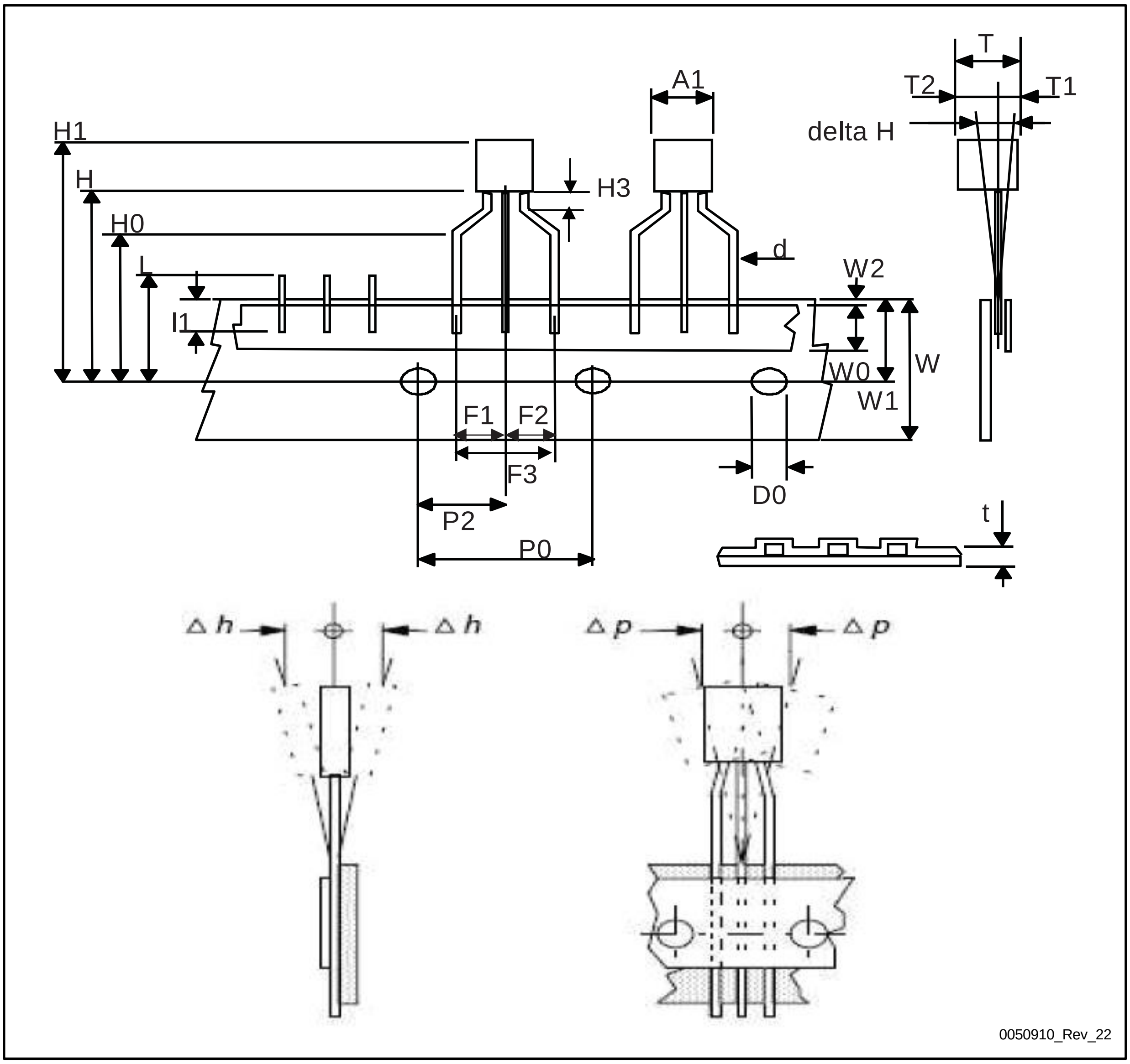


Table 10: TO-92 ammopak mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A1			4.80
T			3.80
T1			1.60
T2			2.30
d	0.45	0.47	0.48
P0	12.50	12.70	12.90
P2	5.65	6.35	7.05
F1, F2	2.40	2.50	2.94
F3	4.98	5.08	5.48
delta H	-2.00		2.00
W	17.50	18.00	19.00
W0	5.50	6.00	6.50
W1	8.50	9.00	9.25
W2			0.50
H		18.50	21.00
H0	15.50	16.00	18.20
H1		25.00	27.00
H3	0.50	1.00	2.00
D0	3.80	4.00	4.20
t			0.90
L			11.00
I1	3.00		
delta P	-1.00		1.00

5 Revision history

Table 11: Document revision history

Date	Revision	Changes
19-Jul-2012	1	First release.
24-Jan-2017	2	Modified title, features and description on cover page Modified *Table 2: "Absolute maximum ratings", Table 5: "On/off states"* and *Table 9: "Gate-source Zener diode"* Modified: *Figure 11: "Normalized on-resistance vs temperature"* Updated *Section 4.1: "TO-92 ammopack package information"* Minor text changes
01-Feb-2017	3	Modified *Figure 2: "Safe operating area".* Minor text changes.