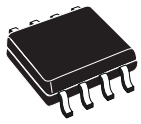
# STS1DNC45

## DUAL N-CHANNEL 450V - 4.1Ω - 0.4A SO-8
## SuperMESH™ POWER MOSFET

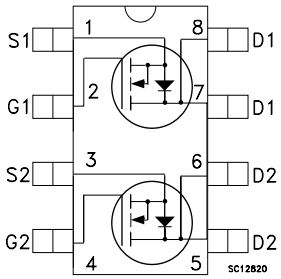
| TYPE | $V_{DSS}$ | $R_{DS(on)}$ | $I_D$ |
|---|---|---|---|
| STS1DNC45 | 450 V | < 4.5 Ω | 0.4 A |

- TYPICAL $R_{DS}(on)$ = 4.1Ω
- STANDARD OUTLINE FOR EASY AUTOMATED SURFACE MOUNT ASSEMBLY
- GATE CHARGE MINIMIZED



**SO-8**

**INTERNAL SCHEMATIC DIAGRAM**




### DESCRIPTION

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

### APPLICATIONS

- SWITCH MODE LOW POWER SUPPLIES (SMPS)
- DC-DC CONVERTERS
- LOW POWER, LOW COST CFL (COMPACT FLUORESCENT LAMPS)
- LOW POWER BATTERY CHARGERS

### ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain-source Voltage ($V_{GS}$ = 0) | 450 | V |
| $V_{DGR}$ | Drain-gate Voltage ($R_{GS}$ = 20 kΩ) | 450 | V |
| $V_{GS}$ | Gate- source Voltage | ± 30 | V |
| $I_D$ | Drain Current (continuous) at $T_C$ = 25°C<br>Drain Current (continuous) at $T_C$ = 100°C | 0.40<br>0.25 | A<br>A |
| $I_{DM}$ (•) | Drain Current (pulsed) | 1.6 | A |
| $P_{TOT}$ | Total Dissipation at $T_C$ = 25°C Dual Operation<br>Total Dissipation at $T_C$ = 25°C Single Operation | 1.6<br>2 | W<br>W |
| dv/dt(1) | Peak Diode Recovery voltage slope | 3 | V/ns |

(●) Pulse width limited by safe operating area

(1)$I_{SD}$ ≤ 0.4 A, di/dt ≤100A/µs, $V_{DD}$ ≤ $V_{(BR)DSS}$, $T_j$ ≤ $T_{JMAX.}$

## THERMAL DATA

| | | | |
|---|---|---|---|
| Rthj-amb(#) | Thermal Resistance Junction-ambient Max Single Operation<br>Thermal Resistance Junction-ambient Max Dual Operation | 62.5<br>78 | °C/W<br>°C/W |
| $T_j$ | Max. Operating Junction Temperature | 150 | °C |
| $T_{stg}$ | Storage Temperature | –65 to 150 | °C |

(#) When Mounted on FR4 board (Steady State)

## AVALANCHE CHARACTERISTICS

| Symbol | Parameter | Max Value | Unit |
|---|---|---|---|
| $I_{AR}$ | Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by $T_j$ max) | 0.4 | A |
| $E_{AS}$ | Single Pulse Avalanche Energy (starting $T_j$ = 25 °C, $I_D = I_{AR}$, $V_{DD}$ = 50 V) | 30 | mJ |

## ELECTRICAL CHARACTERISTICS ($T_{CASE}$ = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source Breakdown Voltage | $I_D$ = 250 µA, $V_{GS}$ = 0 | 450 | | | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current ($V_{GS}$ = 0) | $V_{DS}$ = Max Rating | | | 1 | µA |
| | | $V_{DS}$ = Max Rating, $T_C$ = 125 °C | | | 50 | µA |
| $I_{GSS}$ | Gate-body Leakage Current ($V_{DS}$ = 0) | $V_{GS}$ = ± 30V | | | ±100 | nA |

ON (1)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS} = V_{GS}$, $I_D$ = 250µA | 2.3 | 3 | 3.7 | V |
| $R_{DS(on)}$ | Static Drain-source On Resistance | $V_{GS}$ = 10 V, $I_D$ = 0.5 A | | 4.1 | 4.5 | Ω |

DYNAMIC

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $g_{fs}$ (1) | Forward Transconductance | $V_{DS}$ = 25 V, $I_D$ = 0.5 A | | 1.1 | | S |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 25 V, f = 1 MHz, $V_{GS}$ = 0 | | 160 | | pF |
| $C_{oss}$ | Output Capacitance | | | 27.5 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 4.7 | | pF |

**ELECTRICAL CHARACTERISTICS** (CONTINUED)

SWITCHING ON

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turn-on Delay Time | $V_{DD}$ = 225 V, $I_D$ = 0.5 A | | 6.7 | | ns |
| $t_r$ | Rise Time | $R_G$ = 4.7Ω $V_{GS}$ = 10 V (see test circuit, Figure 3) | | 4 | | ns |
| $Q_g$ | Total Gate Charge | $V_{DD}$ = 360 V, $I_D$ = 1.5 A, | | 7 | 10 | nC |
| $Q_{gs}$ | Gate-Source Charge | $V_{GS}$ = 10 V | | 1.3 | | nC |
| $Q_{gd}$ | Gate-Drain Charge | | | 3.2 | | nC |

SWITCHING OFF

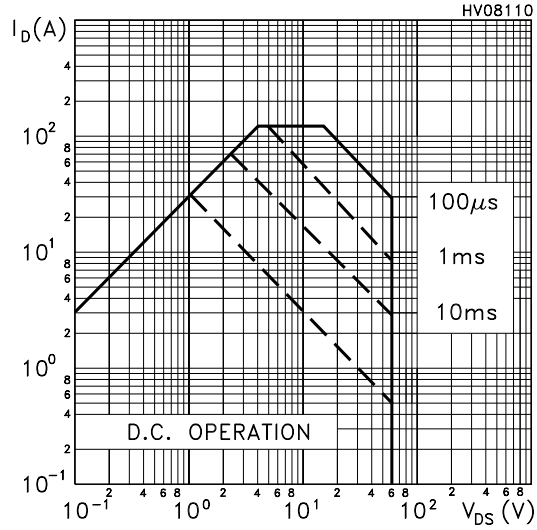
| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{r(off)}$ | Off-voltage Rise Time | $V_{DD}$ = 360 V, $I_D$ = 1.5 A | | 8.5 | | ns |
| $t_f$ | Fall Time | $R_G$ = 4.7Ω, $V_{GS}$ = 10 V | | 12 | | ns |
| $t_c$ | Cross-over Time | (see test circuit, Figure 5) | | 18 | | ns |

SOURCE DRAIN DIODE

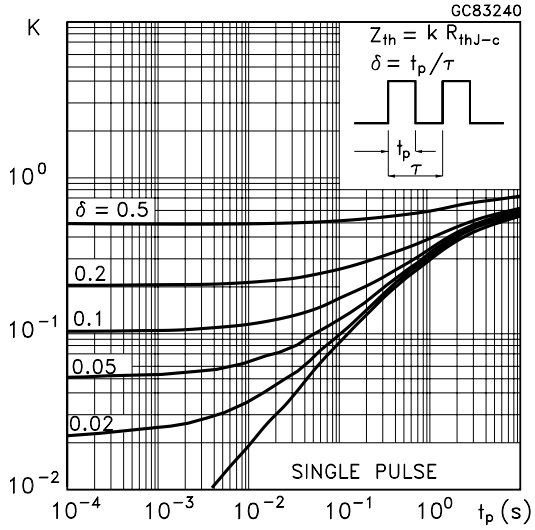
| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$ | Source-drain Current | | | | 0.4 | A |
| $I_{SDM}$ (2) | Source-drain Current (pulsed) | | | | 1.6 | A |
| $V_{SD}$ (1) | Forward On Voltage | $I_{SD}$ = 0.4 A, $V_{GS}$ = 0 | | | 1.6 | V |
| $t_{rr}$ | Reverse Recovery Time | $I_{SD}$ = 0.4 A, di/dt = 100A/µs, | | 225 | | ns |
| $Q_{rr}$ | Reverse Recovery Charge | $V_{DD}$ = 100 V, $T_j$ = 150°C | | 530 | | nC |
| $I_{RRM}$ | Reverse Recovery Current | (see test circuit, Figure 5) | | 4.7 | | A |

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

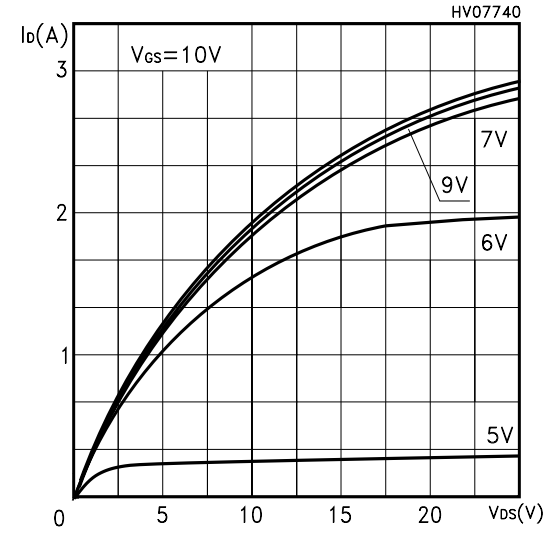
**Safe Operating Area**



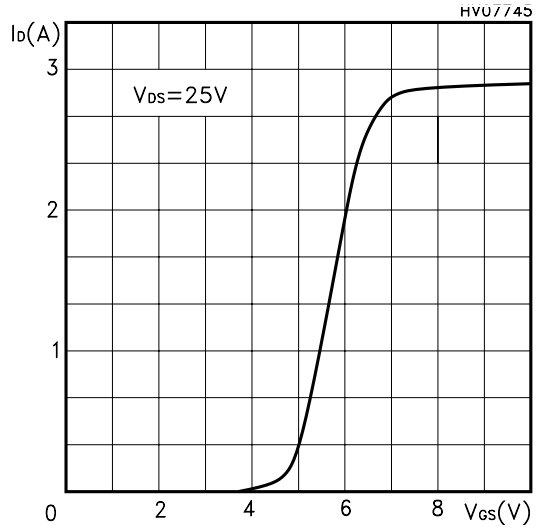

**Thermal Impedance**



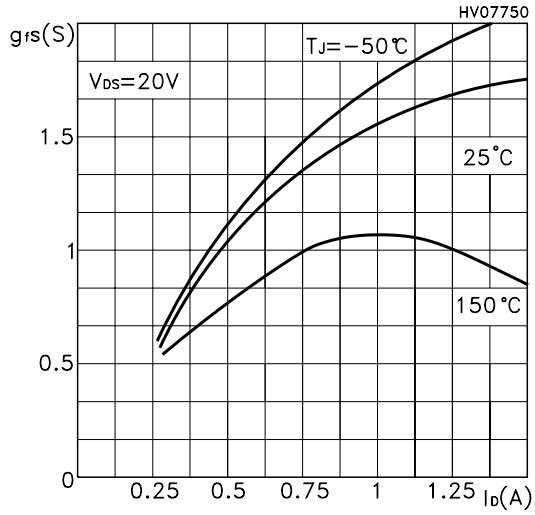
### Output Characteristics



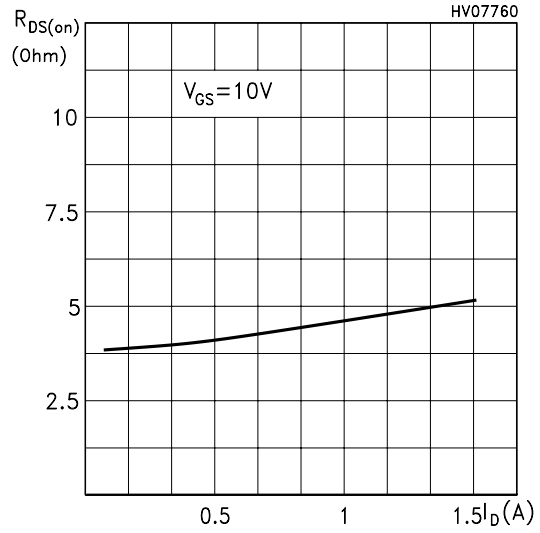

### Transfer Characteristics



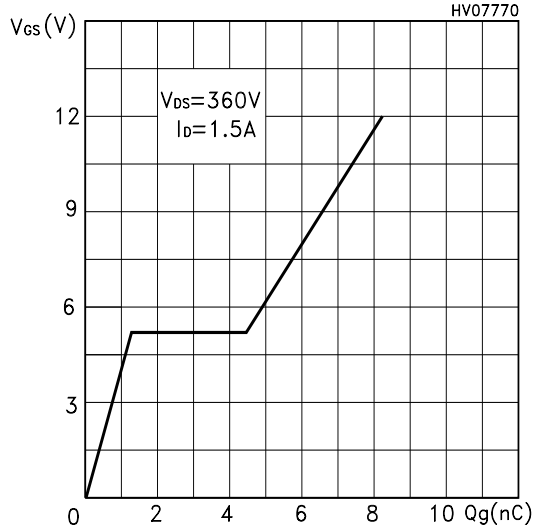

### Transconductance



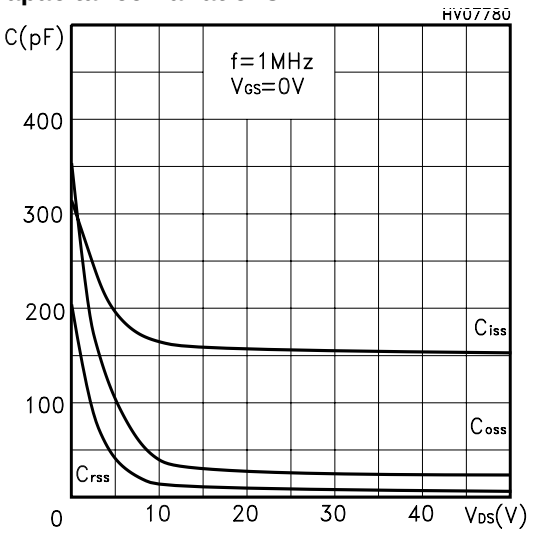

### Static Drain-source On Resistance



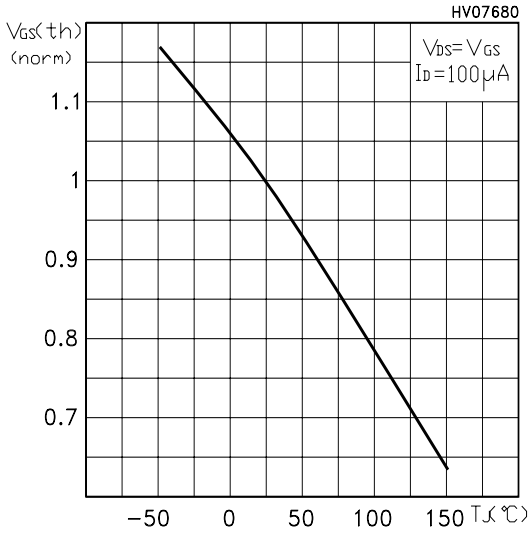

### Gate Charge vs Gate-source Voltage



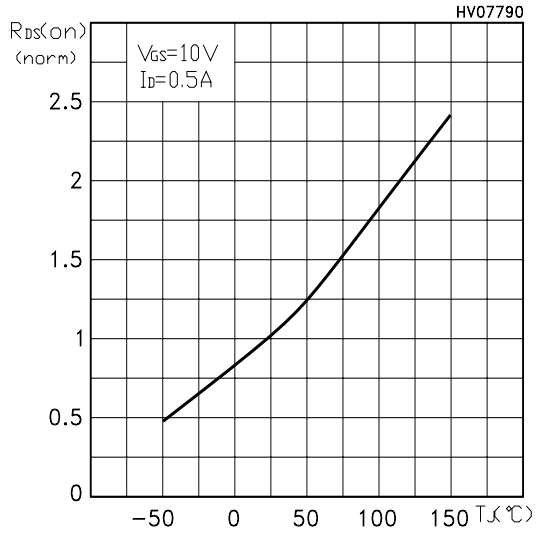

### Capacitance Variations



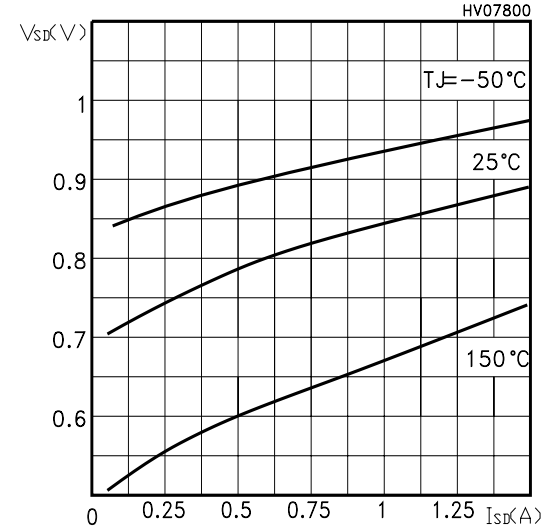
**Normalized Gate Threshold Voltage vs Temp.**



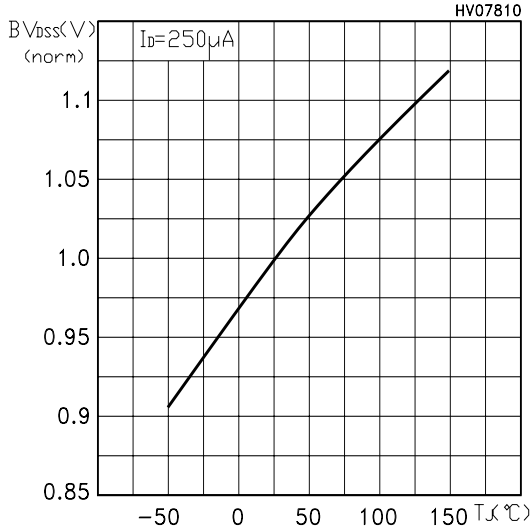

**Normalized On Resistance vs Temperature**



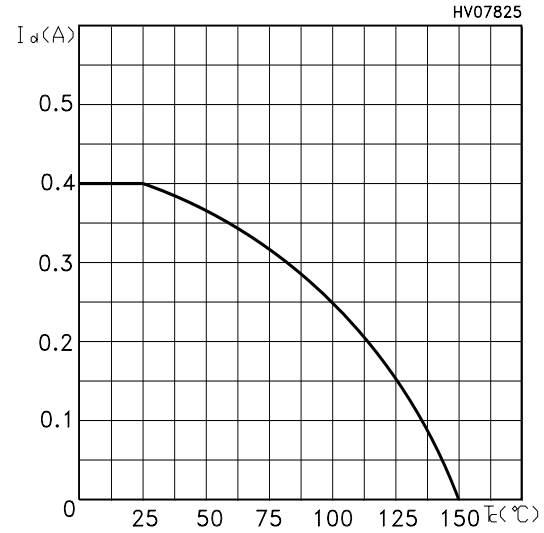

**Source-drain Diode Forward Characteristics**




**Normalized BVDSS vs Temperature**




**Max Id Current vs Tc**




**Maximum Avalanche Energy vs Temperature**

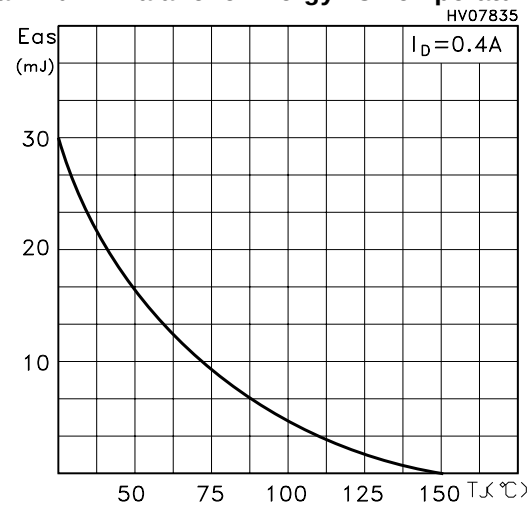


**Fig. 1:** Unclamped Inductive Load Test Circuit

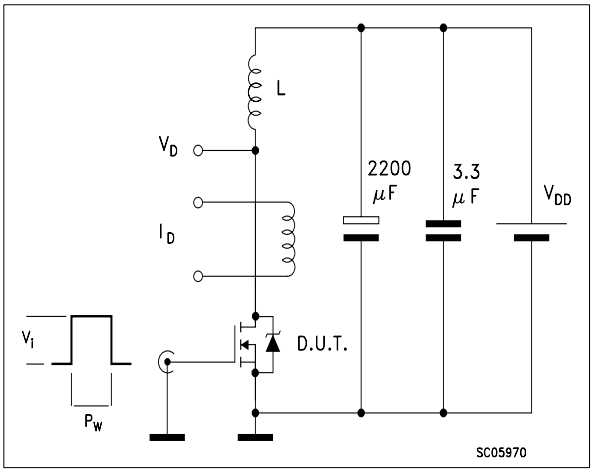



**Fig. 2:** Unclamped Inductive Waveform

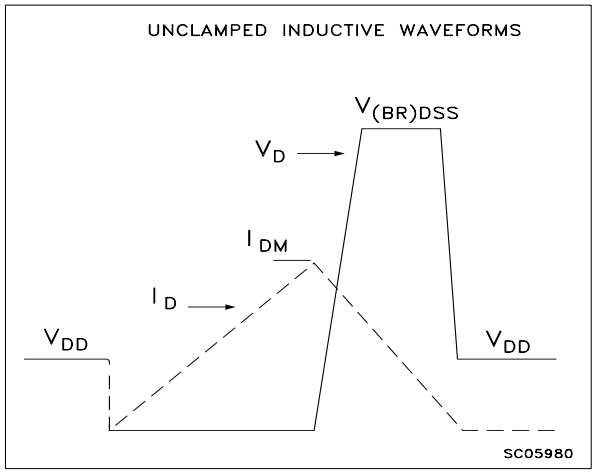



**Fig. 3:** Switching Times Test Circuit For Resistive Load

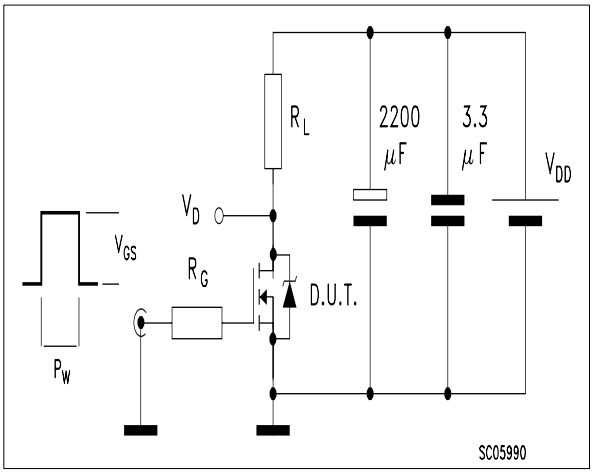



**Fig. 4:** Gate Charge test Circuit

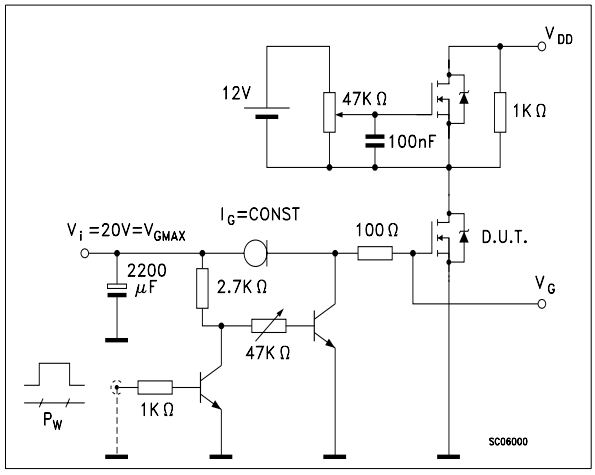
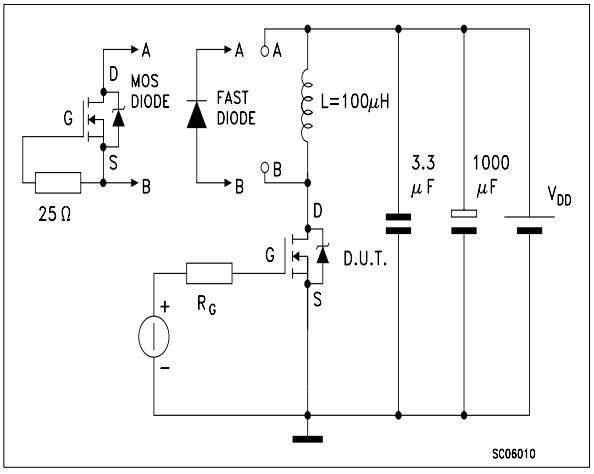
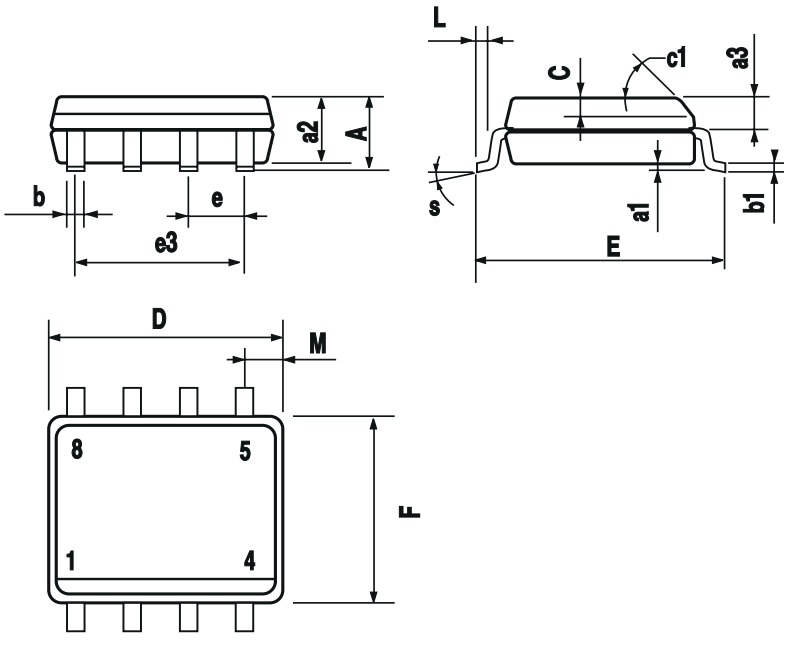



**Fig. 5:** Test Circuit For Inductive Load Switching And Diode Recovery Times



## SO-8 MECHANICAL DATA

| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 1.75 | | | 0.068 |
| a1 | 0.1 | | 0.25 | 0.003 | | 0.009 |
| a2 | | | 1.65 | | | 0.064 |
| a3 | 0.65 | | 0.85 | 0.025 | | 0.033 |
| b | 0.35 | | 0.48 | 0.013 | | 0.018 |
| b1 | 0.19 | | 0.25 | 0.007 | | 0.010 |
| C | 0.25 | | 0.5 | 0.010 | | 0.019 |
| c1 | 45 (typ.) | | | | | |
| D | 4.8 | | 5.0 | 0.188 | | 0.196 |
| E | 5.8 | | 6.2 | 0.228 | | 0.244 |
| e | | 1.27 | | | 0.050 | |
| e3 | | 3.81 | | | 0.150 | |
| F | 3.8 | | 4.0 | 0.14 | | 0.157 |
| L | 0.4 | | 1.27 | 0.015 | | 0.050 |
| M | | | 0.6 | | | 0.023 |
| S | 8 (max.) | | | | | |

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