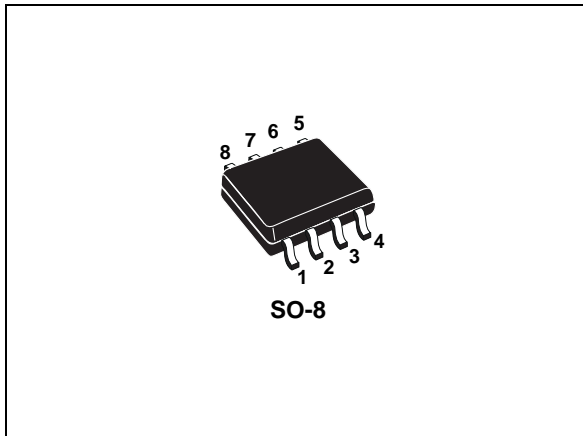


P-channel 60 V, 0.13 Ω typ., 3 A STripFET™ F6 Power MOSFET in a SO-8 package

Datasheet - production data



Features

Order code	V _{DSS}	R _{DS(on)max}	I _D
STN3P6F6	60 V	0.16 Ω @ 10 V	3 A

- R_{DS(on)} * Qg industry benchmark
- Extremely low on-resistance R_{DS(on)}
- High avalanche ruggedness
- Low gate drive power losses

Applications

- Switching applications

Description

This device is a P-channel Power MOSFET developed using the 6th generation of STripFET™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest R_{DS(on)} in all packages.

Figure 1. Internal schematic diagram

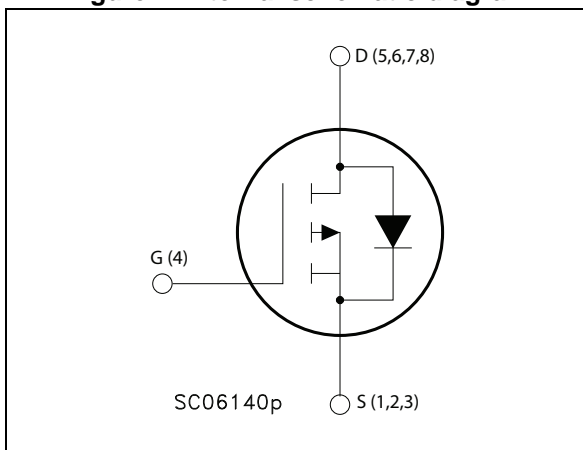


Table 1. Device summary

Order code	Marking	Package	Packaging
STS3P6F6	3K60	SO-8	Tape and reel

Note: For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

Contents

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	60	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	3	A
I_D	Drain current (continuous) at $T_{pcb} = 100\text{ }^\circ\text{C}$	2	A
$I_{DM}^{(1)}$	Drain current (pulsed)	12	A
P_{TOT}	Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	2.7	W
T_j P_{stg}	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

1. Pulse width is limited by safe operating area.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	47	$^\circ\text{C/W}$

1. When mounted on FR-4 board of 15 mm^2 , 2 Oz Cu, $t < 10\text{ sec}$

Note: For the P-channel Power MOSFET actual polarity of voltages and current has to be reversed.

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified).

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0, I _D = 250 μA	60			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0, V _{DS} = 60 V			1	μA
		V _{GS} = 0, V _{DS} = 60 V, T _C = 125 °C			10	μA
I _{GSS}	Gate-body leakage current	V _{DS} = 0, V _{GS} = ± 20 V			±100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	2		4	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 1.5 A		0.13	0.16	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{GS} = 0, V _{DS} = 48 V, f = 1 MHz	-	340	-	pF
C _{oss}	Output capacitance		-	40	-	pF
C _{rss}	Reverse transfer capacitance		-	20	-	pF
Q _g	Total gate charge	V _{DD} = 48 V, I _D = 3 A, V _{GS} = 10 V (see Figure 14)	-	6.4	-	nC
Q _{gs}	Gate-source charge		-	1.7	-	nC
Q _{gd}	Gate-drain charge		-	1.7	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 48 V, I _D = 1.5 A, R _G = 4.7 Ω, V _{GS} = 10 V (see Figure 13)	-	64	-	ns
t _r	Rise time		-	5.3	-	ns
t _{d(off)}	Turn-off delay time		-	14	-	ns
t _f	Fall time		-	3.7	-	ns

Note: For the P-channel Power MOSFET actual polarity of voltages and current has to be reversed.

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		3	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		12	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0, I_{SD} = 3 \text{ A}$	-		1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = 5 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 16 \text{ V}, T_j = 150 \text{ }^\circ\text{C}$ (see Figure 15)	-	20		ns
Q_{rr}	Reverse recovery charge		-	17.8		nC
I_{RRM}	Reverse recovery current		-	1.8		A

1. Pulse width limited by safe operating area.
2. Pulse duration = 300 μs , duty cycle 1.5%

Note: For the P-channel Power MOSFET actual polarity of voltages and current has to be reversed.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

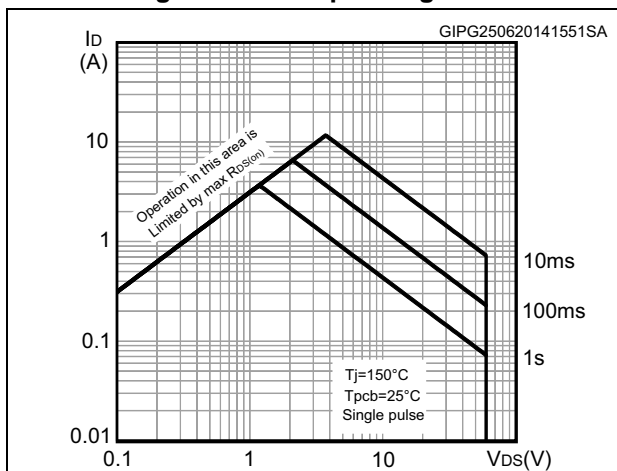


Figure 3. Thermal impedance

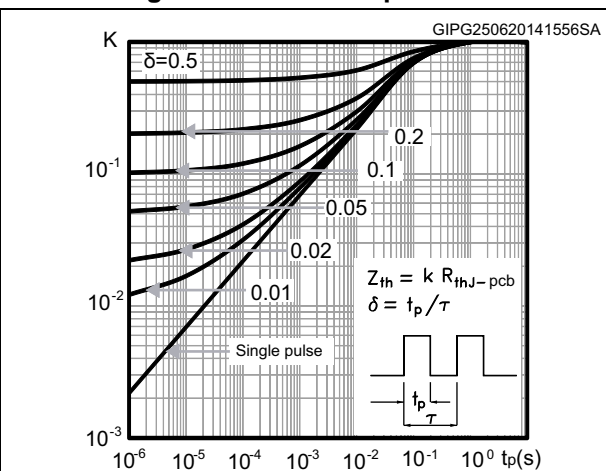


Figure 4. Output characteristics

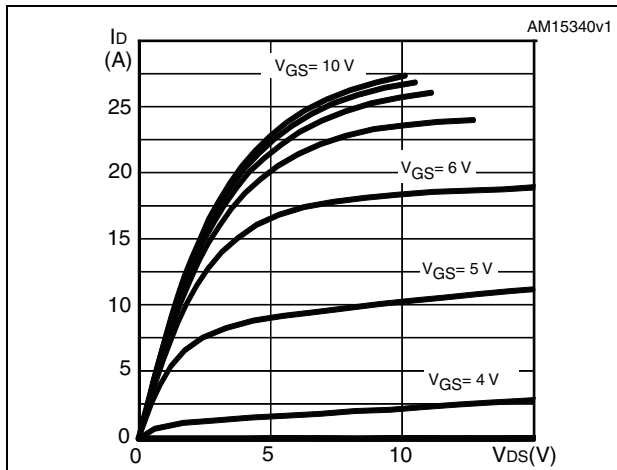


Figure 5. Transfer characteristics

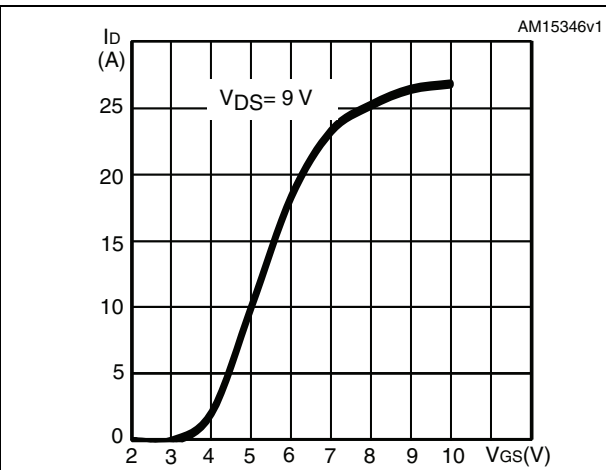


Figure 6. Gate charge vs gate-source voltage

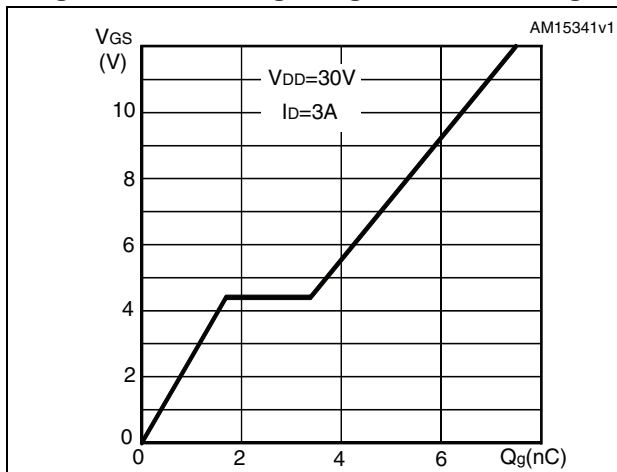


Figure 7. Static drain-source on-resistance

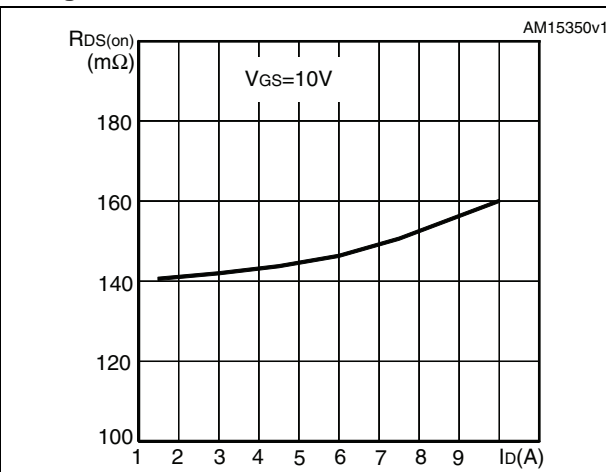


Figure 8. Capacitance variations

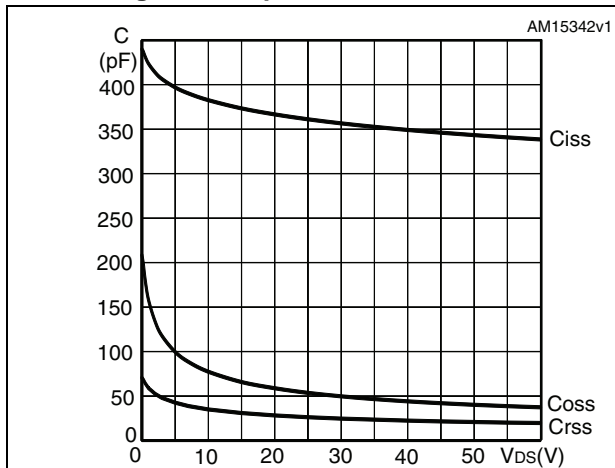


Figure 9. Normalized $V_{(BR)DSS}$ vs temperature

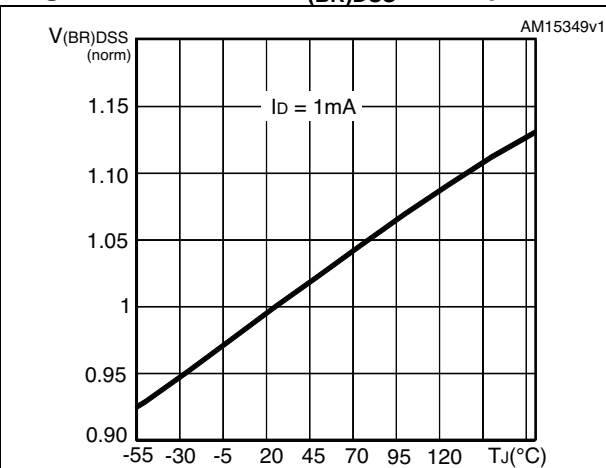


Figure 10. Normalized gate threshold voltage vs temperature

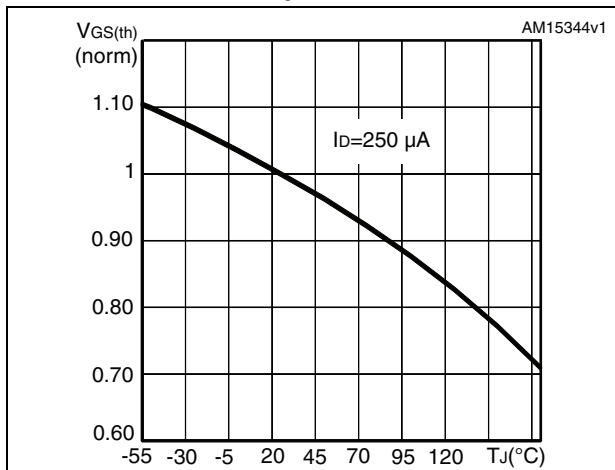


Figure 11. Normalized on-resistance vs temperature

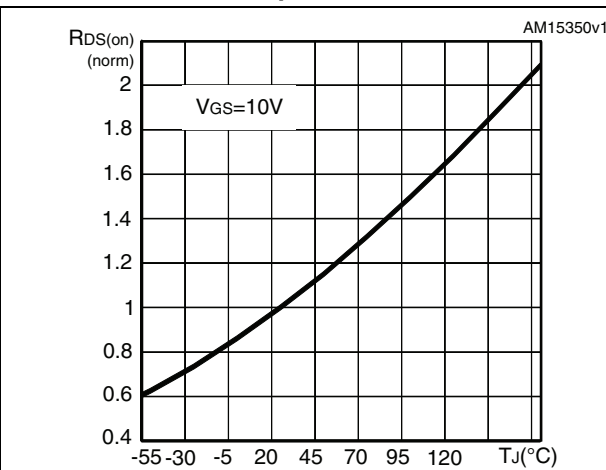
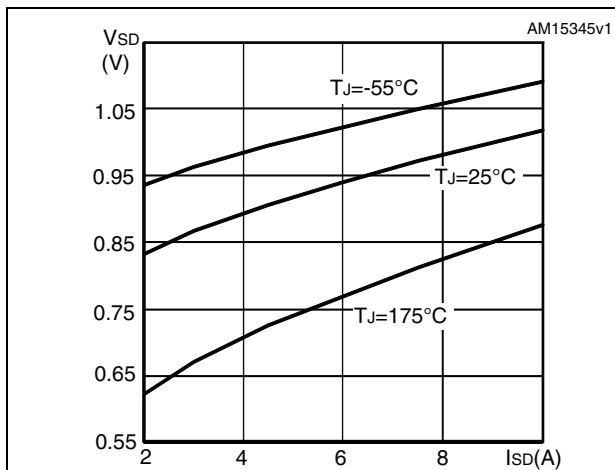


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

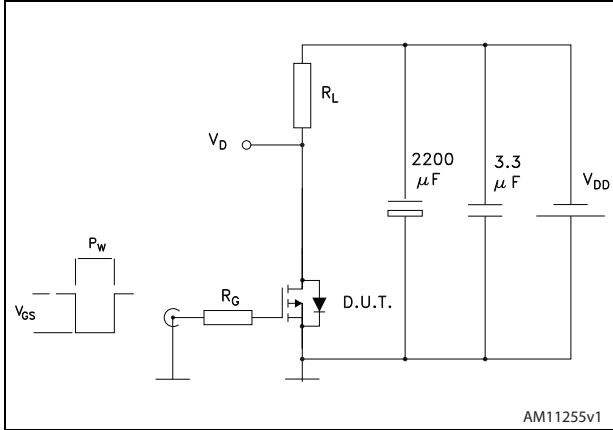


Figure 14. Gate charge test circuit

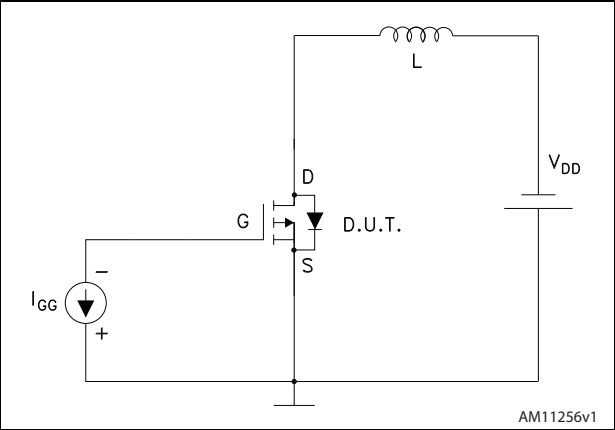
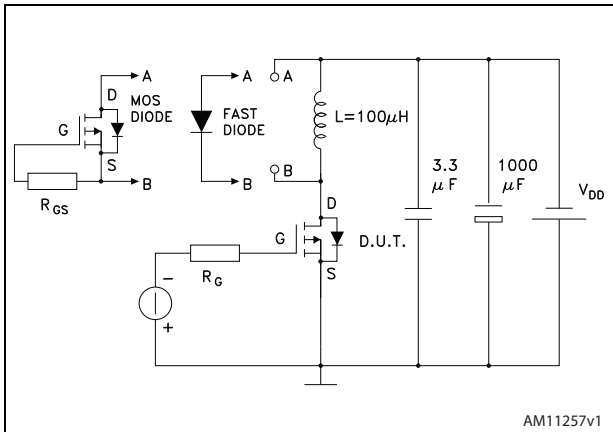


Figure 15. Test circuit for inductive load switching and diode recovery times



4 Package mechanical data

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Figure 16. SO-8 drawing

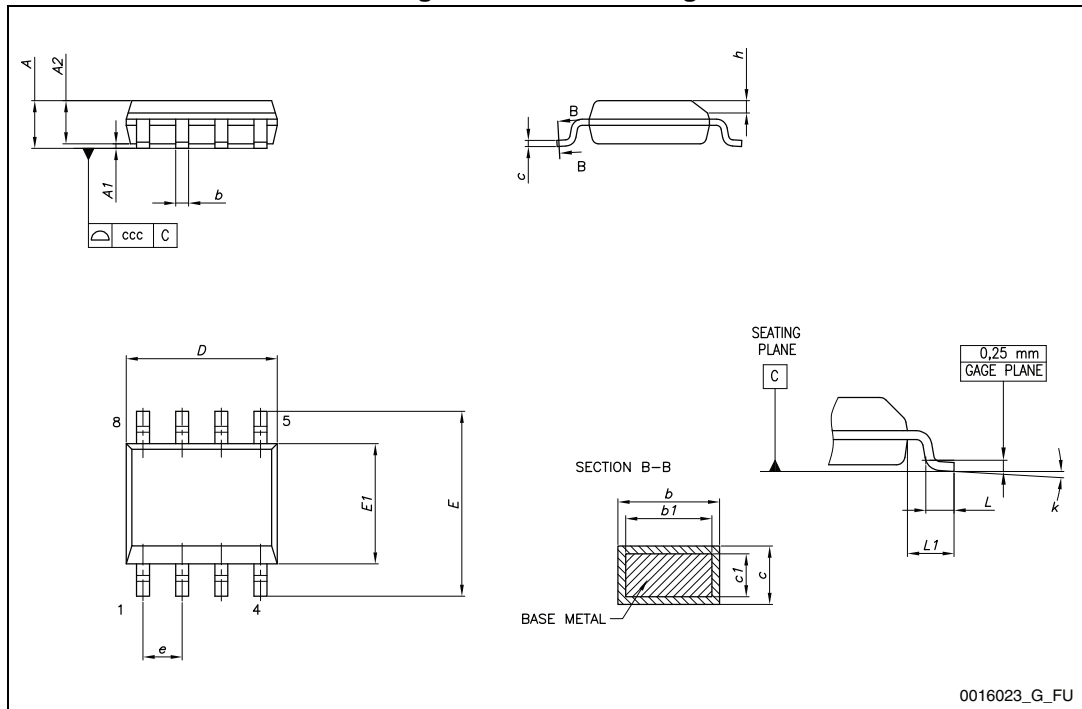
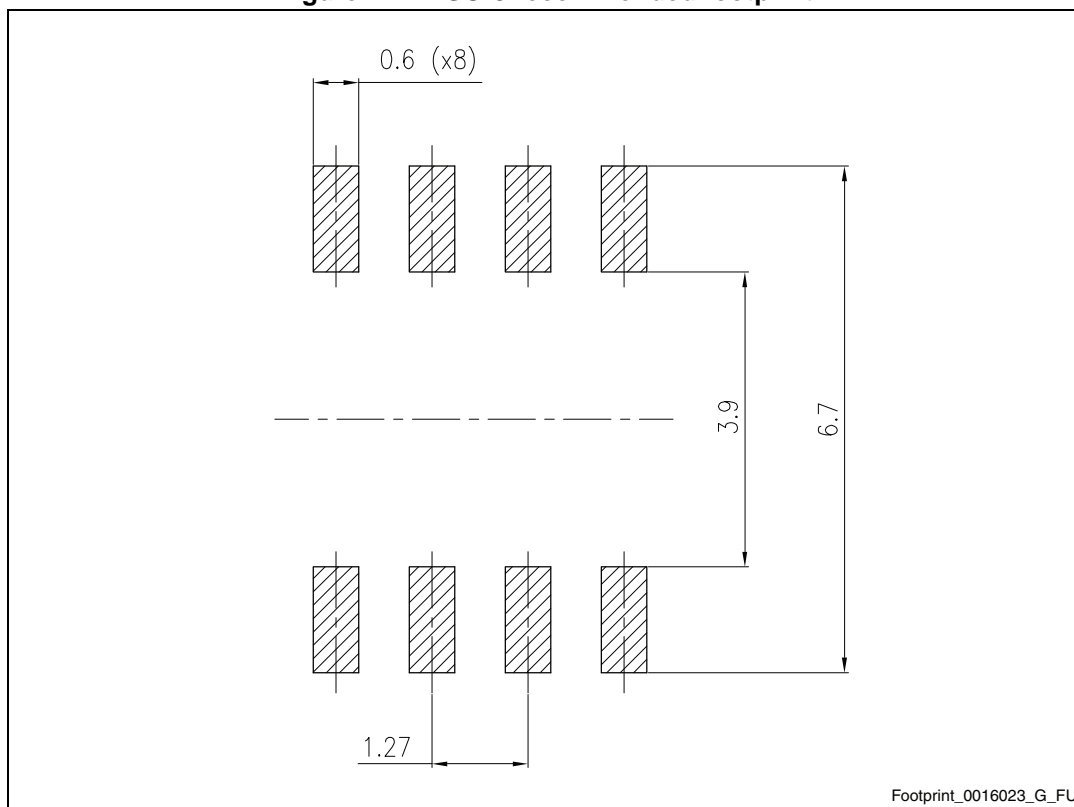


Table 8. SO-8 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
b1	0.28		0.48
c	0.10		0.25
c1	0.10		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
L2		0.25	
k	0°		8°
ccc			0.10

Figure 17. (a) SO-8 recommended footprint



a. All dimensions are in millimeters.

5 Packaging mechanical data

Figure 18. SO-8 tape and reel dimensions

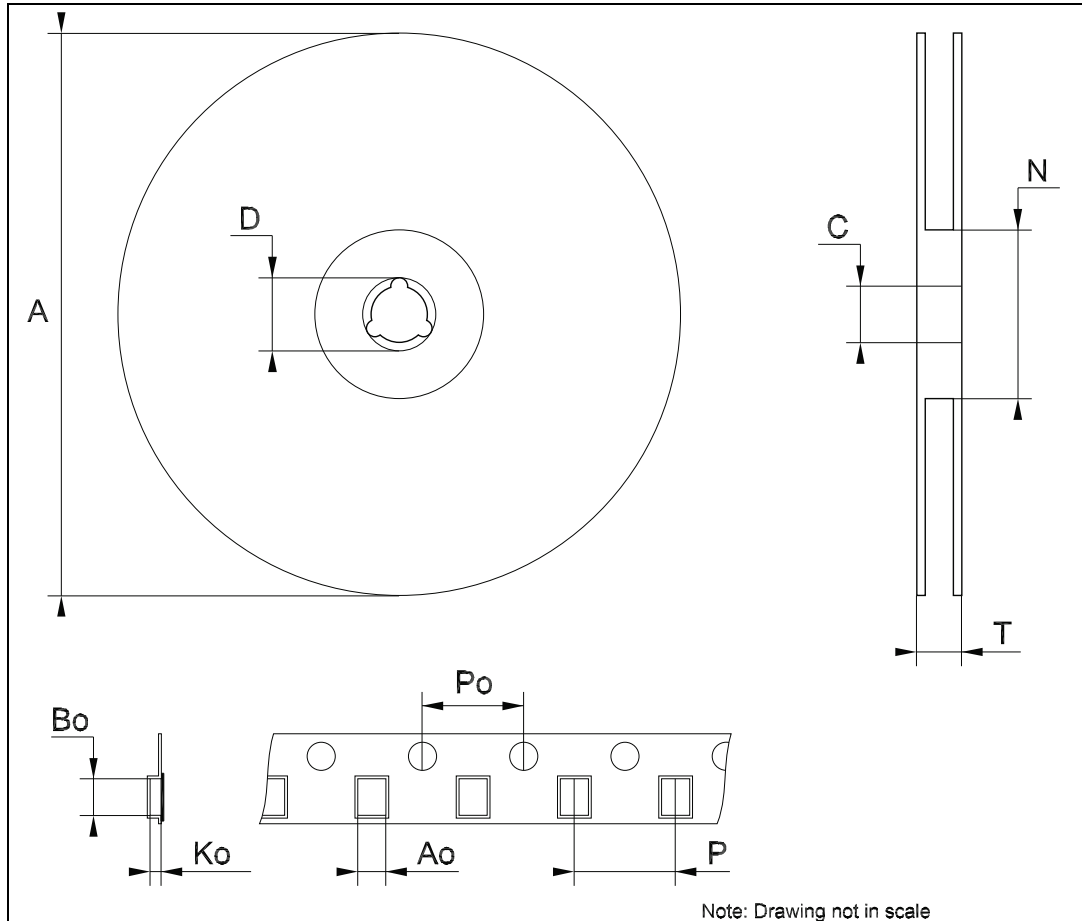


Table 9. SO-8 tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A		-	330
C	12.8	-	13.2
D	20.2	-	
N	60	-	
T		-	22.4
Ao	8.1	-	8.5
Bo	5.5	-	5.9
Ko	2.1	-	2.3
Po	3.9	-	4.1
P	7.9	-	8.1

6 Revision history

Table 10. Document revision history

Date	Revision	Changes
22-Mar-2013	1	First release.
14-Jul-2014	2	<ul style="list-style-type: none">– Modified: the entire typical values in Table 6– Modified: Section 3: Test circuits– Added: Section 2.1: Electrical characteristics (curves)– Minor text changes

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