



STS5NF60L

N-channel 60V - 0.045Ω - 5A - SO-8
STripFET™ Power MOSFET

General features

Type	V _{DSS}	R _{DS(on)}	I _D
STS5NF60L	60V	<0.055Ω	5A

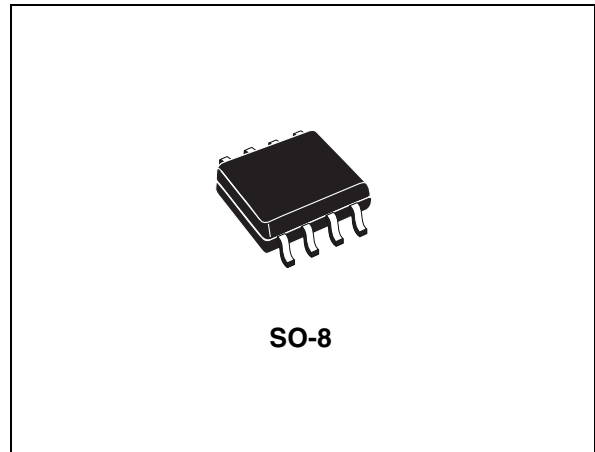
- Standard outline for easy automated surface mount assembly
- Low threshold drive

Description

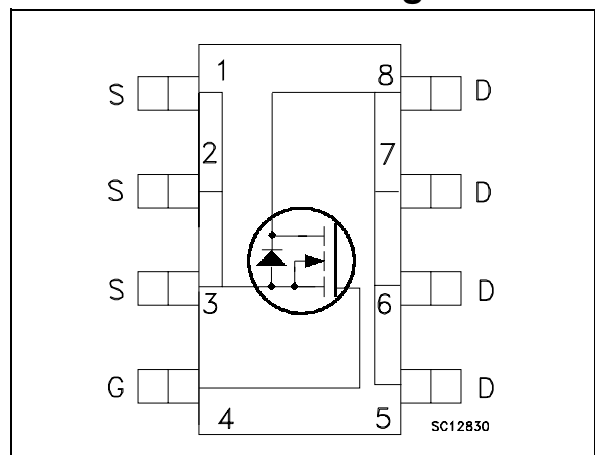
This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

Applications

- Switching application



Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STS5NF60L	S5NF60L	SO-8	Tape&reel

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($v_{GS} = 0$)	60	V
V_{GS}	Gate- source voltage	± 20	V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	5	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	3	A
$I_{DM}^{(1)}$	Drain current (pulsed)	20	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	2.5	W
	Derating factor	0.02	W/ $^\circ\text{C}$
$dv/dt^{(2)}$	Peak diode recovery voltage slope	5.5	V/ns
T_{stg}	Storage Temperature	-55 to 150	$^\circ\text{C}$
T_j	Max operating junction temperature	150	$^\circ\text{C}$

1. Pulse width limited by safe operating area

2. $I_{SD} \leq 5\text{A}$, $di/dt \leq 100\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$

Table 2. Thermal data

R_{thj-a}	⁽¹⁾ Thermal resistance junction-ambient Max	50	$^\circ\text{C}/\text{W}$
T_l	Maximum lead temperature for soldering purpose Typ	150	$^\circ\text{C}$

1. Mounted on FR-4 board (t 10 sec.).

2 Electrical characteristics

($T_{CASE}=25^{\circ}C$ unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	$I_D = 250 \mu A, V_{GS} = 0$	60			V
I_{DSS}	Zero gate voltage	$V_{DS} = \text{Max rating}$			1	μA
	Drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating},$ $T_C = 125^{\circ}C$			10	μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20V$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	1	1.7	2.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 2.5A$		0.045	0.055	Ω
		$V_{GS} = 4.5V, I_D = 2.5A$		0.050	0.065	Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15V, I_D = 2.5 A$		7		S
C_{iss}	Input capacitance	$V_{DS} = 25V, f = 1 \text{ MHz},$ $V_{GS} = 0$		1250		pF
C_{oss}	Output capacitance			130		pF
C_{rss}	Reverse transfer capacitance			26		pF
Q_g	Total gate charge	$V_{DD} = 48V, I_D = 5A,$ $V_{GS} = 5V$ (see Figure 13)		17		nC
Q_{gs}	Gate-source charge			4.5		nC
Q_{gd}	Gate-drain charge			6		nC

1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5.

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time	$V_{DD} = 30 V, I_D = 2.5A,$ $R_G = 4.7\Omega, V_{GS} = 4.5V$ (see Figure 12)		13		ns
	Rise time			28		ns
$t_{d(off)}$ t_f	Turn-off Delay Time		$V_{DD} = 30 V, I_D = 2.5A$ $R_G = 4.7\Omega, V_{GS} = 4.5V$ (see Figure 12)		45	
	Fall Time			10		ns

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				20	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 5A, V_{GS} = 0$			1.2	V
t_{rr}	Reverse recovery time	$I_{SD} = 5A, V_{DD} = 40V$ $di/dt = 100A/\mu s,$ $T_j = 150^\circ C$ (see Figure 14)		85		ns
Q_{rr}	Reverse recovery charge			85		nC
I_{RRM}	Reverse recovery current			2		A

1. Pulse width limited by safe operating area.

2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

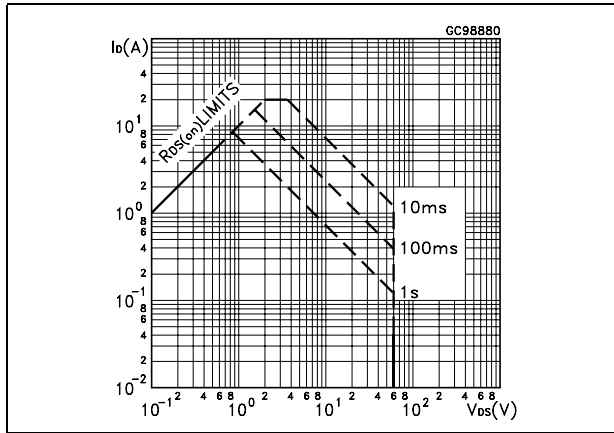


Figure 2. Thermal impedance

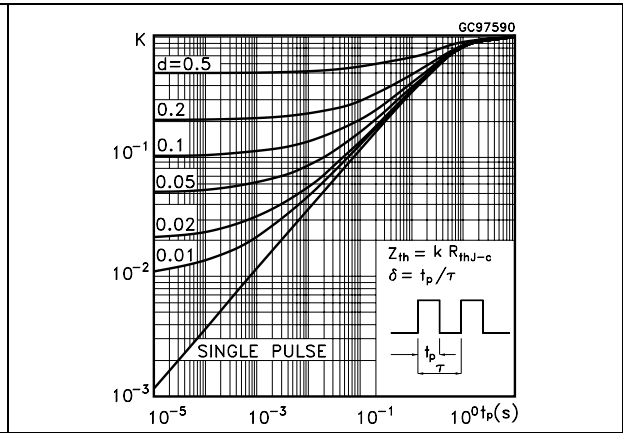


Figure 3. Output characteristics

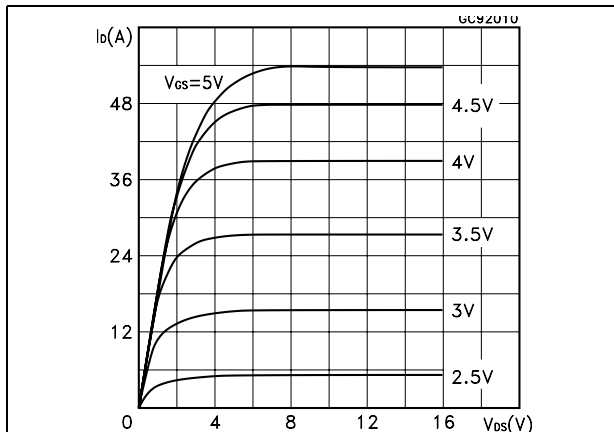


Figure 4. Transfer characteristics

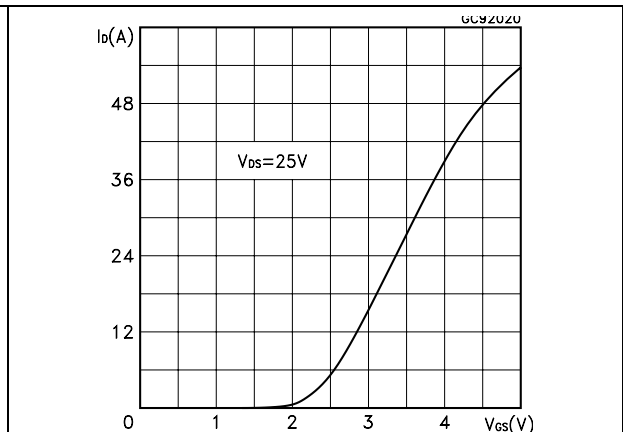


Figure 5. Transconductance

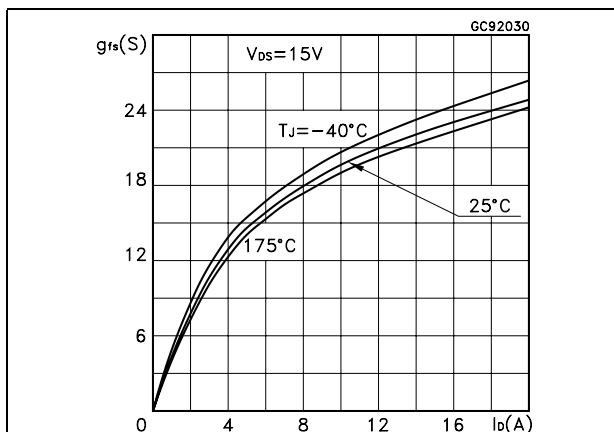


Figure 6. Static drain-source on resistance

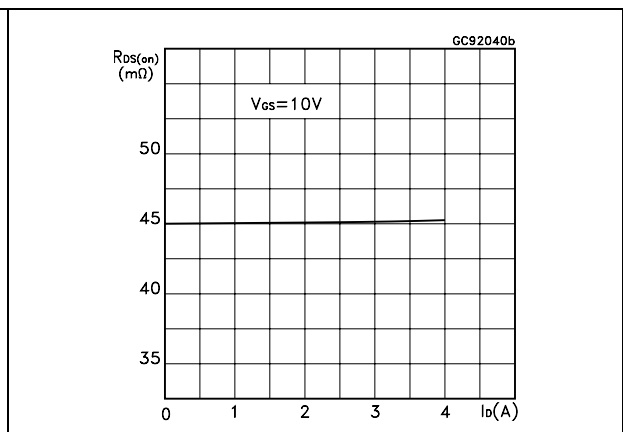


Figure 7. Gate charge vs. gate-source voltage Figure 8. Capacitance variations

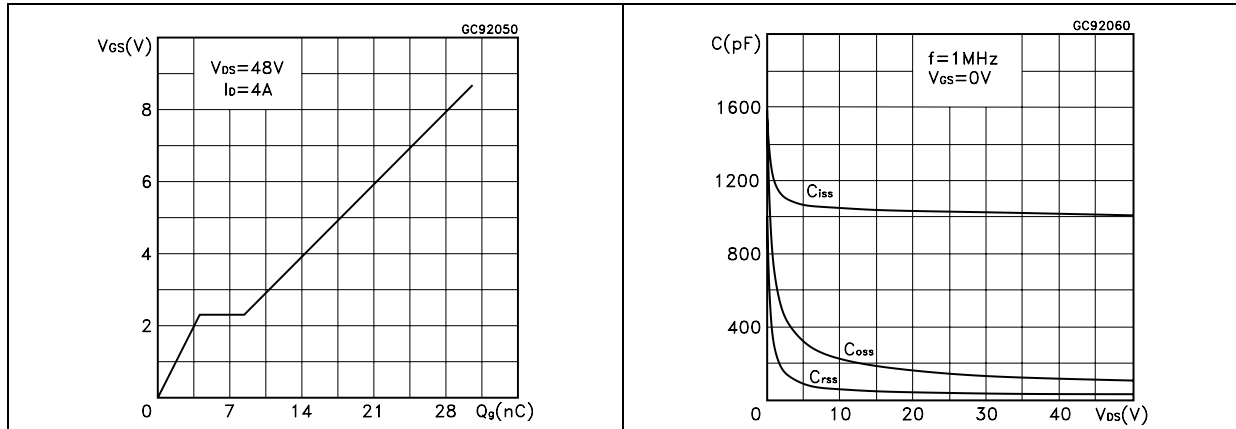


Figure 9. Normalized gate threshold voltage vs. temperature Figure 10. Normalized on resistance vs. temperature

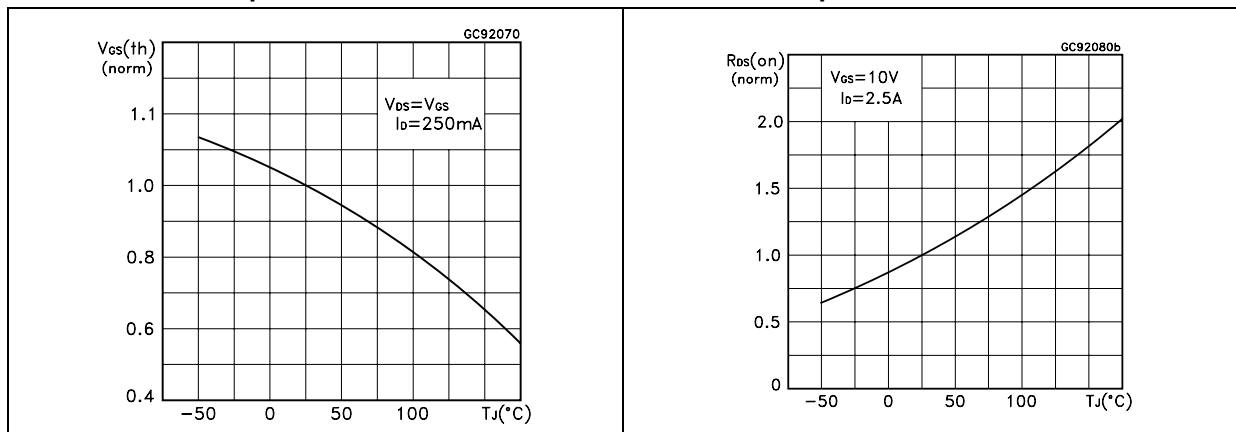
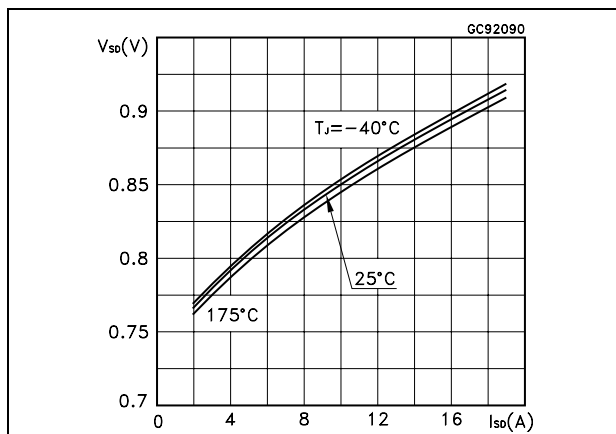


Figure 11. Source-drain diode forward characteristics



3 Test circuit

Figure 12. Switching times test circuit for resistive load

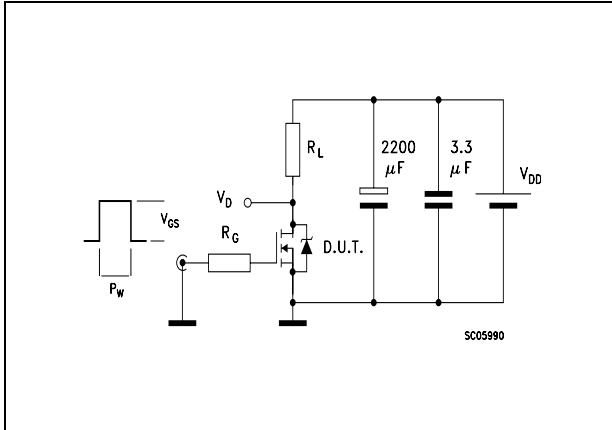


Figure 13. Gate charge test circuit

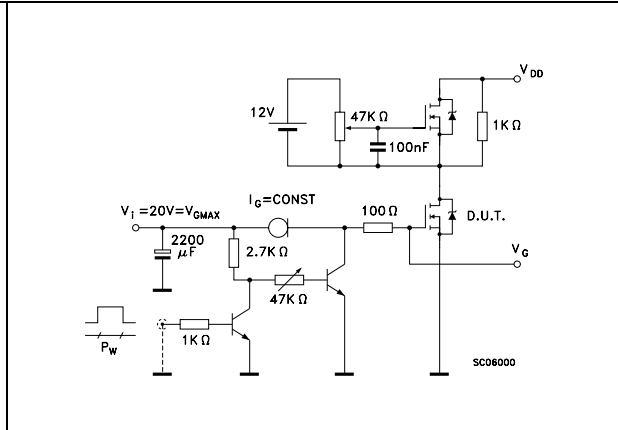


Figure 14. Test circuit for inductive load switching and diode recovery times

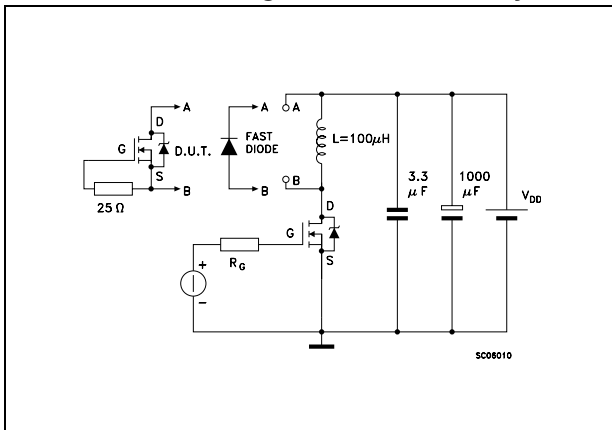


Figure 15. Unclamped Inductive load test circuit

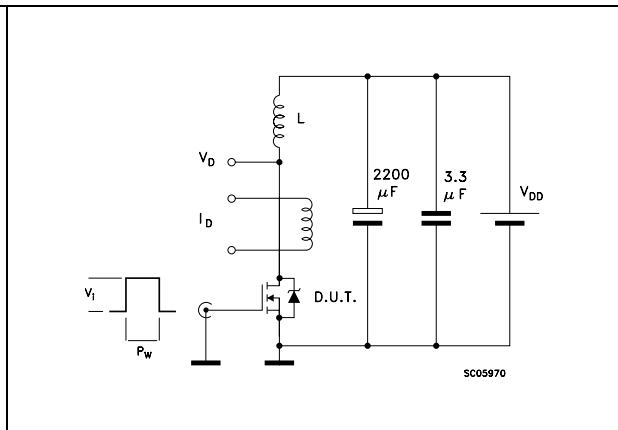


Figure 16. Unclamped inductive waveform

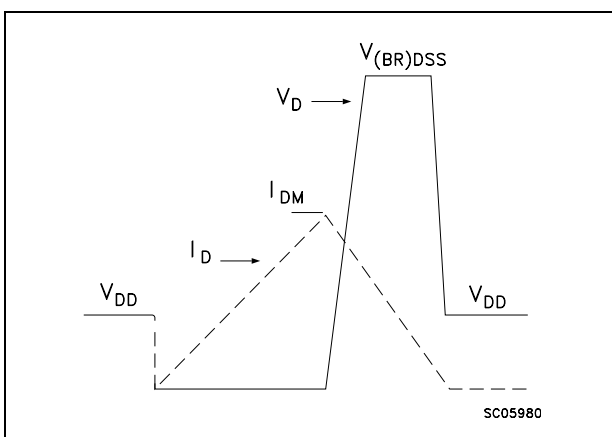
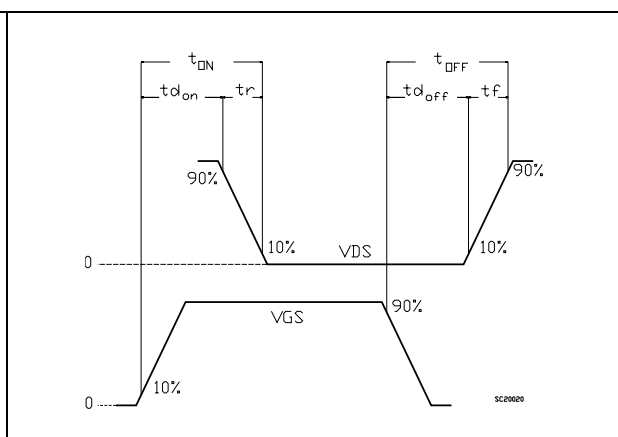


Figure 17. Switching time waveform

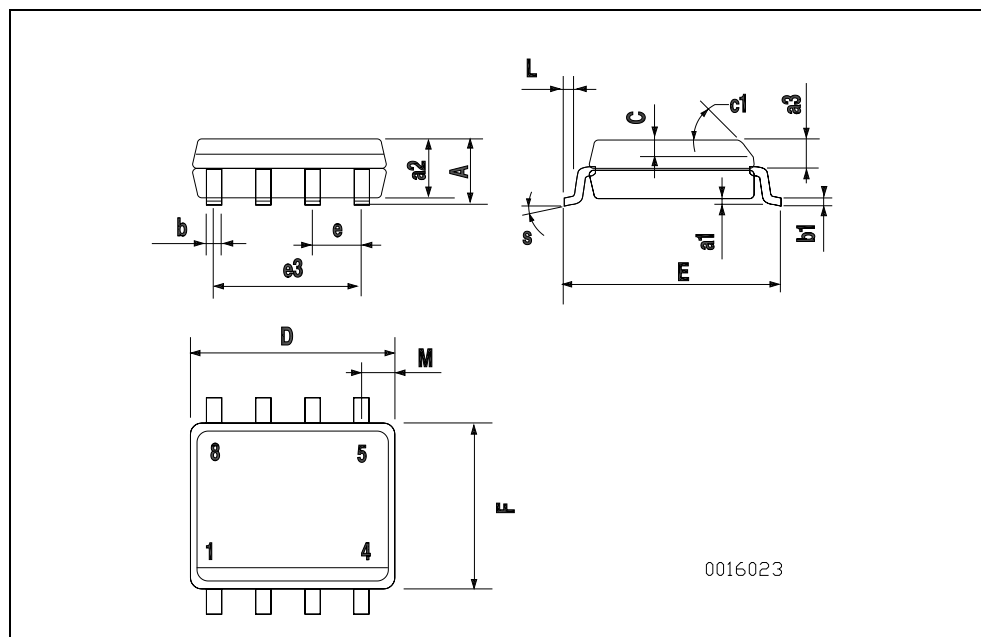


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at : www.st.com

SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



5 Revision history

Table 7. Revision history

Date	Revision	Changes
21-Jun-2004	2	First release
06-Nov-2006	3	The document has been reformatted
30-Jan-2007	4	Typo mistake on Table 1 .

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