STU12N60M2

N-channel 600 V, 0.395 Ω typ., 9 A MDmesh™ M2 Power MOSFET in an IPAK package

Datasheet - production data

IPAK
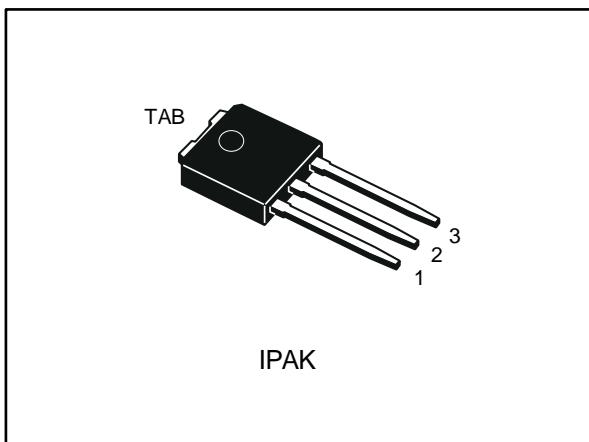
Figure 1: Internal schematic diagram

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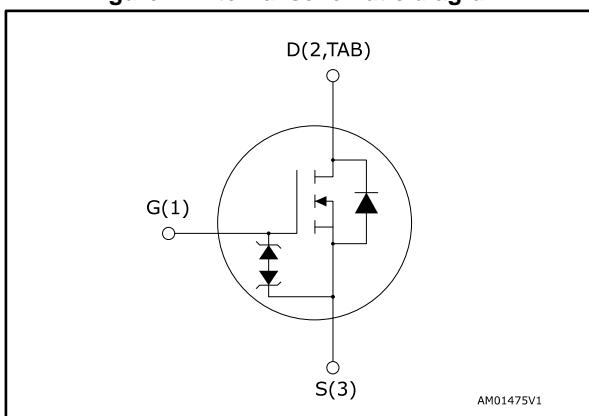
Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STU12N60M2	600 V	0.450 Ω	9 A	85 W

- Extremely low gate charge
- Excellent output capacitance (C_{OSS}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

Table 1: Device summary

Order code	Marking	Package	Packing
STU12N60M2	12N60M2	IPAK	Tube

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Contents

1   Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_{case} = 25 °C	9	A
	Drain current (continuous) at T_{case} = 100 °C	5.7	
I_{DM}[1]	Drain current (pulsed)	36	A
P_{TOT}	Total dissipation at T_{case} = 25 °C	85	W
dv/dt[2]	Peak diode recovery voltage slope	15	V/ns
dv/dt[3]	MOSFET dv/dt ruggedness	50	
T_{stg}	Storage temperature	-55 to 150	°C
T_j	Operating junction temperature		

Notes:

[1] Pulse width is limited by safe operating area.

[2] I_{SD} ≤ 9 A, di/dt=400 A/µs; $V_{DS(peak)}$ < $V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$.

[3] V_{DS} ≤ 480 V.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	1.47	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient	62.5	

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}[1]	Avalanche current, repetitive or not repetitive	2.6	A
E_{AR}[2]	Single pulse avalanche energy	117	mJ

Notes:

[1] Pulse width limited by T_{jmax}.

[2] starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V.

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 5: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			1	μA
		V_{GS} = 0 V, V_{DS} = 600 V, T_{case} = 125 °C			100	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±10	μA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 μA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 4.5 A		0.395	0.450	Ω

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	538	-	pF
C_{oss}	Output capacitance		-	29	-	
C_{rss}	Reverse transfer capacitance		-	1.1	-	
$C_{oss\ eq.}$ [(1)](#)	Equivalent output capacitance	V_{DS} = 0 to 480 V, V_{GS} = 0 V	-	106	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	7	-	Ω
Q_g	Total gate charge	V_{DD} = 400 V, I_D = 9 A, V_{GS} = 10 V (see *Figure 15: "Gate charge test circuit"*)	-	16	-	nC
Q_{gs}	Gate-source charge		-	2.3	-	
Q_{gd}	Gate-drain charge		-	8.5	-	

Notes:

[(1)] $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 4.5 A R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 14: "Switching times test circuit for resistive load"* and *Figure 19: "Switching time waveform"*)	-	9.2	-	ns
t_r	Rise time		-	9.2	-	
$t_{d(off)}$	Turn-off delay time		-	5	-	
t_f	Fall time		-	18	-	

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		9	A
I_{SDM}[(1)]	Source-drain current (pulsed)		-		36	A
V_{SD}[(2)]	Forward on voltage	V_{GS} = 0 V, I_{SD} = 9 A	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 9 A, di/dt = 100 A/µs, V_{DD} = 60 V (see *Figure 16: "Test circuit for inductive load switching and diode recovery times"*)	-	284		ns
Q_{rr}	Reverse recovery charge		-	2.4		µC
I_{RRM}	Reverse recovery current		-	17		A
t_{rr}	Reverse recovery time	I_{SD} = 9 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_j = 150 °C (see *Figure 16: "Test circuit for inductive load switching and diode recovery times"*)	-	404		ns
Q_{rr}	Reverse recovery charge		-	3.5		µC
I_{RRM}	Reverse recovery current		-	17.5		A

**Notes:**

[(1)] Pulse width is limited by safe operating area.

[(2)] Pulse test: pulse duration = 300 µs, duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area
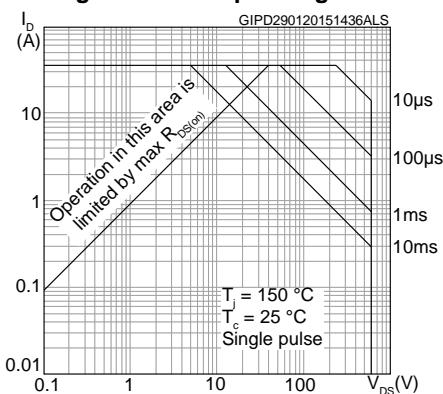
Figure 3: Thermal impedance
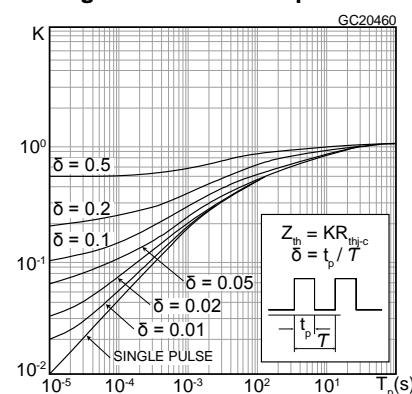
Figure 4: Output characteristics
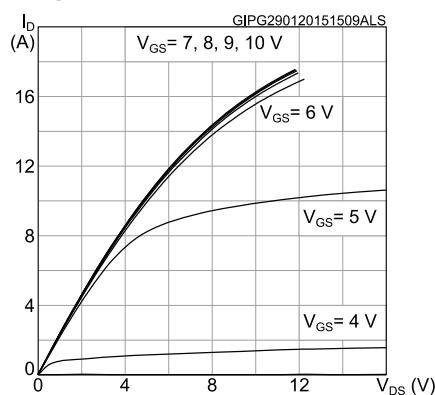
Figure 5: Transfer characteristics
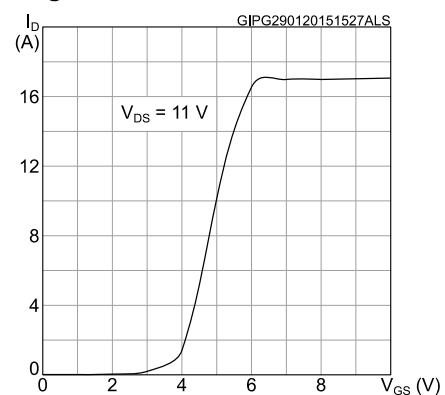
Figure 6: Gate charge vs gate-source voltage
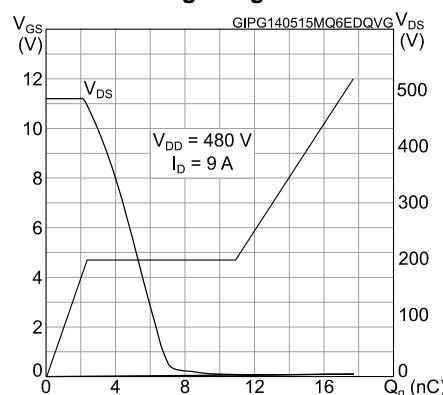
Figure 7: Static drain-source on-resistance
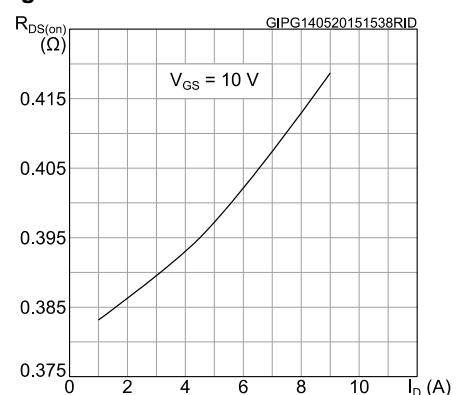
Figure 8: Capacitance variations
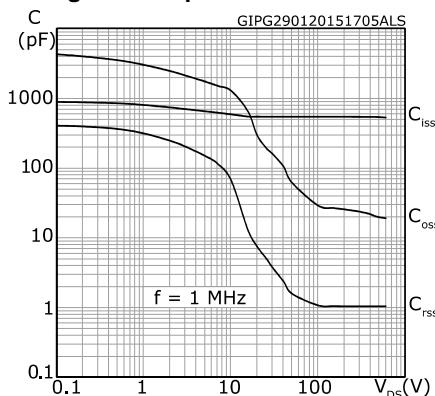
Figure 9: Normalized gate threshold voltage vs temperature
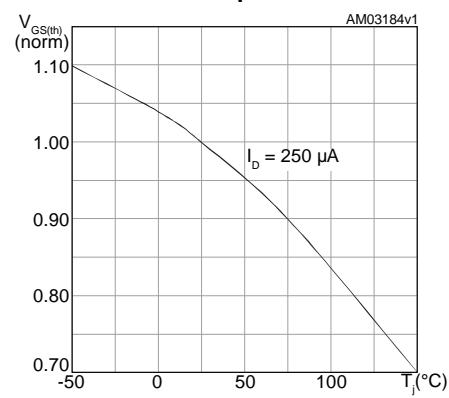
Figure 10: Normalized on-resistance vs temperature
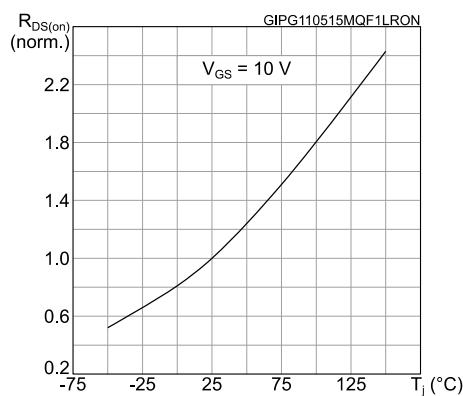
Figure 11: Normalized V(BR)DSS vs temperature
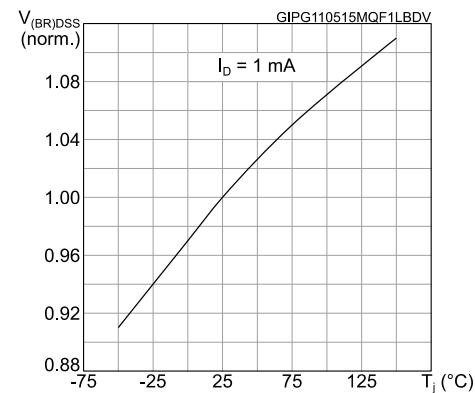
Figure 12: Output capacitance stored energy
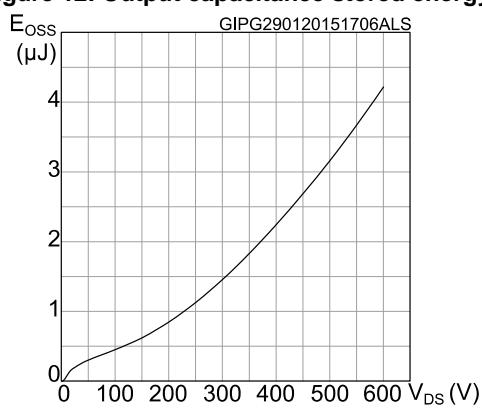
Figure 13: Source- drain diode forward characteristics
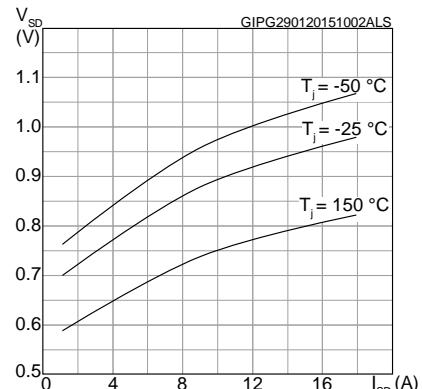
3 Test circuits

Figure 14: Switching times test circuit for resistive load
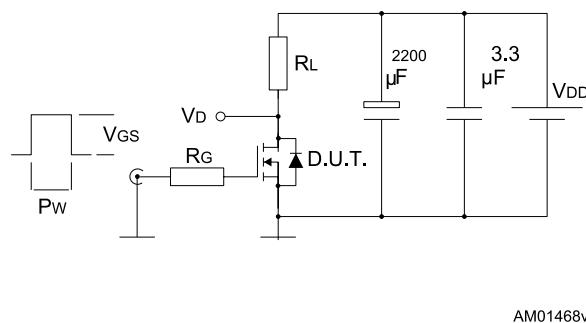
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Figure 15: Gate charge test circuit

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Figure 16: Test circuit for inductive load switching and diode recovery times

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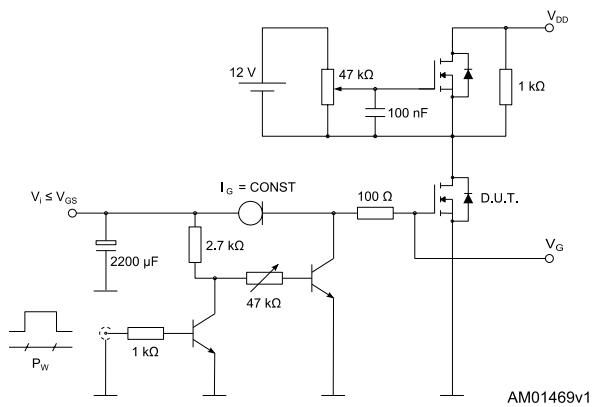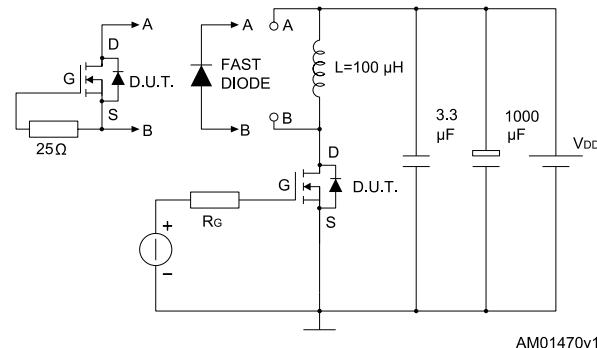
Figure 17: Unclamped inductive load test circuit

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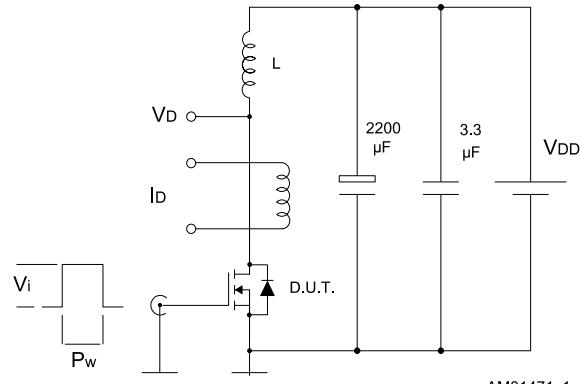
Figure 18: Unclamped inductive waveform

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Figure 19: Switching time waveform

AM01473v1
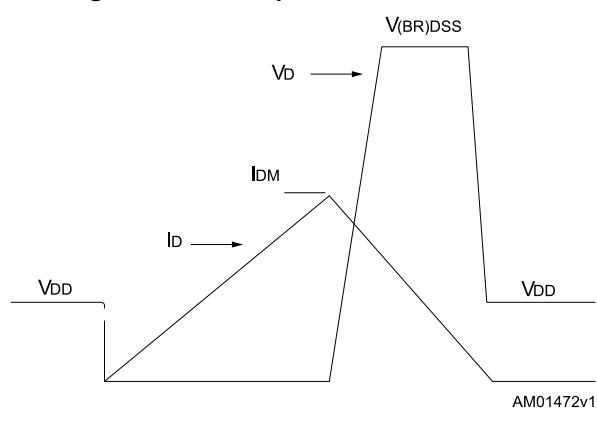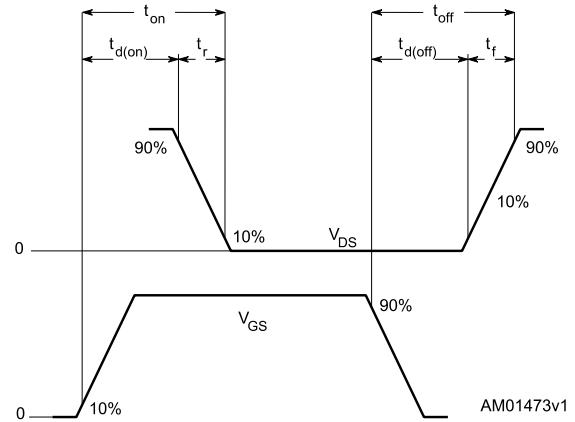
4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

4.1 IPAK (TO-251) Type A package information

**Figure 20: IPAK (TO-251) type A package outline**

0068771_IK_typeA_rev13
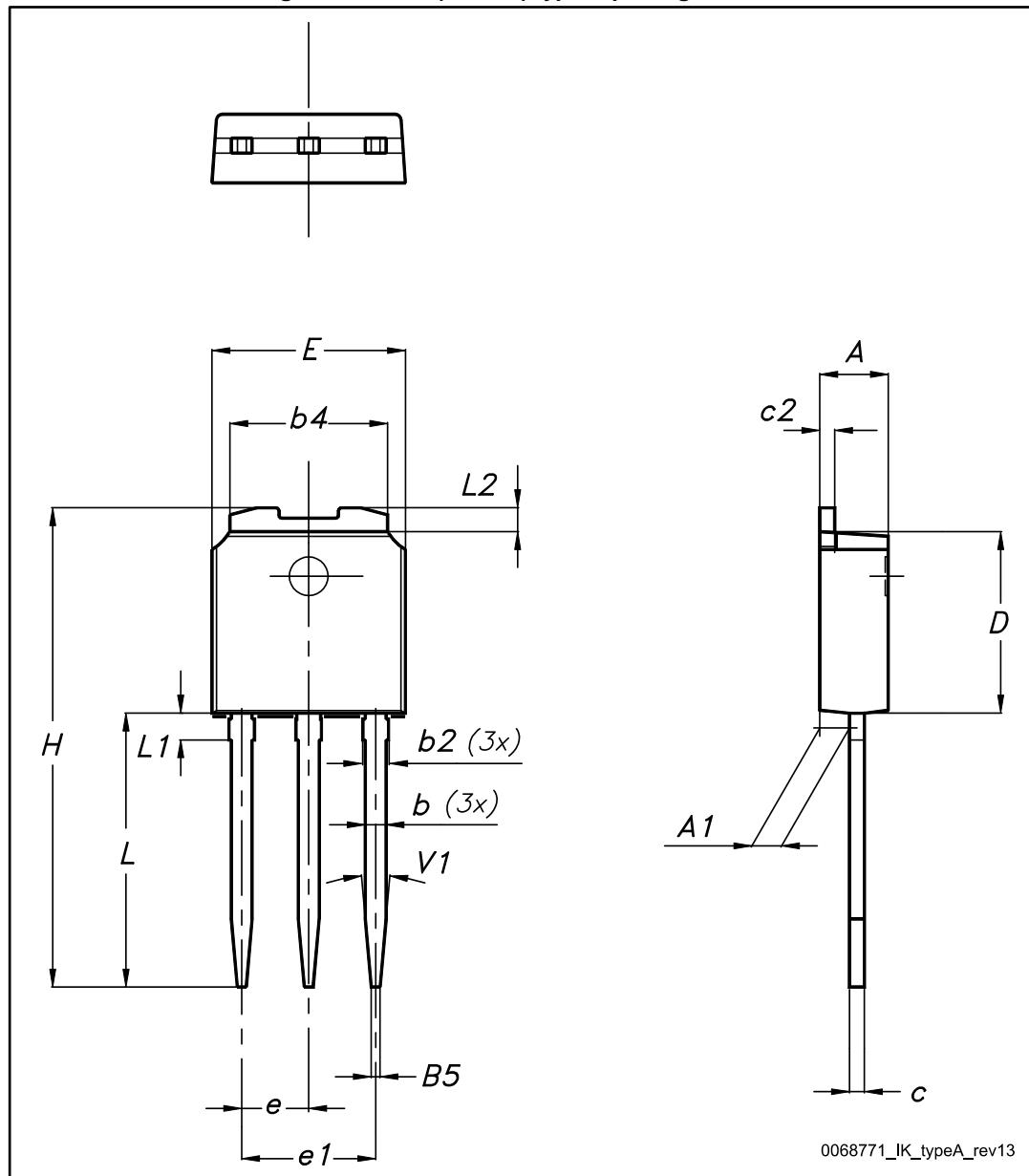
Table 9: IPAK (TO-251) type A package mechanical data

Dim.	mm		
	Min.	**Typ.**	**Max.**
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
22-May-2015	1	First release.

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