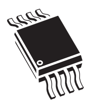
STVM100

I^2C LCD/e-paper VCOM calibrator

Datasheet - production data

TDFN8 (3 mm x 3 mm) (DC)



TSSOP8 (3 mm x 3 mm) (DS)

Features

- I^2C interface, slave address: 1001111
- 7-bit adjustable sink current output
- 2.25 V to 3.6 V logic supply voltage V_{DD}
- AV_{DD} operating voltages
  - 4.5 V to 20 V for V_{DD} from 2.6 V to 3.6 V
  - 4.5 V to 13 V for V_{DD} from 2.25 V to 3.6 V
- EEPROM for storing the optimum V_{COM} setting
- Guaranteed monotonic output over operating range
- 400 kHz maximum interface bus speed
- Operating temperature: –40 °C to 85 °C
- Available in an 8-pin 3 mm x 3 mm TDFN8 or 3 mm x 3 mm TSSOP8 package

Applications

- TFT-LCD panels
- e-paper and e-book displays

Description

The STVM100 is a programmable VCOM adjustment solution for thin-film transistor (TFT) liquid-crystal displays (LCDs) to remove “flickers”. It is also used in e-paper and e-book applications to avoid the “ghosting” effect (residual pixels after display refresh). It can replace a mechanical potentiometer, so that the factory operator can physically view the front screen when performing the VCOM adjustment. This significantly reduces labor costs, increases reliability, and enables automation.

The STVM100 provides a digital I^2C interface to control the sink current output (I_{OUT}). This output drives an external resistive voltage divider, which can then be applied to an external V_{COM} buffer. Three external resistors R_1, R_2, and R_{SET} determine the highest and lowest value of the V_{COM}. An increase in the output sink current will lower the voltage on the external divider so that the V_{COM} can be adjusted by 128 steps within this range. Once the desired V_{COM} setting is achieved, it can be stored in the internal EEPROM that will be automatically recalled during each power-up.

The STVM100 is available in an 8-pin, 3 mm x 3 mm TDFN8 or 3 mm x 3 mm TSSOP8 package.

Table 1. Device summary

Order code	Optimum temperature range	Package	Packing
STVM100DC6F	–40 °C to 85 °C	TDFN8	ECOPACK® package, tape and reel
STVM100DS6F	–40 °C to 85 °C	TSSOP8	ECOPACK® package, tape and reel

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1 Device overview

Figure 1. Logic diagram

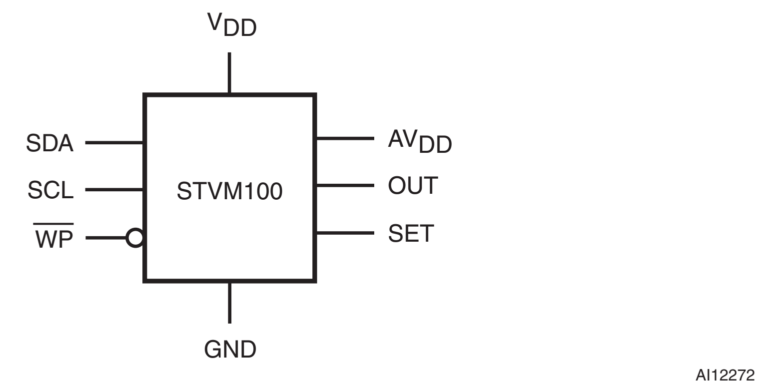


Table 2. Pin names and functions

Name	Type	Function
OUT	Analog	Adjustable sink current output pin. (1) See *Section 3: Application information on page 12*.
AV_{DD}	Supply	High-voltage analog supply. Bypass to GND with a 0.1 µF capacitor.
$\overline{WP}$	Input	WRITE protectection. Active-low. To enable write operations to the DAC or to the EEPROM writing, connect to 0.7 V_{DD} or greater. Internally pulled down by a 130 kΩ resistor.
GND		Supply ground.
V_{DD}	Supply	System power supply input. Bypass to GND with a 0.1 µF capacitor.
SDA	Input/Output	I^2C serial data input/output.
SCL	Input	I^2C serial clock input.
SET	Analog	Maximum sink current adjustment point. Connect a resistor from SET to GND to set the maximum adjustable sink current of the OUT pin. The maximum adjustable sink current is equal to AV_{DD} /20 divided by R_{SET} (see *Figure 4 on page 7*).

1. See SET pin function in this table for the maximum adjustable sink current setting.

Figure 2. Connections diagram

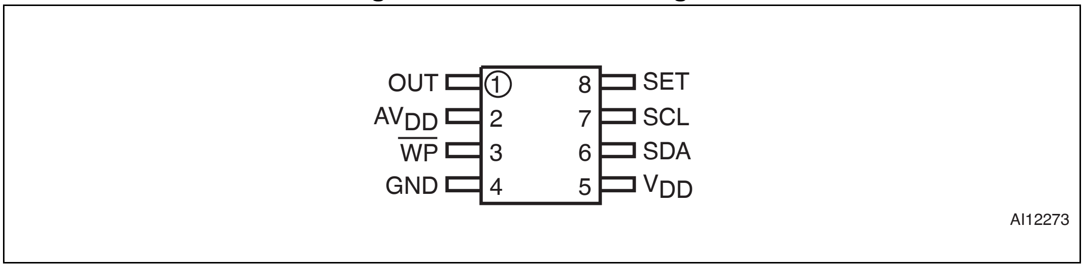


Figure 3. Block diagram

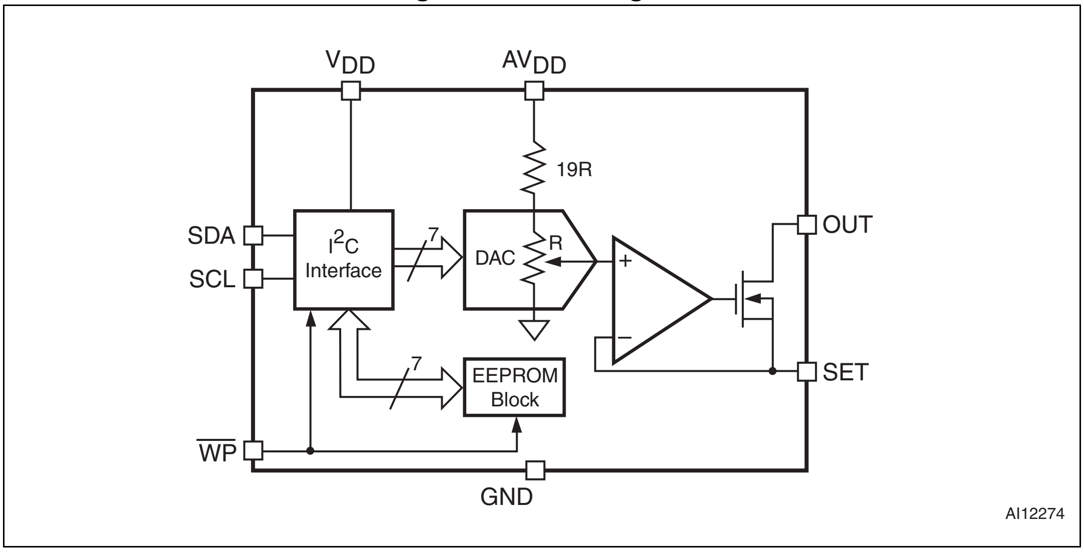
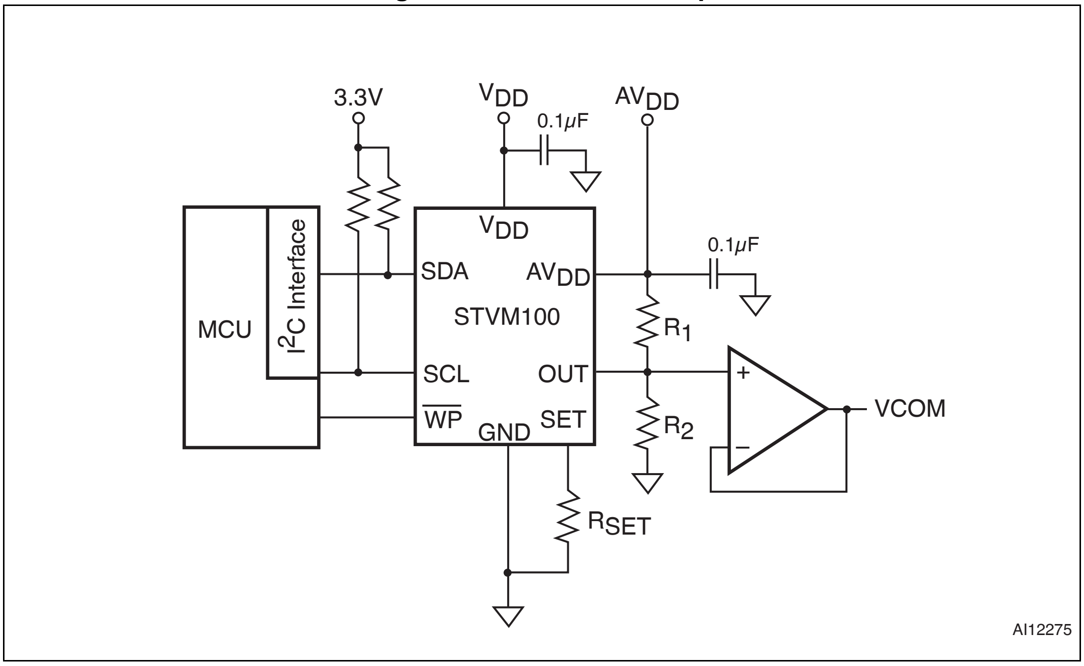


Figure 4. Hardware hookup



2 Device operation

The STVM100 operates as a slave device on the serial bus. Access is obtained by implementing a start condition, followed by the 7-bit slave address (1001111), and the eighth bit for READ/WRITE identification. The volatile DAC register and non-volatile EEPROM values can be read out or written in.

2.1 2-wire bus characteristics and conditions

This bus is intended for communication between different ICs. It consists of two lines:

- a bi-directional data signal (SDA).
- a clock signal (SCL).

The SDA and SCL lines must be connected to a positive supply voltage via a pull-up resistor. The following protocols have been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high.
- Changes in the data line while the clock line is high will be interpreted as control signals.

2.1.1 Bus not busy

Both data and clock lines remain high.

2.1.2 Start data transfer

A change in the data line state from high-to-low while the clock is high indicate the start condition.

2.1.3 Stop data transfer

A change in the data line state from low-to-high while the clock is high indicates the stop condition.

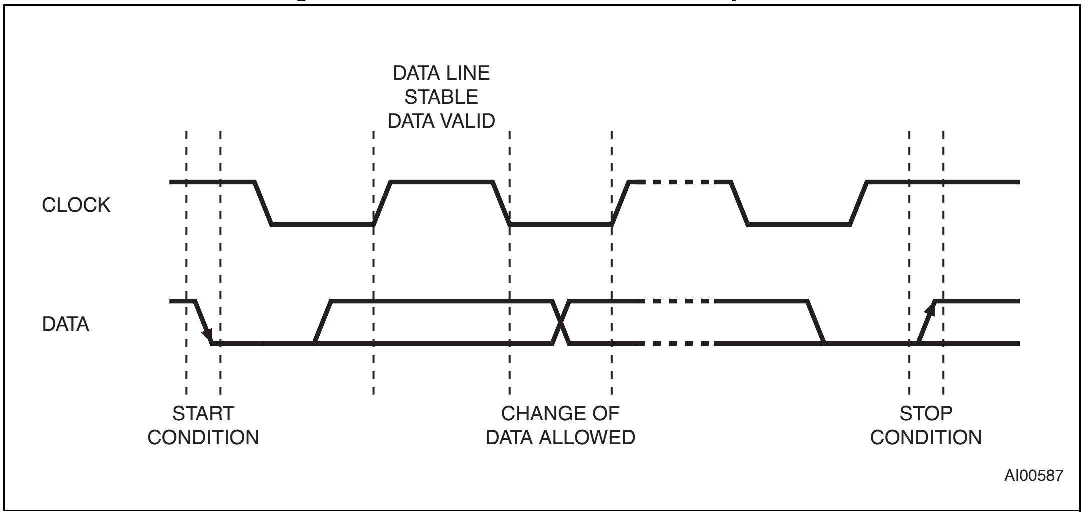
2.1.4 Data valid

The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the clock signal on the SCL line is low (see *Figure 5*). The data on the line may be changed during the clock signal low period. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition. The number of data bytes transferred between the start and stop conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges transmission with a ninth bit.

By definition, the device that gives out a message is called “transmitter”, the device that gets the message is called “receiver”. The device that controls the message is called the “master”. The devices controlled by the master are called “slave” devices.

Figure 5. Serial bus data transfer sequence

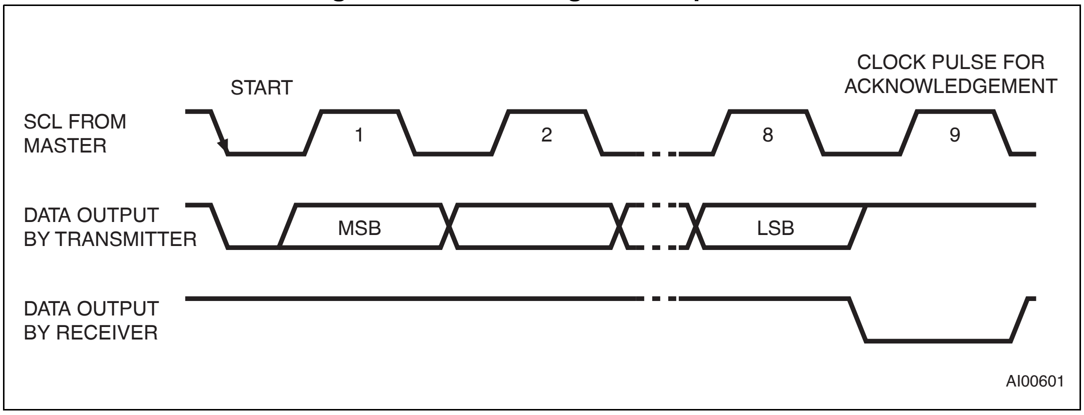


2.1.5 Acknowledge

Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level signal put on the bus by the receiver, whereas the master generates an extra acknowledge-related clock pulse (see *Figure 6*). A slave receiver which is addressed is obliged to generate an acknowledge signal after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges transmissions has to pull down the SDA line during the acknowledge clock pulse in such a way, that the SDA line is a stable low during the high period of the acknowledge-related clock pulse. The setup and hold times must be taken into account. A master receiver must signal an end of transmitted data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case, the transmitter must leave the data line high to enable the master to generate the stop condition.

Figure 6. Acknowledgment sequence



2.2 Read mode

In READ mode, after the start condition, the master sets the slave address (see *Figure 7*). Followed by the READ/WRITE mode control bit ($R/\overline{W}$=1) and the acknowledge bit, the value in DAC register will be transmitted and the master receiver will send an acknowledge bit to the slave transmitter. Finally the stop condition will terminate the READ operation. In READ mode, the valid data is the first 7 bits and the P bit (the eight bit) is don't care.

2.3 Write mode

In WRITE mode the master transmits to the STVM100 slave receiver. The bus protocol is shown in *Figure 7*. Following the start condition and slave address, a logic '0' ($R/\overline{W}$ = 0) is placed on the bus to identify a WRITE operation. After the acknowledgement by the slave, the data will be transmitted to the slave with the 7-bit which indicates the data is valid as well as the eighth bit "P" for the register's identification. When P = 1, the DAC register is written to, and when P = 0, the EEPROM is written to (**P**rogramming). After receiving the data, the slave will generate an acknowledge signal, then a stop condition will terminate the WRITE operation. STVM100 is pre-programmed with 80H in the EEPROM after manufacturing.

A period of t_W (see *Table 8*) is needed for EEPROM programming. During this period, the slave will not acknowledge any WRITE operation.

The bit P values in both READ and WRITE modes are shown in *Table 3*.

Figure 7. Read/write mode sequence

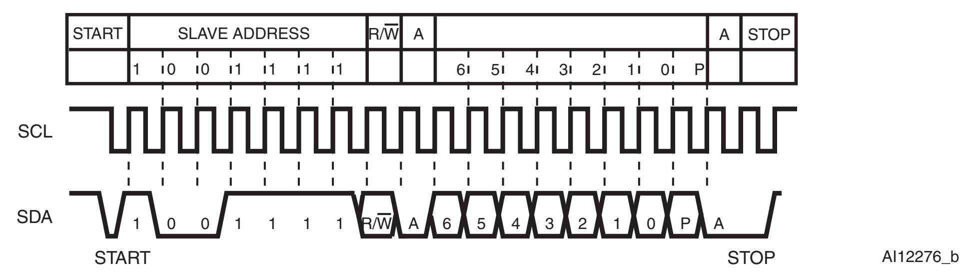


Table 3. Bit P read and write mode values

Operation	P-bit value	Description
READ	X	Don't care
WRITE	1	DAC register WRITE
	0	EEPROM WRITE (programming)

2.4 V_{DD} power supply ramp-up

The ramp-up from 10% V_{DD} to 90% V_{DD} level should be achieved in less than or equal to 10ms to ensure that the EEPROM and power-on reset circuits are synchronized, and the correct value is read from the EEPROM.

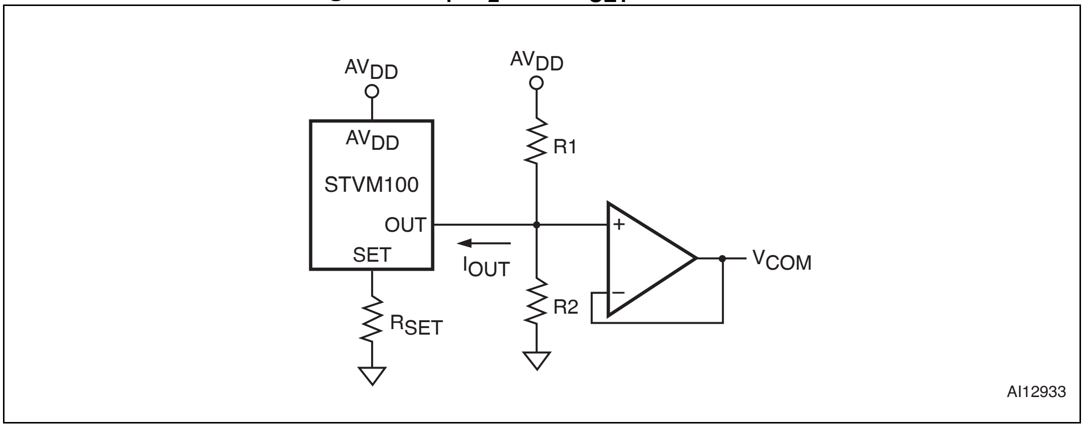
3 Application information

The STVM100 is a programmable V_{COM} calibrator to remove flickers in TFT-LCDs or to avoid the “ghosting effect” (residual pixels during refresh) in e-paper and e-books. It provides a digital I^2C interface to control the sink current output. This output drives an external resistive voltage divider, which can then be applied to an external V_{COM} buffer.

The highest and lowest V_{COM} value is determined by three resistors, R_1, R_2, and R_{SET}. The connection is shown in *Figure 8*.

The sink current from the STVM100 OUT pin is given in *Equation 1*. This current then flows through R_{SET}. This current must be less than 120 µA (see I_{SET} value in *Table 7 on page 16*).

Figure 8. R_1, R_2, and R_{SET} connection



Note: In order to choose an appropriate device to buffer the output of STVM100, please see our operational amplifier product portfolio available at:
http://www.st.com/stonline/products/families/amplifiers_comparators/amplifiers_comparators.htm

Equation 1

$$I_{OUT} = \frac{D+1}{128} \cdot \frac{AV_{DD}}{20(R_{SET})}$$

Note: “D” is a user-selected value, an integer ranging from 0 to 127.

The V_{COM} value can be obtained in *Equation 2*.

Equation 2

$$V_{COM} = \frac{R_2}{R_1 + R_2} \cdot AV_{DD}\left(1 - \frac{D+1}{128} \cdot \frac{R_1}{20(R_{SET})}\right)$$

If the user-selected value is 0 (zero scale), the minimum current is sunk. The maximum V_{COM} value is obtained in *Equation 3*.

Equation 3

$$V_{COM(max)} = \frac{R_2}{R_1 + R_2} \cdot AV_{DD}\left(1 - \frac{1}{128} \cdot \frac{R_1}{20(R_{SET})}\right)$$

If the user-selected value is 127 (full scale), the maximum current is sunk and the minimum V_{COM} value is obtained in *Equation 4*.

Equation 4

$$V_{COM(min)} = \frac{R_2}{R_1 + R_2} \cdot AV_{DD}\left(1 - \frac{R_1}{20(R_{SET})}\right)$$

During operation, the $V_{COM(max)}$ and $V_{COM(min)}$ range is set, based on different TFT-LCD processes.The R1 value is given based on the acceptable power loss from the AV_{DD} supply rail. Using *Equation 3* and *Equation 4*, the R_2 and R_{SET} values can be calculated. If R_{SET} is put into *Equation 1 on page 12* and maximum $I_{OUT} \geq 120\ \mu A$, then R_1 should be increased.

4 Maximum ratings

Stressing the device above the ratings listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 4. Absolute maximum ratings

Symbol	Parameter		Value	Unit
T_{STG}	Storage temperature (V_{DD} off, AV_{DD} off)		–55 to 150	°C
T_{SLD}[(1)]	Lead solder temperature for 10 seconds		260	°C
T_J	Maximum junction temperature (plastic package)		150	°C
V_{OUT}	Output voltage (OUT pin to GND)		–0.3 to 20	V
V_{DD}	V_{DD} to GND		+5.5	V
AV_{DD}	AV_{DD} input voltage to GND		–0.3 to 20	V
V_{SET}	Output voltage (SET pin to GND)		–0.3 to 5.5	V
P_{DIS}	Power dissipation	TDFN8	2.66	W
		TSSOP8	0.53	W

1. Reflow at peak temperature of 260 °C. The time above 255 °C must not exceed 30 seconds.

5 DC and AC parameters

This section summarizes the operating measurement conditions, and the dc and ac characteristics of the device. The parameters in the DC and AC characteristics tables that follow, are derived from tests performed under the measurement conditions summarized in *Table 5*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 5. Operating and AC measurement conditions

Parameter	Conditions	Unit
V_{DD} supply voltage	2.25 to 3.6	V
V_{DD} EEPROM programming supply voltage	2.25 to 3.6	V
AV_{DD} reference voltage	4.5 to 20	V
Ambient operating temperature (T_A)	–40 to 85	°C

Table 6. Capacitances

Symbol	Parameter(1)(2)		Min	Max	Unit
C_b	Bus capacitive load			400	pF
C_{SDA}	Capacitance on SDA			10	pF
C_S	Capacitance on SCL	WP = 0		10	pF
		WP = 1		22	pF

1. Effective capacitance measured with power supply at 3 V. Sampled only, not 100% tested.
2. At 25 °C, f = 1 MHz.

Table 7. DC and AC characteristics

Sym	Description	Test condition(1)	Min	Typ	Max	Unit
V_{DD}	Supply voltage		2.25		3.6	V
	EEPROM programming supply voltage		2.25		3.6	V
I_{DD}(2)	V_{DD} supply current				50	µA
AV_{DD}	Analog supply voltage	V_{DD} = 2.6 V to 3.6 V	4.5		20	V
		V_{DD} = 2.25 V to 3.6 V	4.5		13	V
I_{AVDD}(3)	AV_{DD} supply current				25	µA
SET_{VR}	SET voltage resolution			7		Bits
SET_{DN}	SET differential nonlinearity	Monotonic over temperature			±1	LSB
SET_{ZSE}	SET zero scale error				±2	LSB
SET_{FSE}	SET full scale error				±8	LSB
I_{SET}(4)	SET current	Through R_{SET}			120	µA
SET_{ER}	SET external resistance	To GND, AV_{DD} = 20 V	10		200	kΩ
		To GND, AV_{DD} = 4.5 V	2.25		45	kΩ
AV_{DD} to SET	AV_{DD} to SET voltage attenuation(5)			20		V/V
OUT_{ST}	OUT settling time			8		µs
V_{OUT}	OUT voltage		V_{SET} + 0.5V		13	V
SET_{VD}	SET voltage drift(5)	T = 25 °C to 55 °C		<10		mV
V_{IH}	SDA, SCL, $\overline{WP}$ input logic high		0.7 V_{DD}			V
V_{IL}	SDA, SCL, $\overline{WP}$ input logic low				0.3V_{DD}	V
	SDA, SCL hysteresis(5)			0.22 V_{DD}		V
$I_{IL(WPN)}$	WP_N input current		15	25	35	µA
$V_{OL(s)}$	SDA, SCL output logic low	At 3 mA			0.4	V

1. Valid for ambient operating temperature: T_A = –40 to 85 °C; V_{DD} = 3 V; AV_{DD} = 10 V; typical T_A = 25 °C; OUT = 1/2AV_{DD}; R_{SET} = 24.9 kΩ (except where noted).
2. Simulated maximum current draw when Programming EEPROM is 23 mA; should be considered when designing a power supply.
3. Tested at AV_{DD} = 20 V.
4. A typical Current of 20 µA is calculated using AV_{DD} = 10 V and R_{SET} = 24.9 kΩ. The maximum suggested SET current should be 120 µA.
5. Simulated and determined via design and NOT directly tested.

Figure 9. Bus timing requirements sequence

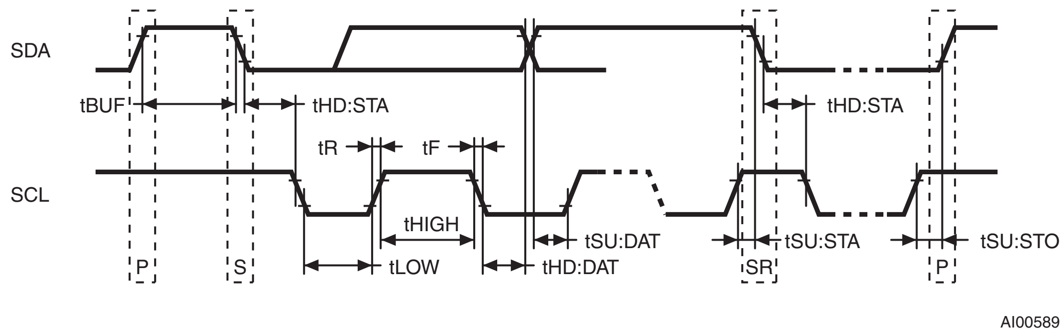


Table 8. AC characteristics

Sym	Description	Test Condition[1]	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency		0		400	kHz
t_{LOW}	Clock low period		1.3			µs
t_{HIGH}	Clock high period		0.6			µs
$t_{SU:DAT}$	Data setup time		100			ns
$t_{HD:DAT}$	Data hold time		0		900	ns
t_R	SDA and SCL rise time	Dependent on load (see Table 6 on page 15)		20 + 0.1 C_b	300	ns
t_F	SDA and SCL fall time				300	ns
t_{BUF}	Bus free time before new transmission can start		1.3			µs
t_{DSP}	I^2C spike rejection filter pulse width		0		50	ns
$t_{SU:STA}$	Repeated start condition setup time		0.6			µs
$t_{HD:STA}$	Repeated start condition hold time		0.6			µs
$t_{SU:STO}$	Stop condition setup time		0.6			µs
t_W	WRITE cycle time				100	ms

1. Valid for ambient operating temperature: T_A = –40 to 85 °C; V_{DD} = 3.0 V to 3.6 V; AV_{DD} = 10 V; OUT = 1/2AV_{DD}; R_{SET} = 24.9 kΩ (except where noted, see Figure 9).

6 Typical operating characteristics

Typical operating characteristics for the STVM100 are T_A = 25 °C, V_{DD} = 3 V, AV_{DD} = 10 V, OUT = 1/2AV_{DD}, and R_{SET} = 24.9 kΩ except where noted.

Figure 10. V_{DD} supply current vs. V_{DD}

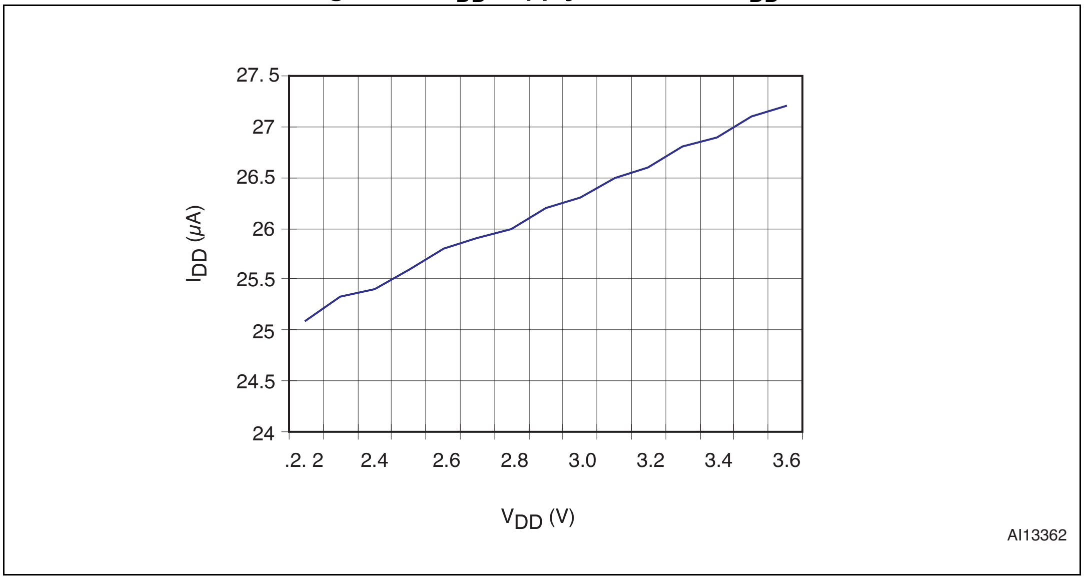


Figure 11. AV_{DD} supply current vs. AV_{DD}

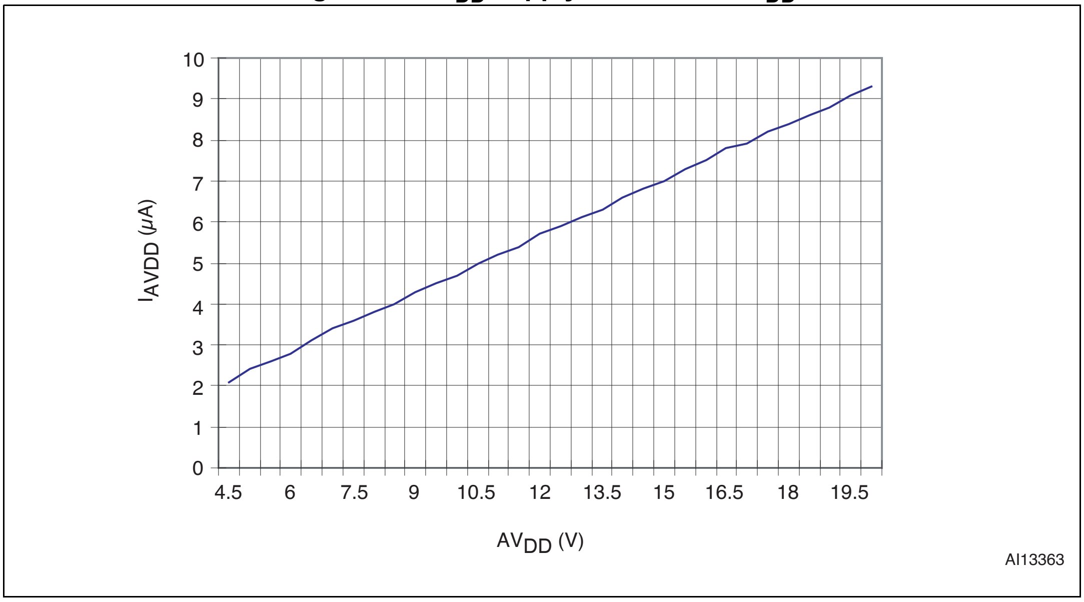


Figure 12. V_{DD} supply current vs. temperature

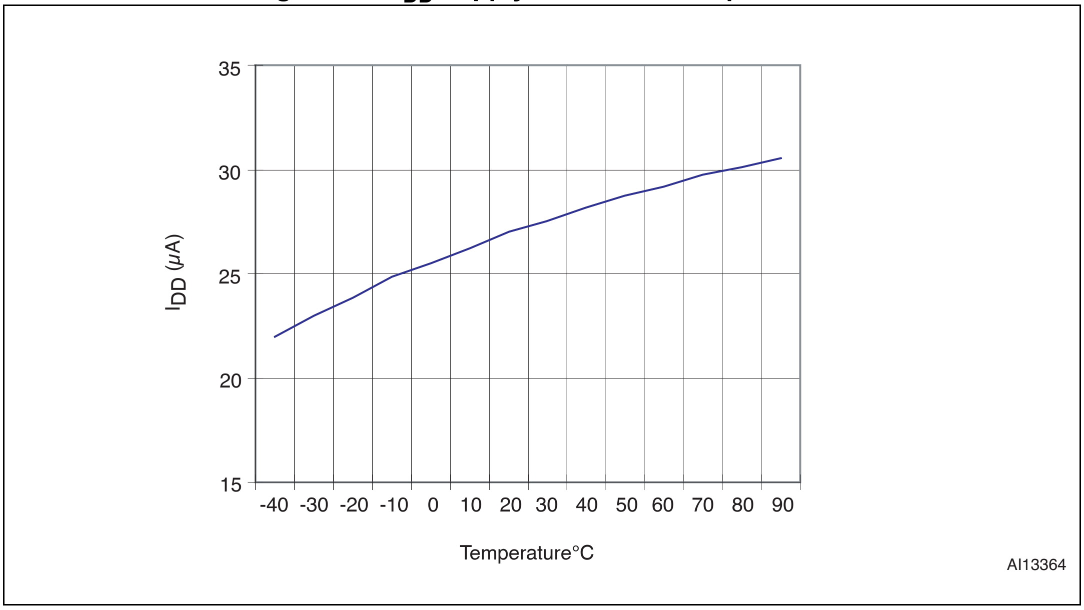


Figure 13. AV_{DD} supply current vs. temperature

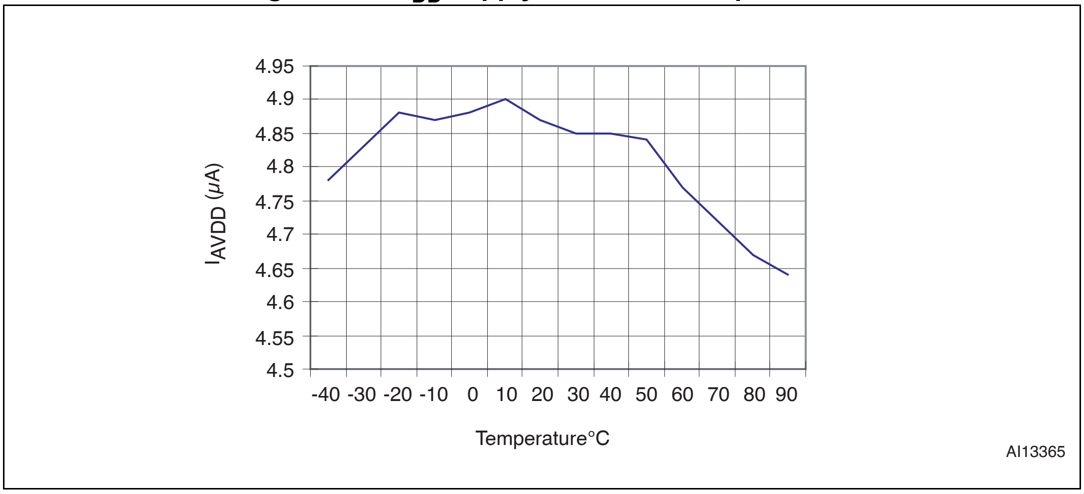


Figure 14. I_{OUT} error vs. temperature (STVM100 at middle scale)

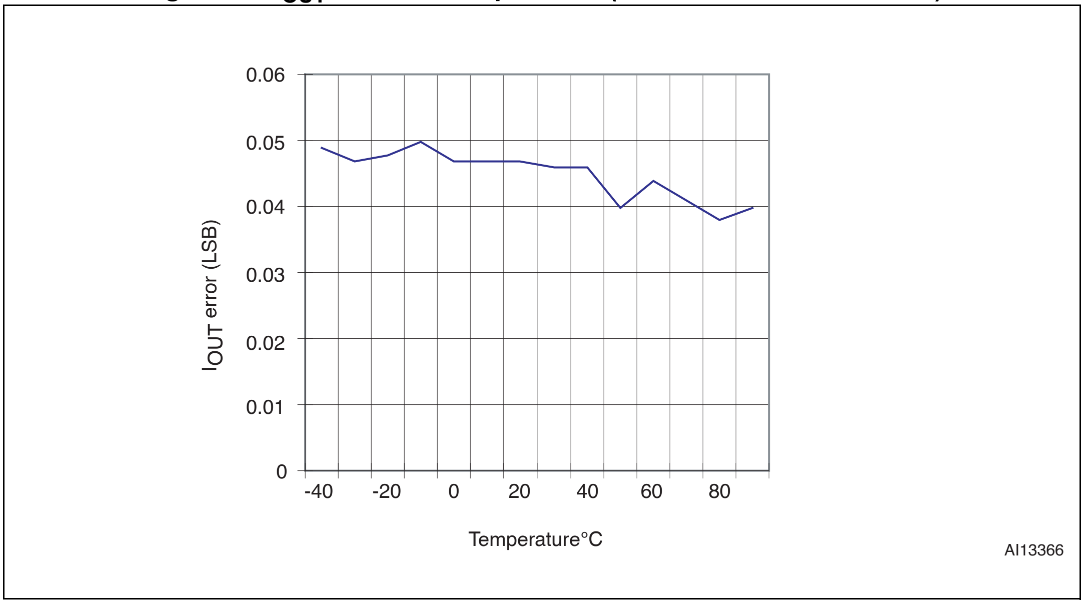


Figure 15. Total unadjusted error vs. DAC setting

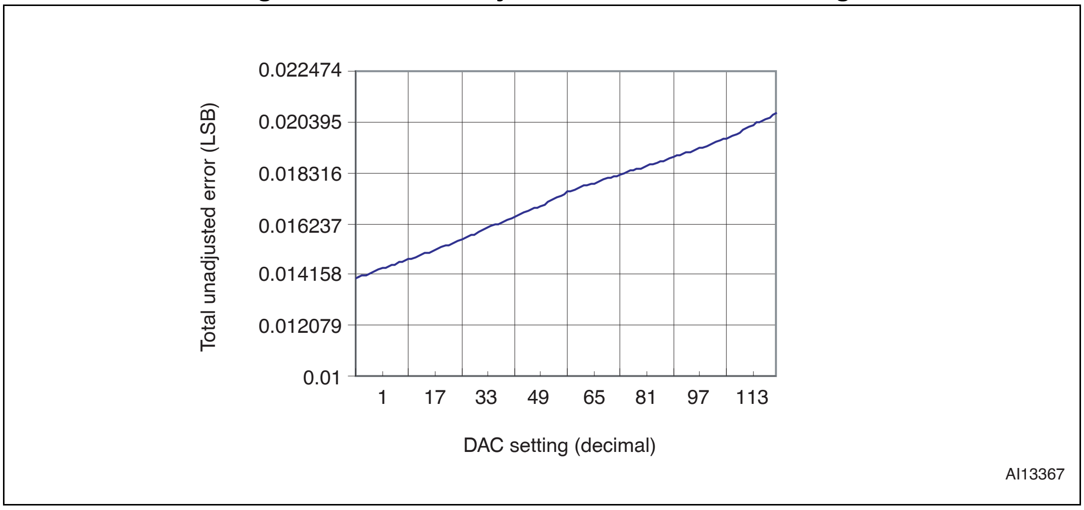


Figure 16. Differential non-linearity vs. DAC setting

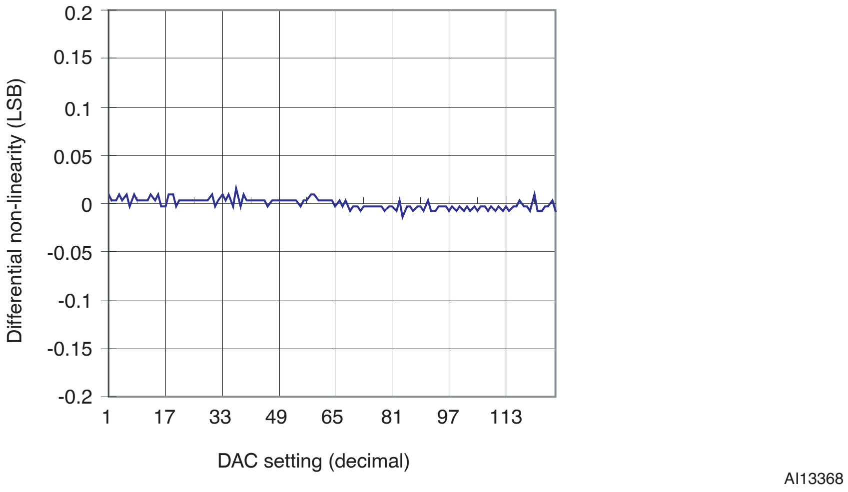


Figure 17. Integral non-linearity vs. DAC setting

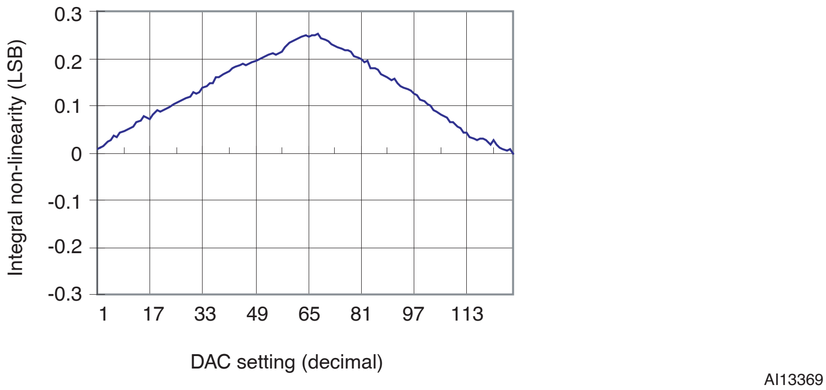
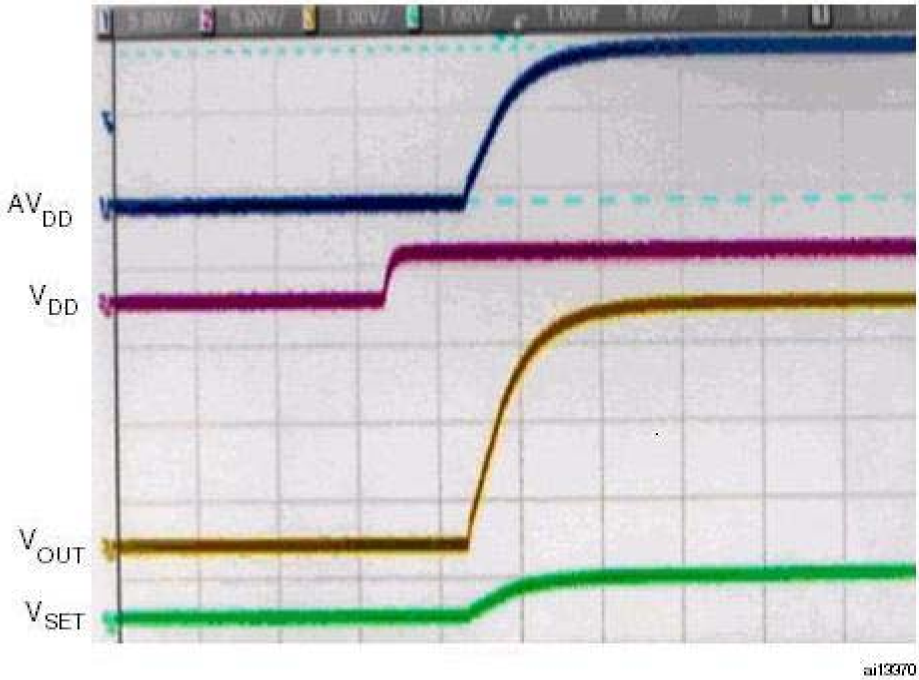
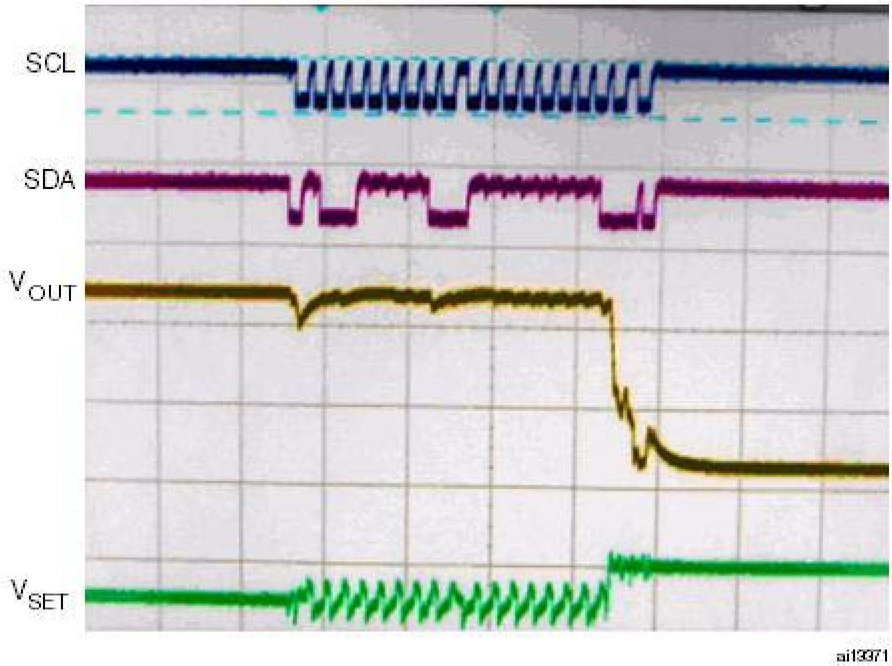


Figure 18. AV_{DD} power-up response



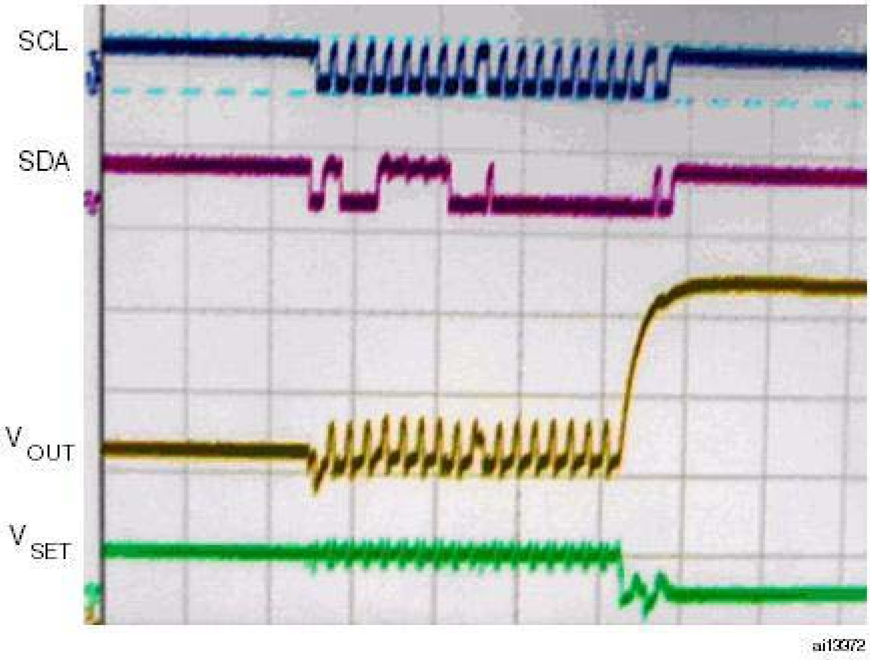
5ms/DIV
AV_{DD}: 5V/DIV, V_{DD}: 5V/DIV, V_{OUT}: 1V/DIV, V_{SET}: 1V/DIV

Figure 19. Full scale-up response



20µs/DIV
SCL: 5V/DIV, SDA: 5V/DIV, V_{OUT}: 1V/DIV, V_{SET}: 1V/DIV

Figure 20. Full scale-down response

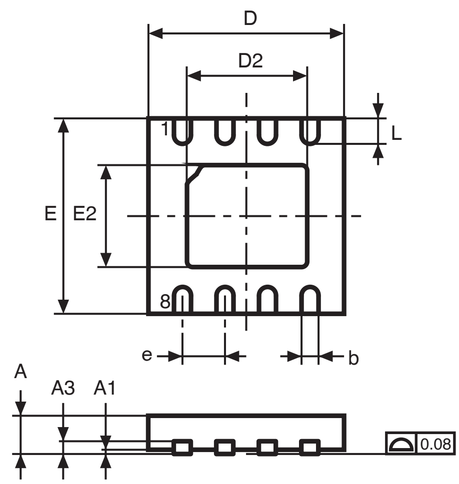


20µs/DIV
SCL: 5V/DIV, SDA: 5V/DIV, V_{OUT}: 1V/DIV, V_{SET}: 1V/DIV

7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 21. TDFN8 3 x 3 x 0.75 mm, pitch 0.65, package mechanical data

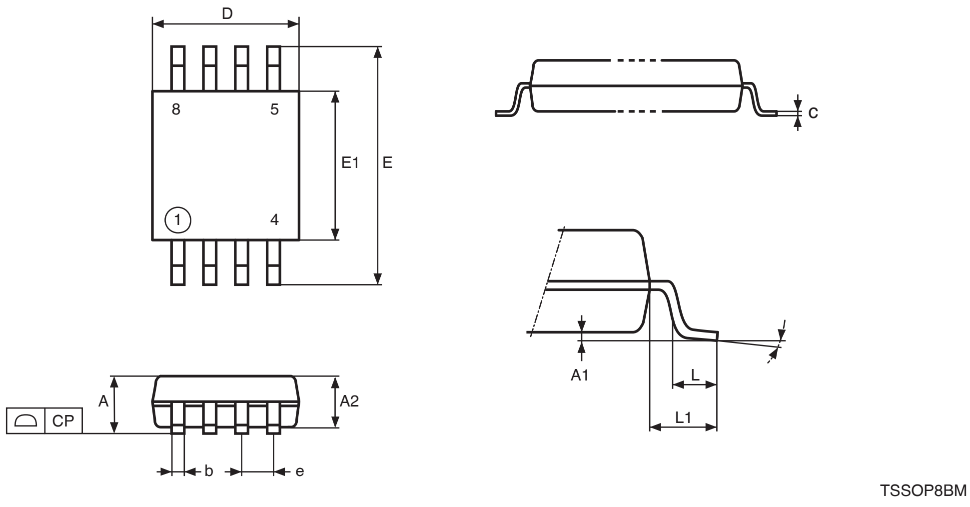


Note: Drawing is not to scale.

Table 9. TDFN8 3 x 3 x 0.75 mm, pitch 0.65, package mechanical data

Sym	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A	0.75	0.70	0.80	0.0295	0.0276	0.0315
A1	0.02	0.00	0.05	0.0008	0.0000	0.0020
A3	0.20			0.0079		
b	0.30	0.25	0.35	0.0118	0.0098	0.0138
D	3.00			0.1181		
D2	2.38	2.23	2.48	0.0937	0.0878	0.0976
E	3.00			0.1181		
E2	1.64	1.49	1.74	0.0646	0.0587	0.0685
e	0.65	–	–	0.0256	–	–
L	0.40	0.30	0.50	0.0157	0.0118	0.0197

Figure 22. TSSOP8 – 8-lead, thin shrink small outline, 3 mm x 3 mm, mech. data



Note: Drawing is not to scale.

Table 10. TSSOP8 – 8-lead, thin shrink small outline, 3 mm x 3 mm, mech. data

Sym	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.100			0.0433
A1		0.050	0.150		0.0020	0.0059
A2	0.850	0.750	0.950	0.0335	0.0295	0.0374
b		0.250	0.400		0.0098	0.0157
c		0.130	0.230		0.0051	0.0091
CP			0.100			0.0039
D	3.000	2.900	3.100	0.1181	0.1142	0.1220
e	0.650	–	–	0.0256	–	–
E	4.900	4.6500	5.150	0.1929	0.1831	0.2028
E1	3.000	2.900	3.100	0.1181	0.1142	0.1220
L	0.550	0.400	0.700	0.0217	0.0157	0.0276
L1	0.950			0.0374		
α		0°	6°		0°	6°
N	8			8		

8 Part numbering

Table 11. Ordering information scheme

Example: STVM100 DC 6 F

Device type

STVM100, V_{COM} calibrator with 7-bit DAC and I^2C interface

Package

DC = TDFN8

DS = TSSOP8

Temperature range

6 = –40 to 85°C

Shipping method

E = ECOPACK® package, tubes

F = ECOPACK® package, tape & reel

For other options, or for more information on any aspect of this device, please contact the ST sales office nearest you.

9 Revision history

Table 12. Document revision history

Date	Revision	Changes
09-May-2006	1	Initial release.
14-Jul-2006	2	Graphical and textual updates
08-Nov-2006	3	Document status upgraded to Preliminary Data; changed the wording of Input function to include ‘WRITE operations’ instead of ‘programming’ in *Table 2: Pin names and functions*; deleted some bracketed text and modified the P bit function in *Section 2.2: Read mode*; ensured that all of *Equation 2* and *Equation 3* were visible; amalgamated 2 cells containing the same information (V_{DD}) in *Table 7: DC and AC characteristics*; deleted footnotes 2 and 3 of *Table 8: AC characteristics*; updated package mechanical information in *Figure 21*, *Table 9*, and *Table 10*.
12-Feb-2007	4	Reformatted inside cover page according to new template; renamed section 1 *Device overview* and section 2 *Device operation*; deleted Signal names table; moved and renamed *Table 2: Pin names and functions*, added*Section 6: Typical operating characteristics* and *Figure 10* to *Figure 20*.
20-Apr-2007	5	Value added in *Section 2.3: Write mode*.
24-Jul-2007	6	Document status upgraded to full datasheet.
04-Nov-2009	7	Added “Note” to *Figure 8*; updated footnote of *Table 4*; minor textual changes.
09-Dec-2009	8	Updated title of datasheet, *Applications*, *Description*, and *Section 3: Application information*.
07-Jun-2013	9	Replaced order code STVM100DC6E with STVM100DC6F in *Table 1: Device summary*

Please Read Carefully: