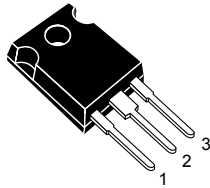
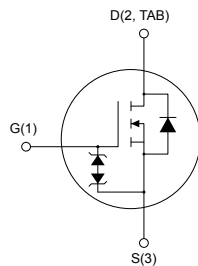


N-channel 650 V, 0.156 Ω typ., 20 A, MDmesh™ DM2 Power MOSFET in a TO-247 package



TO-247



AM01475V1

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STW26N65DM2	650 V	0.190 Ω	20 A	170 W

- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

Applications

- Switching applications

Description

This high-voltage N-channel Power MOSFET is part of the MDmesh™ DM2 fast-recovery diode series. It offers very low recovery charge (Q_{rr}) and time (t_{rr}) combined with low $R_{DS(on)}$, rendering it suitable for the most demanding high-efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

Product status link

[STW26N65DM2](#)

Product summary

Order code	STW26N65DM2
Marking	26N65DM2
Package	TO-247
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_{case} = 25\text{ }^{\circ}\text{C}$	20	A
	Drain current (continuous) at $T_{case} = 100\text{ }^{\circ}\text{C}$	12.6	
$I_{DM}^{(1)}$	Drain current (pulsed)	53	A
P_{TOT}	Total dissipation at $T_{case} = 25\text{ }^{\circ}\text{C}$	170	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	50	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	
T_{stg}	Storage temperature range	-55 to 150	$^{\circ}\text{C}$
T_j	Operating junction temperature range		

1. Pulse width is limited by safe operating area.
2. $I_{SD} \leq 20\text{ A}$, $di/dt=900\text{ A}/\mu\text{s}$, $V_{DS\text{ peak}} < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$
3. $V_{DS} \leq 520\text{ V}$

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.74	$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	50	

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
$I_{AR}^{(1)}$	Avalanche current, repetitive or not repetitive	3	A
$E_{AS}^{(2)}$	Single pulse avalanche energy	530	mJ

1. Pulse width is limited by T_{Jmax}
2. Starting $T_j = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$

2 Electrical characteristics

($T_{\text{case}} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{\text{GS}} = 0\text{ V}$, $I_{\text{D}} = 1\text{ mA}$	650			V
I_{DSS}	Zero gate voltage drain current	$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 650\text{ V}$			1	μA
		$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 650\text{ V}$, $T_{\text{case}} = 125\text{ }^{\circ}\text{C}^{(1)}$			100	
I_{GSS}	Gate-body leakage current	$V_{\text{DS}} = 0\text{ V}$, $V_{\text{GS}} = \pm 25\text{ V}$			± 5	μA
$V_{\text{GS(th)}}$	Gate threshold voltage	$V_{\text{DS}} = V_{\text{GS}}$, $I_{\text{D}} = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{\text{DS(on)}}$	Static drain-source on-resistance	$V_{\text{GS}} = 10\text{ V}$, $I_{\text{D}} = 10\text{ A}$		0.156	0.190	Ω

1. Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance		-	1480	-	pF
C_{oss}	Output capacitance	$V_{\text{DS}} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{\text{GS}} = 0\text{ V}$	-	62	-	
C_{riss}	Reverse transfer capacitance		-	2	-	
$C_{\text{oss eq.}}^{(1)}$	Equivalent output capacitance	$V_{\text{DS}} = 0\text{ to }520\text{ V}$, $V_{\text{GS}} = 0\text{ V}$	-	140	-	pF
R_{G}	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_{\text{D}} = 0\text{ A}$	-	4.6	-	Ω
Q_{g}	Total gate charge	$V_{\text{DD}} = 520\text{ V}$, $I_{\text{D}} = 20\text{ A}$, $V_{\text{GS}} = 0\text{ to }10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	35.5	-	nC
Q_{gs}	Gate-source charge		-	8.2	-	
Q_{gd}	Gate-drain charge		-	17.6	-	

1. $C_{\text{oss eq.}}$ is defined as the constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{\text{d(on)}}$	Turn-on delay time	$V_{\text{DD}} = 325\text{ V}$, $I_{\text{D}} = 10\text{ A}$, $R_{\text{G}} = 4.7\text{ }\Omega$, $V_{\text{GS}} = 10\text{ V}$	-	17	-	ns
t_{r}	Rise time		-	7	-	
$t_{\text{d(off)}}$	Turn-off delay time	(see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	51	-	
t_{f}	Fall time		-	10	-	

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		20	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		53	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 20\text{ A}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 20\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 100\text{ V}$	-	100		ns
Q_{rr}	Reverse recovery charge		-	0.365		μC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	7.3		A
t_{rr}	Reverse recovery time	$I_{SD} = 20\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 100\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$	-	200		ns
Q_{rr}	Reverse recovery charge		-	1.39		μC
I_{RRM}	Reverse recovery current		(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	13.9	

1. Pulse width is limited by safe operating area.
2. Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

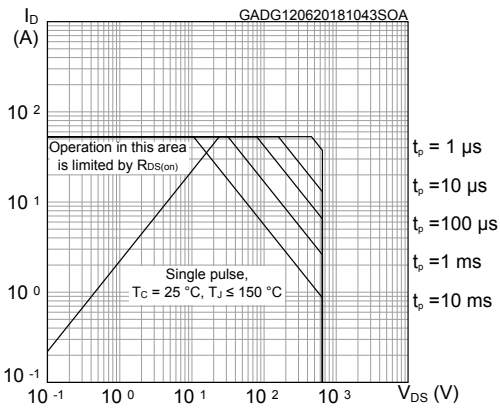


Figure 2. Thermal impedance

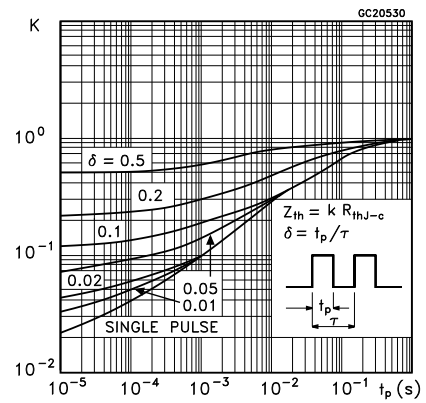


Figure 3. Output characteristics

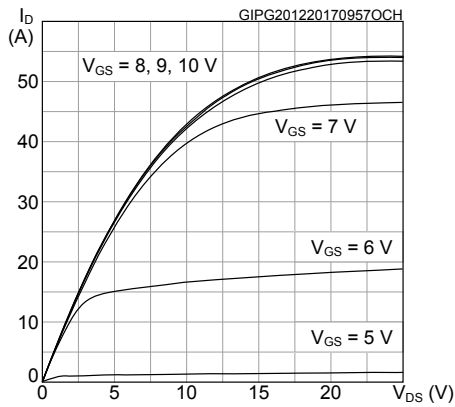


Figure 4. Transfer characteristics

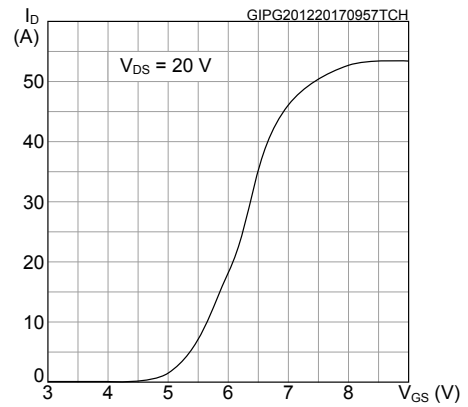


Figure 5. Gate charge vs gate-source voltage

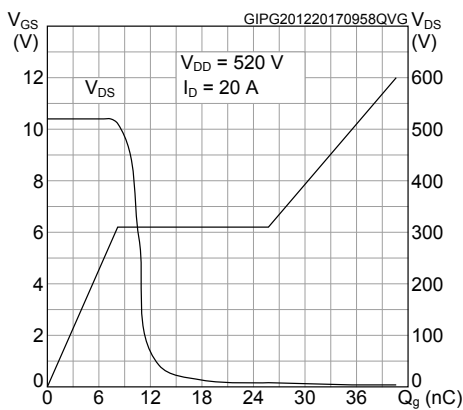


Figure 6. Static drain-source on-resistance

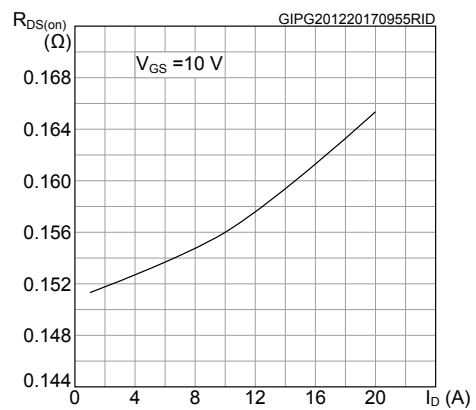


Figure 7. Capacitance variations

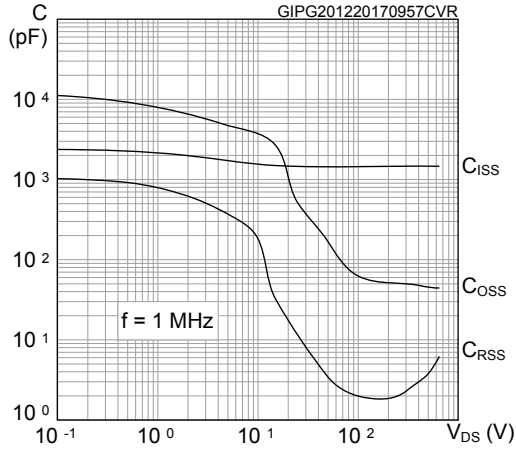


Figure 8. Normalized gate threshold voltage vs temperature

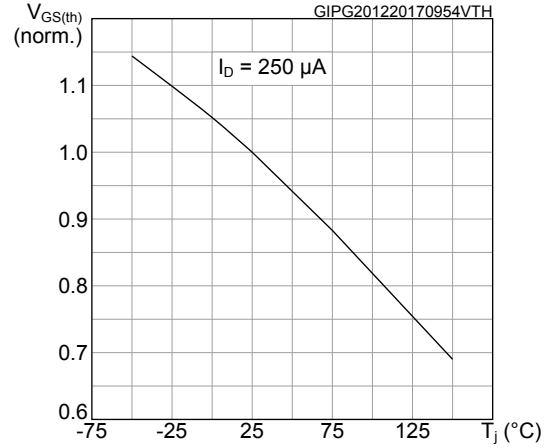


Figure 9. Normalized on-resistance vs temperature

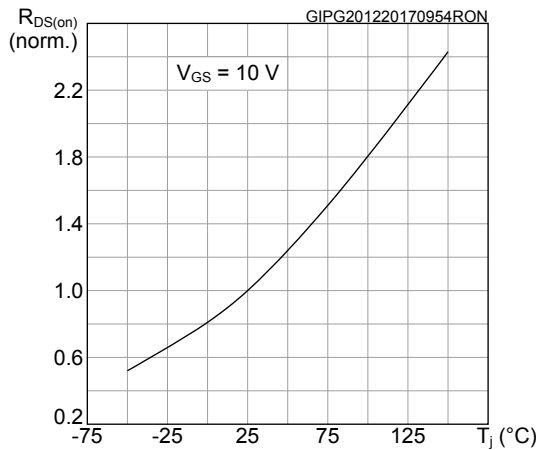


Figure 10. Normalized $V_{(BR)DSS}$ vs temperature

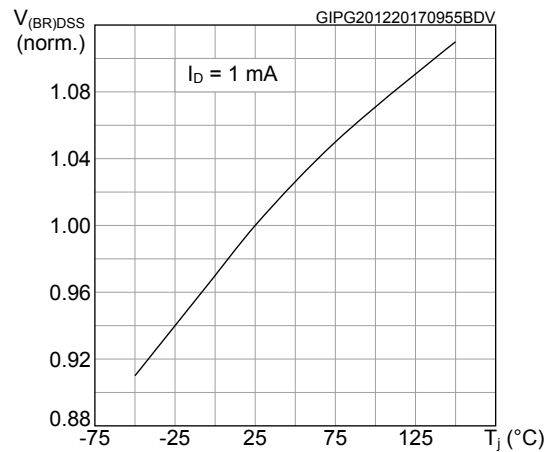


Figure 11. Output capacitance stored energy

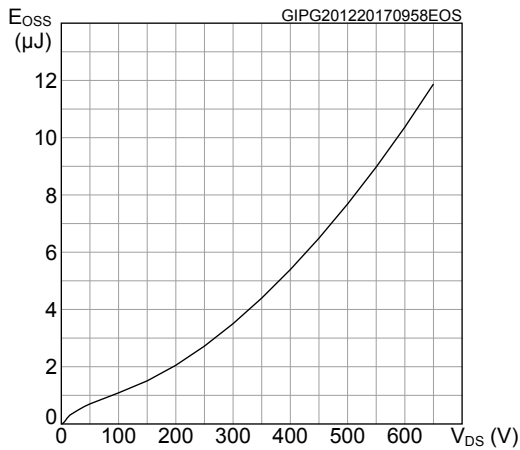
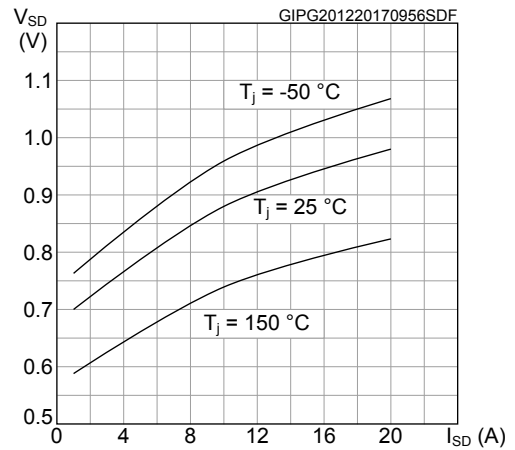
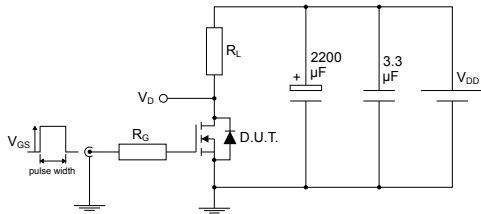


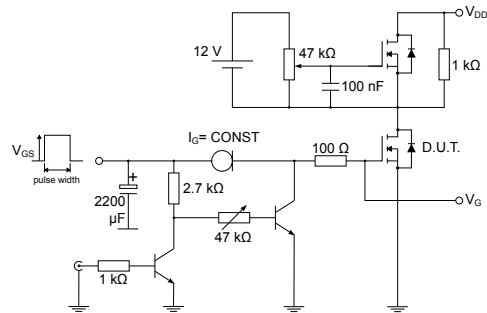
Figure 12. Source-drain diode forward characteristics



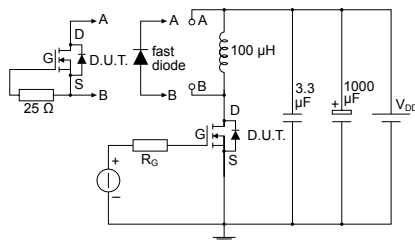
3 Test circuits

Figure 13. Test circuit for resistive load switching times


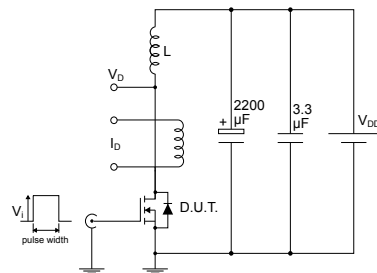
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Figure 14. Test circuit for gate charge behavior


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Figure 15. Test circuit for inductive load switching and diode recovery times


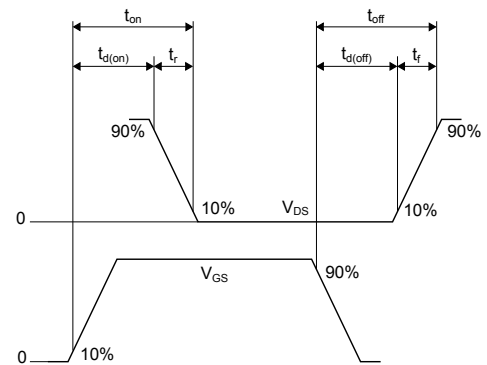
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Figure 16. Unclamped inductive load test circuit


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Figure 17. Unclamped inductive waveform


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Figure 18. Switching time waveform


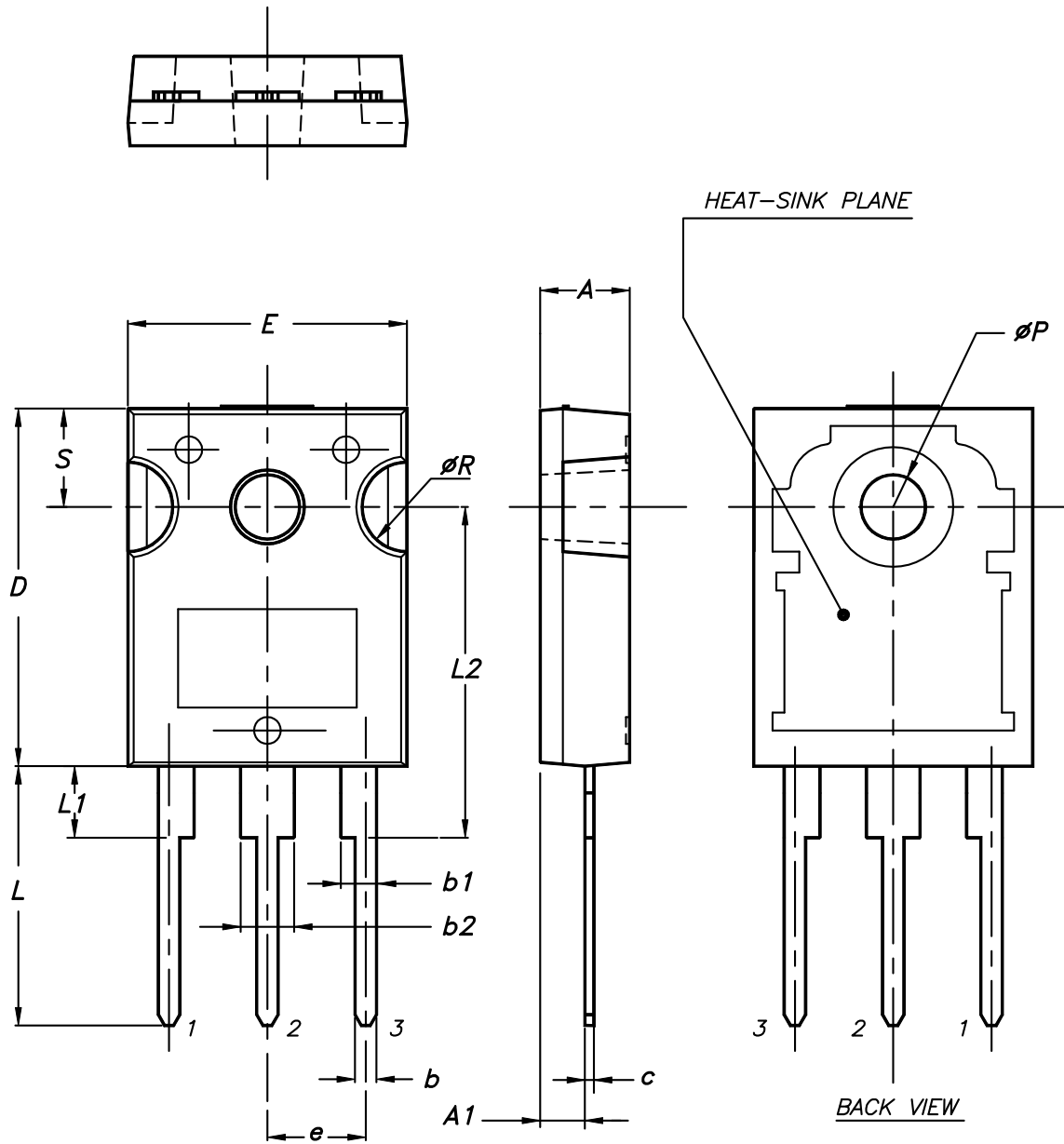
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-247 package information

Figure 19. TO-247 package outline



0075325_9

Table 8. TO-247 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

Revision history

Table 9. Document revision history

Date	Version	Changes
03-Jul-2018	1	Initial release. The document status is production data.

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