

N-channel 650 V, 0.056  $\Omega$  typ., 42 A MDmesh™ V Power MOSFETs  
in TO-247 and TO-247 long leads packages

Datasheet - production data

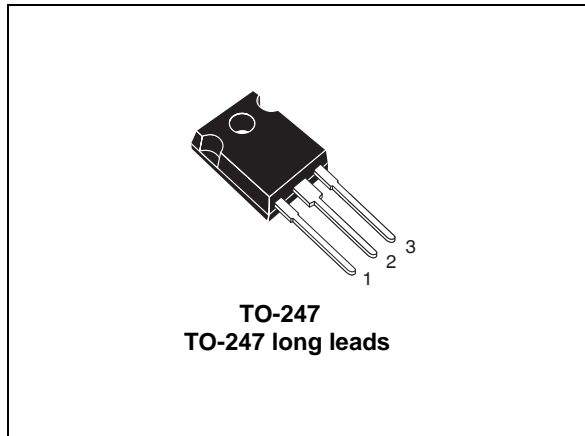
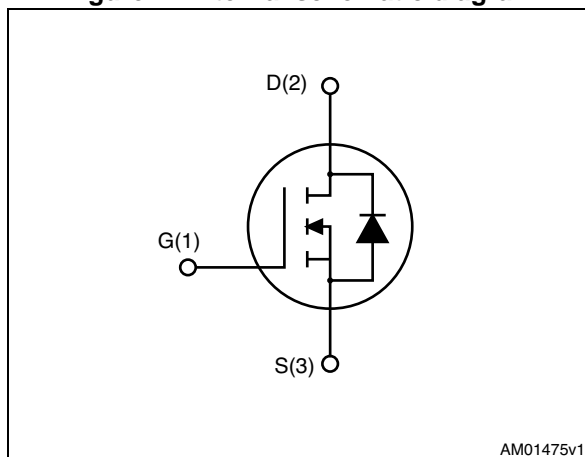


Figure 1. Internal schematic diagram



## Features

Order codes	$V_{DS} @ T_{Jmax}$	$R_{DS(on) max}$	$I_D$
STW57N65M5	710 V	0.063 $\Omega$	42 A
STWA57N65M5			

- Worldwide best  $R_{DS(on)}$ \* area amongst the silicon based devices
- Higher  $V_{DSS}$  rating, high dv/dt capability
- Excellent switching performance
- Easy to drive, 100% avalanche tested

## Applications

- Switching applications

## Description

These devices are N-channel MDmesh™ V Power MOSFETs based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

Table 1. Device summary

Order codes	Marking	Packages	Packaging
STW57N65M5	57N65M5	TO-247	Tube
STWA57N65M5		TO-247 long leads	

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate- source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	42	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	26.5	A
$I_{DM}^{(1)}$	Drain current (pulsed)	168	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	250	W
$I_{AR}$	Max current during repetitive or single pulse avalanche (pulse width limited by $T_{JMAX}$ )	11	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{V}$ )	960	mJ
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(3)}$	MOSFET $dv/dt$ ruggedness	50	V/ns
$T_{stg}$	Storage temperature	-55 to 150	$^\circ\text{C}$
$T_j$	Max. operating junction temperature	150	$^\circ\text{C}$

1. Pulse width limited by safe operating area.

2.  $I_{SD} \leq 42\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DS(peak)} < V_{(BR)DSS}$ ,  $V_{DD} = 400\text{ V}$

3.  $V_{DS} \leq 520\text{ V}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.50	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	50	$^\circ\text{C}/\text{W}$

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 4. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0$	650			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 650\text{ V}$ $V_{DS} = 650\text{ V}$ , $T_C = 125\text{ °C}$			1 100	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 25\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 21\text{ A}$		0.056	0.063	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$	-	4200	-	pF
$C_{oss}$	Output capacitance		-	115		pF
$C_{riss}$	Reverse transfer capacitance		-	9		pF
$C_{o(er)}^{(1)}$	Equivalent output capacitance energy related	$V_{GS} = 0$ , $V_{DS} = 0\text{ to }520\text{ V}$	-	93	-	pF
$C_{o(tr)}^{(2)}$	Equivalent output capacitance time related		-	303	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ , $I_D = 0$	-	1.3	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 520\text{ V}$ , $I_D = 21\text{ A}$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 17</a> and <a href="#">20</a> )	-	98	-	nC
$Q_{gs}$	Gate-source charge		-	23		nC
$Q_{gd}$	Gate-drain charge		-	40		nC

- $C_{o(er)}^{(1)}$  is a constant capacitance value that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$
- $C_{o(tr)}^{(2)}$  is a constant capacitance value that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(V)}$	Voltage delay time	$V_{DD} = 400\text{ V}$ , $I_D = 28\text{ A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 17</a> and <a href="#">20</a> )	-	73	-	ns
$t_{r(V)}$	Voltage rise time		-	15	-	ns
$t_{f(i)}$	Current fall time		-	12	-	ns
$t_{c(off)}$	Crossing time		-	19	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		42	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				168	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 42\text{ A}$ , $V_{GS} = 0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 42\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$ (see <a href="#">Figure 17</a> )	-	418		ns
$Q_{rr}$	Reverse recovery charge		-	8		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	40		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 42\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 17</a> )	-	528		ns
$Q_{rr}$	Reverse recovery charge		-	12		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	44		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

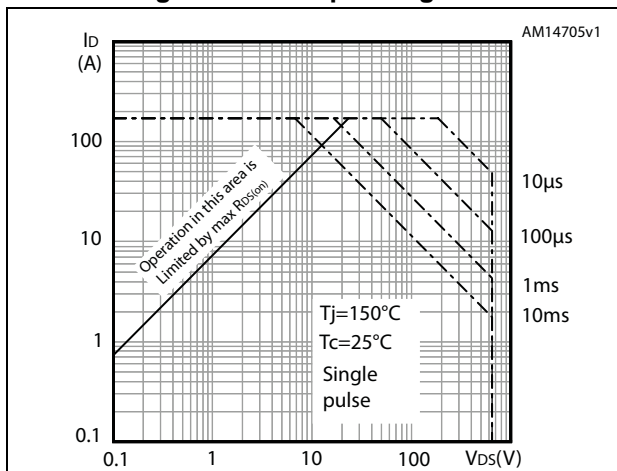


Figure 3. Thermal impedance

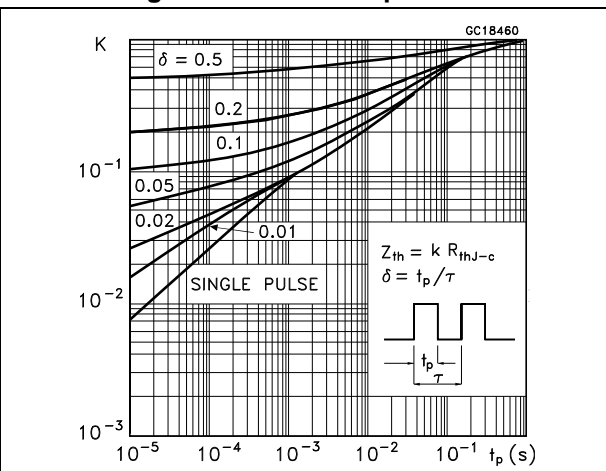


Figure 4. Output characteristics

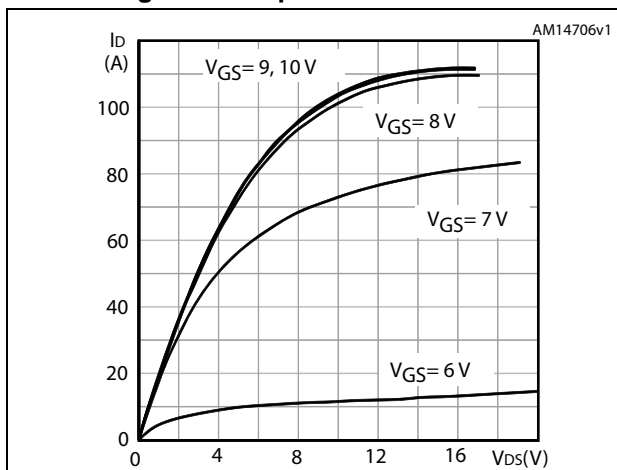


Figure 5. Transfer characteristics

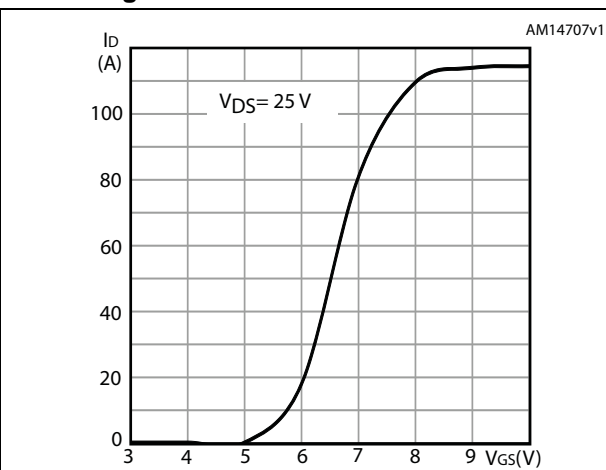


Figure 6. Gate charge vs gate-source voltage

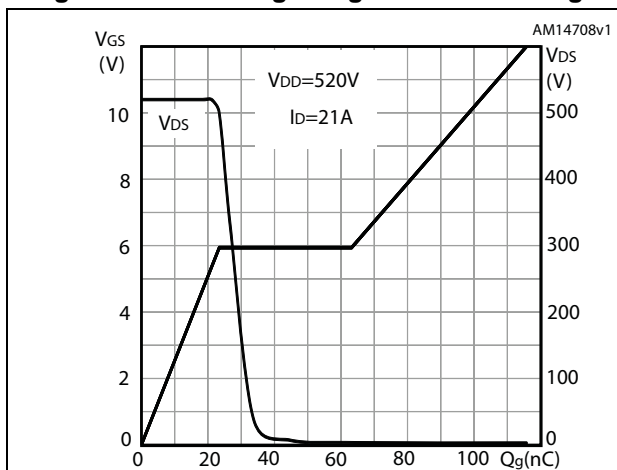


Figure 7. Static drain-source on-resistance

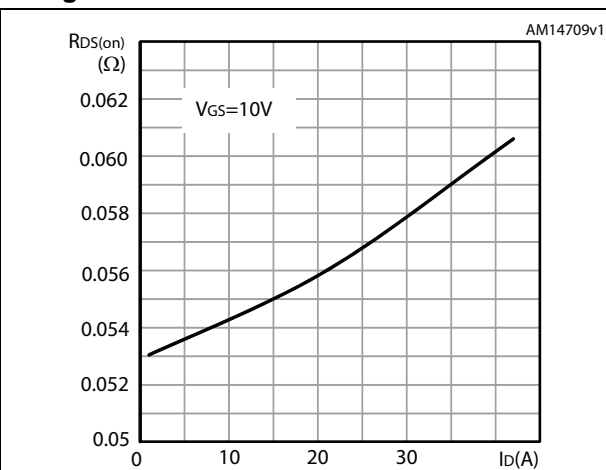


Figure 8. Capacitance variations

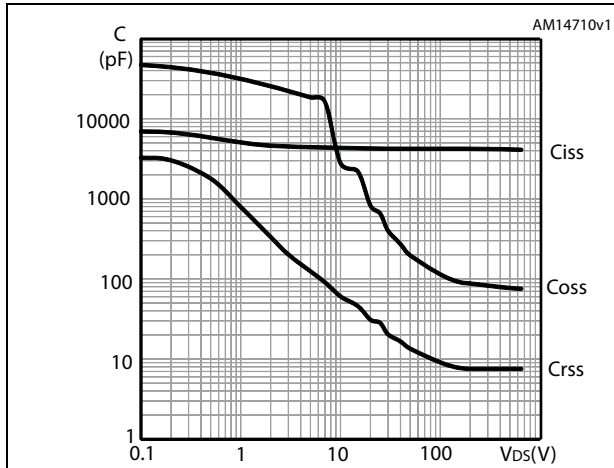


Figure 9. Output capacitance stored energy

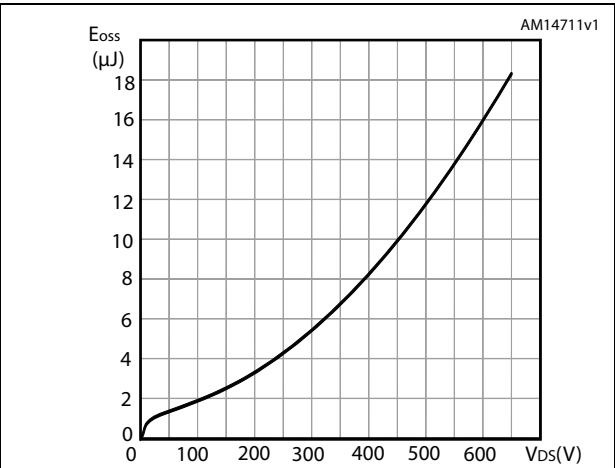


Figure 10. Normalized gate threshold voltage vs temperature

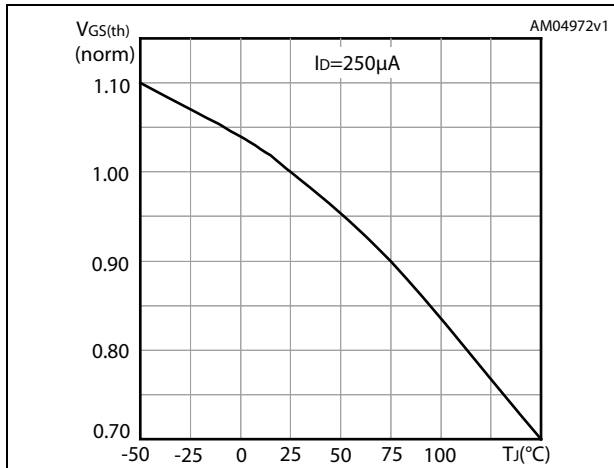


Figure 11. Normalized on-resistance vs temperature

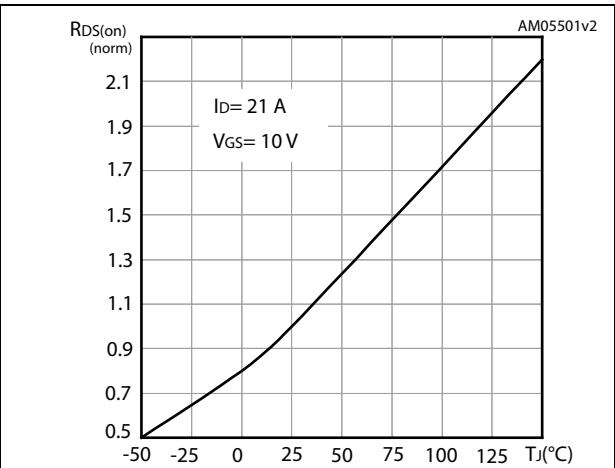


Figure 12. Source-drain diode forward characteristics

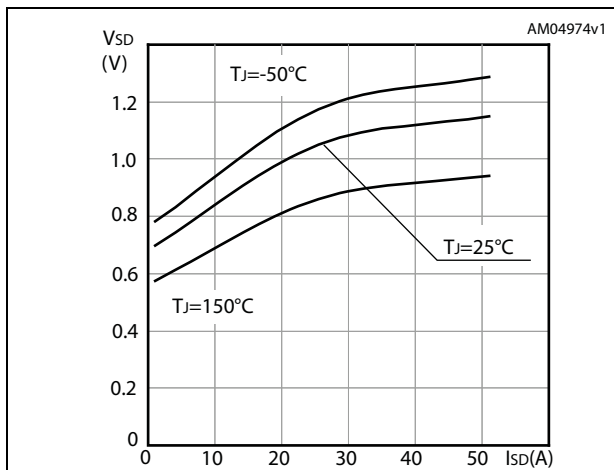


Figure 13. Normalized V<sub>DS</sub> vs temperature

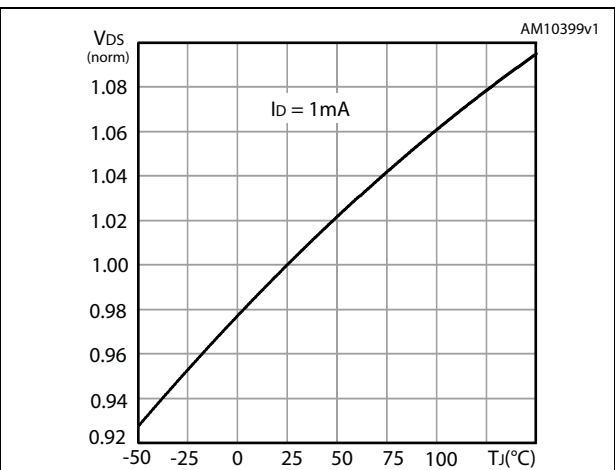
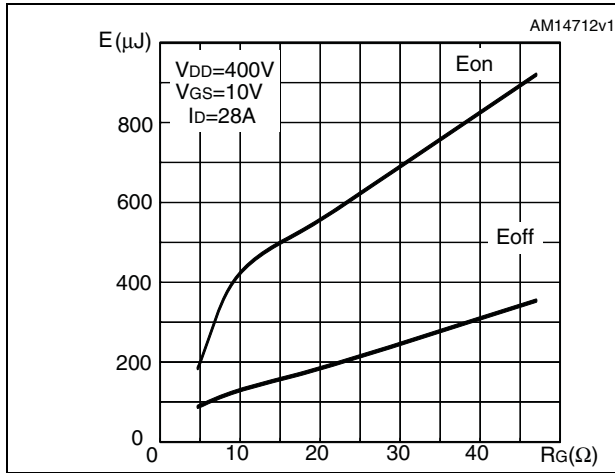


Figure 14. Switching losses vs gate resistance (1)



1.  $E_{on}$  including reverse recovery of a SiC diode



### 3 Test circuits

Figure 15. Switching times test circuit for resistive load

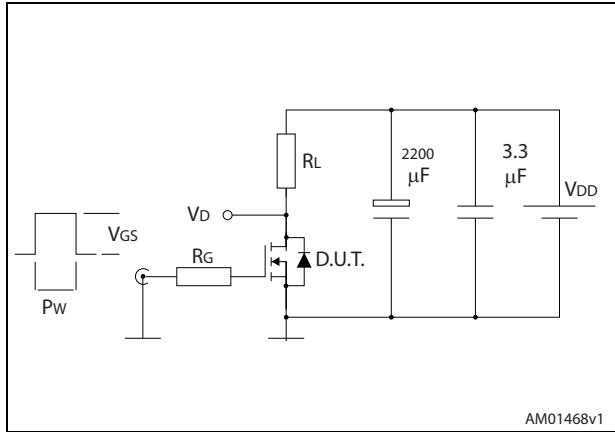


Figure 16. Gate charge test circuit

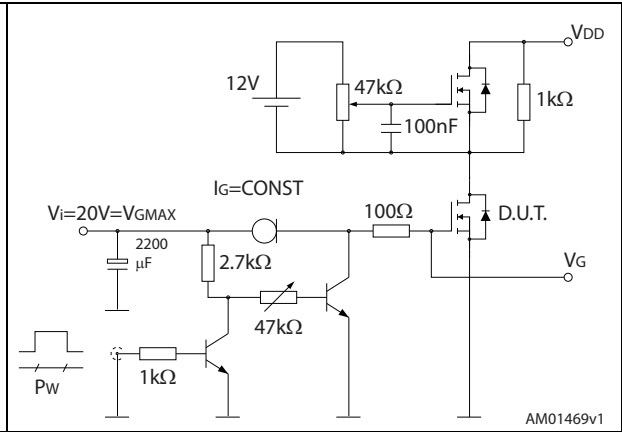


Figure 17. Test circuit for inductive load switching and diode recovery times

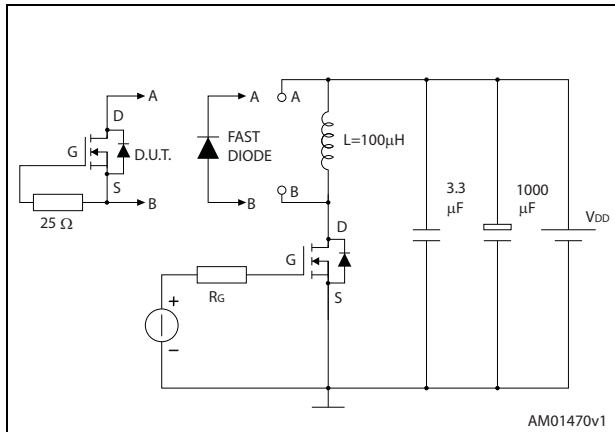


Figure 18. Unclamped inductive load test circuit

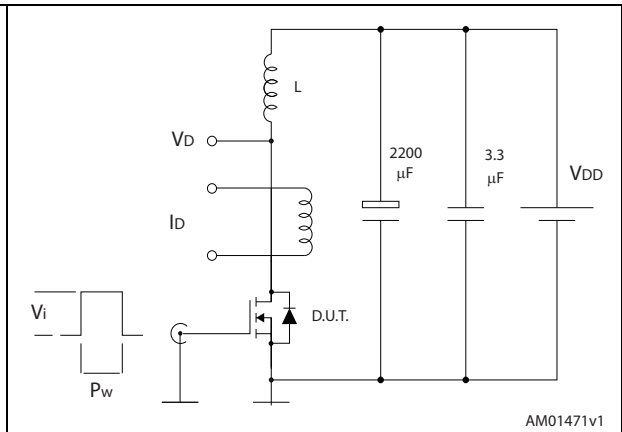


Figure 19. Unclamped inductive waveform

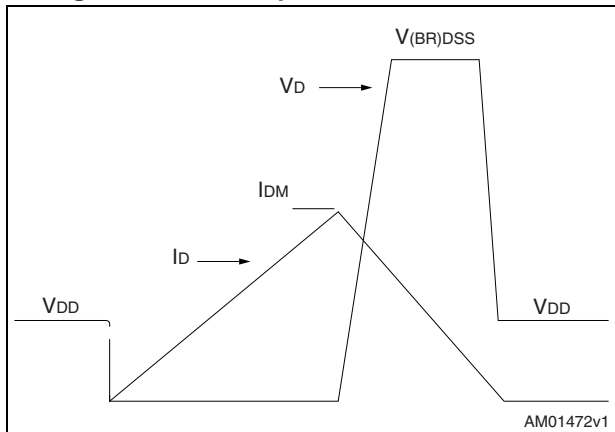
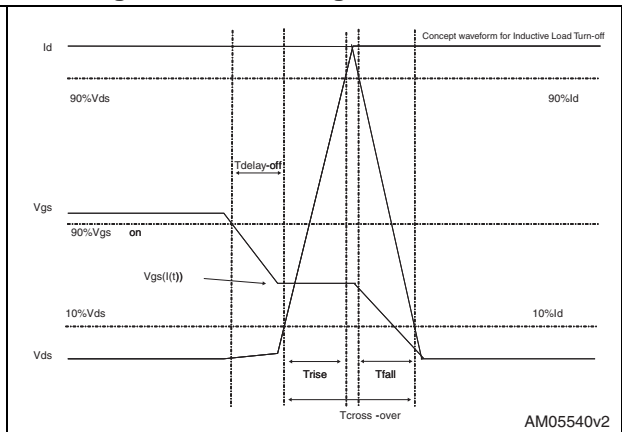


Figure 20. Switching time waveform



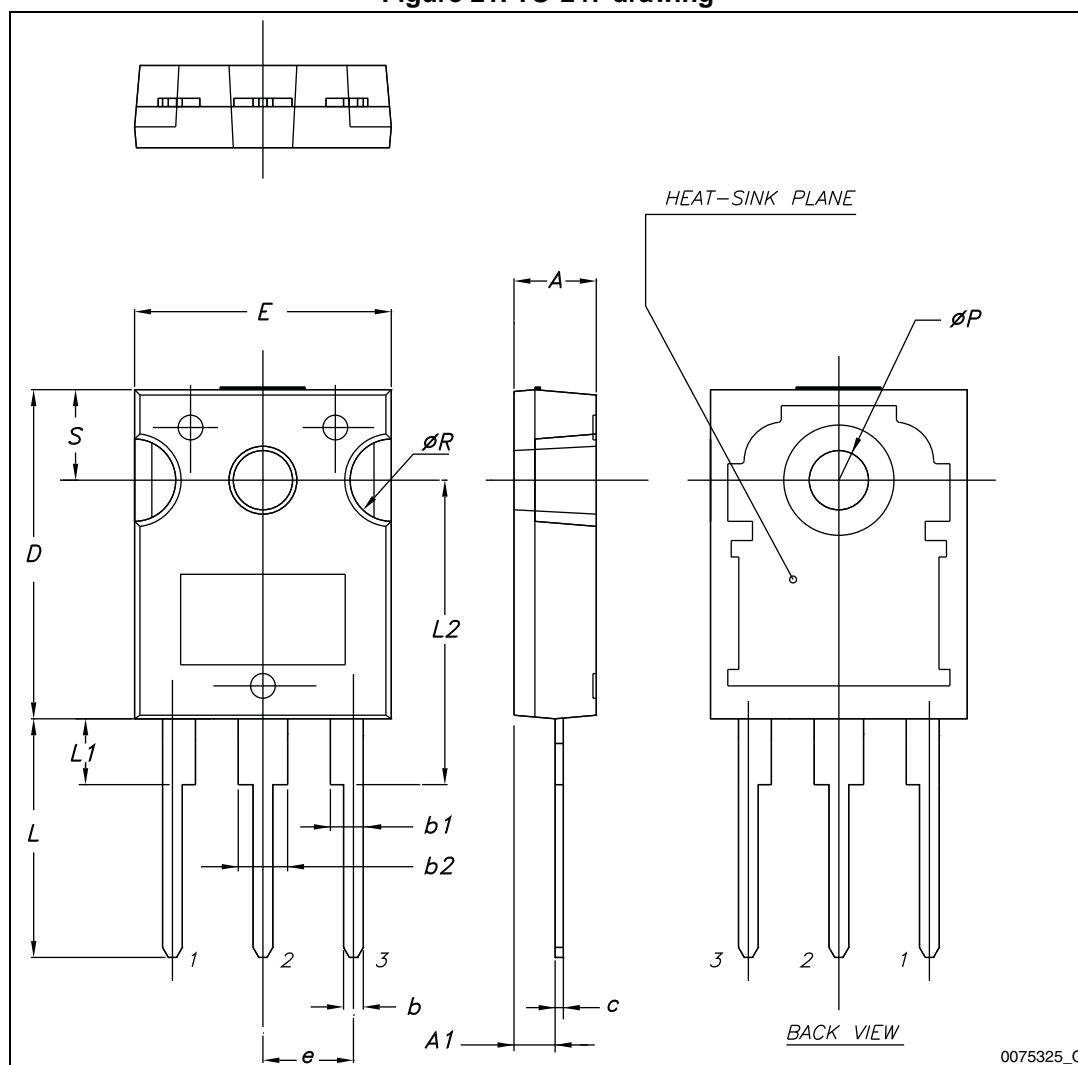
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Table 8. TO-247 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

Figure 21. TO-247 drawing

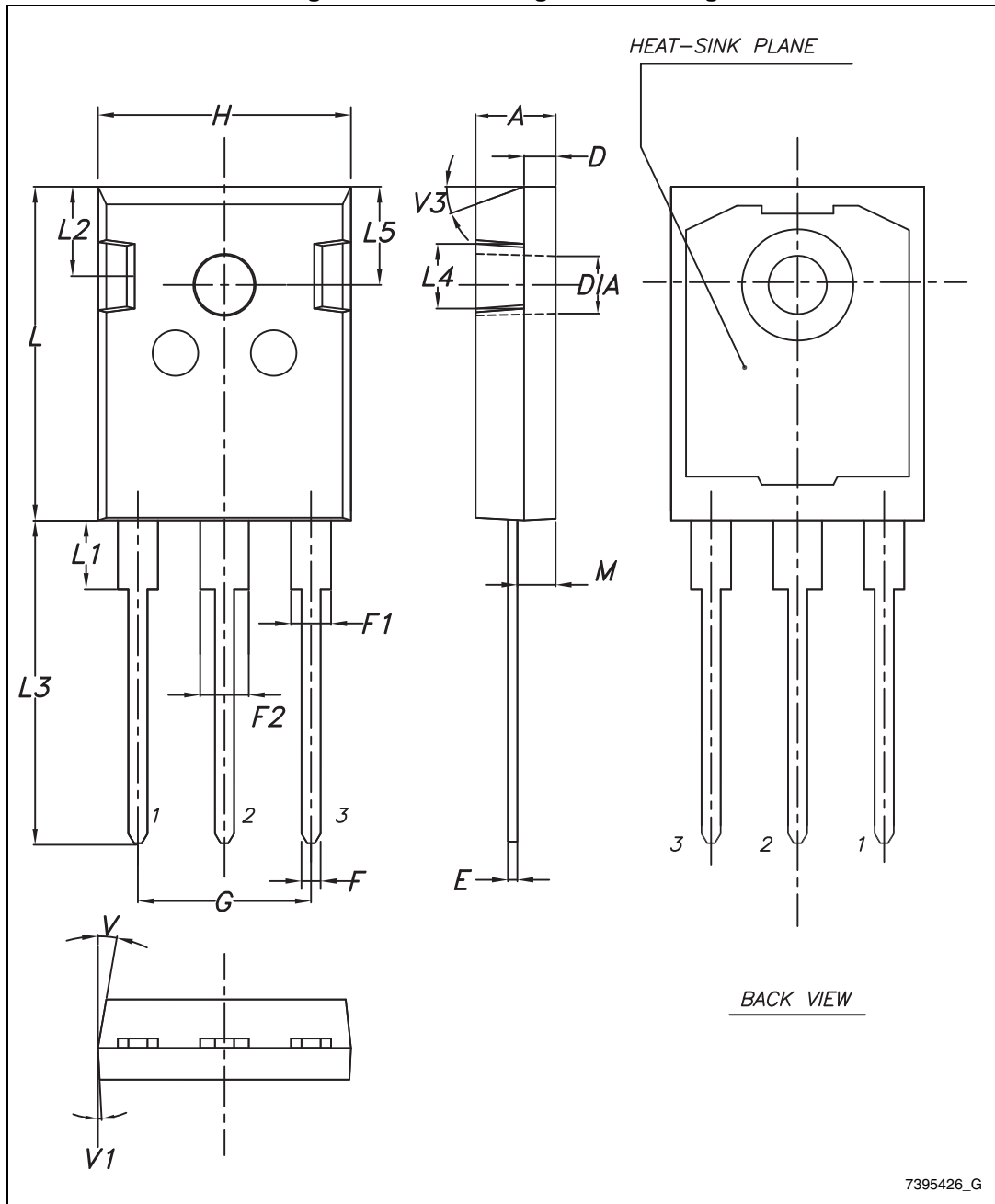


0075325\_G

Table 9. TO-247 long leads mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.90		5.15
D	1.85		2.10
E	0.55		0.67
F	1.07		1.32
F1	1.90		2.38
F2	2.87		3.38
G	10.90 BSC		
H	15.77		16.02
L	20.82		21.07
L1	4.16		4.47
L2	5.49		5.74
L3	20.05		20.30
L4	3.68		3.93
L5	6.04		6.29
M	2.25		2.55
V		10°	
V1		3°	
V3		20°	
Dia.	3.55		3.66

Figure 22. TO-247 long leads drawing



## 5 Revision history

Table 10. Document revision history

Date	Revision	Changes
17-Dec-2012	1	First release.
13-Dec-2013	2	<ul style="list-style-type: none"><li>– Modified: <a href="#">Figure 1</a></li><li>– Added: MOSFET dv/dt ruggedness parameter in <a href="#">Table 2</a> and <a href="#">note 3</a></li><li>– Modified: test conditions <math>C_{o(er)}</math> and <math>C_{o(tr)}</math> in <a href="#">Table 5</a></li><li>– Updated: the entire <a href="#">Section 2.1: Electrical characteristics (curves)</a> except <a href="#">Figure 14: Switching losses vs gate resistance</a></li><li>– Updated: <a href="#">Section 4: Package mechanical data</a></li><li>– Minor text changes</li></ul>

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