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STWLC38

Datasheet

Qi-compliant dual mode wireless power receiver for up to 15W applications

Product status link
STWLC38

Product summary	
Order code	STWLC38JRM
Package	WLCSP40
Packing	Tape and Reel

Features

- Up to 15 W output power
- Up to 5W output power in Tx mode
- Qi 1.3 inductive wireless standard communication protocol compliant
- High efficiency (98% typical) synchronous rectifier operating up to 800 kHz
- Low drop-out linear regulator with output current limit and input voltage control loop
- Adaptive Rectifier Configuration (ARC) Mode for enhanced spatial freedom
- 4 V to 12 V programmable output voltage
- Above 85% overall system efficiency
- 32-bit, 64 MHz ARM Cortex M0+ core with 32kB RRAM,16 kB SRAM,64kB ROM
- 10-bit A/D Converter
- Configurable GPIOs
- I2C Slave interface
- Multi-level ASK modulator, Enhanced FSK demodulator
- Output Over-Voltage clamping protection
- Accurate voltage/current measurement for Foreign Object Detection (FOD)
- On-chip thermal management and protections
- Flip chip 40 bumps (2.12mm x 3.32mm)

Applications

- Smartphones
- Wearable/Hearables TWS
- Asset tracking devices
- Medical and healthcare equipment

Description

The STWLC38 is an integrated Wireless Power Receiver suitable for wearable/ hearable and smart phone applications and can supply up to 15 W of output power. The chip has been designed to support Qi 1.3 specifications for inductive communication protocol, 5W Baseline Power Profile and 15W Extended Power Profile.

STWLC38 shows excellent efficiency performance thanks to the integrated low-loss synchronous rectifier and the low drop-out linear regulator: both elements are dynamically managed by the digital core to minimize the overall power dissipation over a wide range of output load conditions.

Through the I^2C interface the user can access and modify different configuration parameters, tailoring the operation of the device to the needs of custom applications. The configuration parameters can be saved in the embedded Resistive RAM (RRAM) and automatically retrieved at power-up.

STWLC38 is also capable of operating in Tx mode to transmit power to charge other devices. The device can provide power up to 5W Output power in this mode.

The STWLC38 is housed in a Chip-Scale Package to fit real-estate sensitive solutions in wearable devices.

1 Introduction

STWLC38 is a Wireless Power Receiver that rectifies the AC voltage developed across the receiving coil and provides a regulated DC voltage at the output.

The 32-bit core MCU is the supervisor of the whole device and manages all the functional blocks to

- establish and maintain communication with the transmitter,
- ensure adherence to Qi standard specifications (wherever required),
- optimize the efficiency by properly adjusting the operating point
- guarantee reliability by monitoring and protecting both the load and the device itself.

In order to execute the above mentioned (and many others) tasks, the MCU core relies on a resident firmware stored in ROM . In addition, some configuration parameters (e.g. output voltage, FOD tuning parameters, etc.) can be saved in the internal few times programmable Resistive RAM (RRAM) and retrieved at power-up, allowing the STWLC38 to operate as a fully autonomous stand-alone chip.

For applications in which the host system directly monitors or controls the power transfer, the I2C interface provides access to the internal registers of the STWLC38.

The device is also equipped with three programmable general-purpose I/O pins (GPIOs) to implement specific functions (e.g. driving status LEDs, enabling the output on request, informing the host system about faulty conditions, etc.).

Figure below shows the block diagram of the device with simplified interconnections among the functional blocks. The synchronous rectifier converts the AC voltage from the receiving coil into a DC voltage at the VRECT pin. The four switches of the rectifier (that is basically an H-bridge) are controlled by the digital core in order to minimize both conduction and switching losses as a function of the output voltage and current, both monitored by two channels of the ADC. Two bootstrap capacitors are externally connected to the BOOT1-BOOT2 pins to correctly drive the high-side switches of the rectifier.

The output of the rectifier, filtered by an external capacitor, is also the input rail for the main LDO linear regulator and for the auxiliary linear regulators in charge of deriving the 1.1 V and 2.5 V supply voltages.

The digital core has full control of the main LDO linear regulator in order to manage the output voltage, the output current and the drop-out voltage.

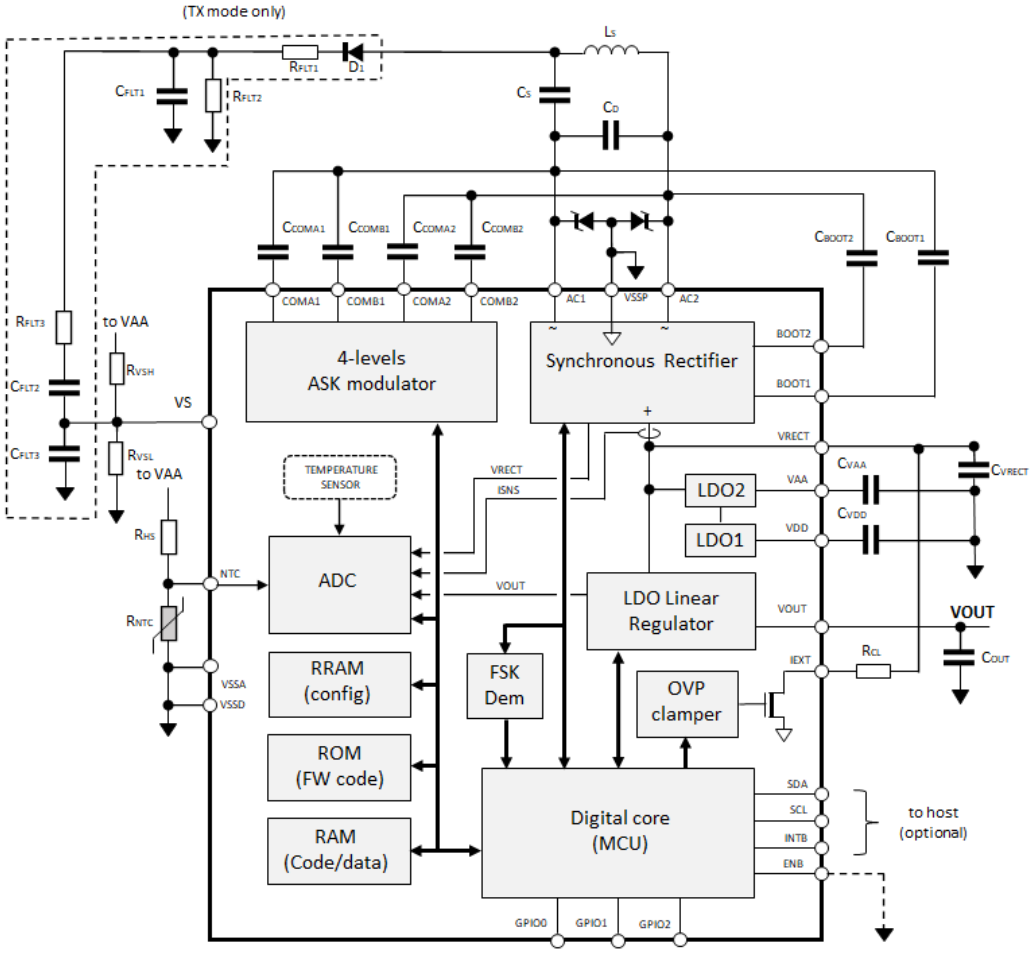
Of course the minimization of the drop-out voltage requires a closed loop regulation of the voltage at the VRECT pin, i.e. a feedback information that is sent to the transmitter (via ASK modulation) which, in turn, adjusts the delivered power by acting on the supply voltage, the switching frequency or the switching duty-cycle (or a combination of the three) of its own power stage, depending on the adopted technique.

This regulation loop involving the transmitter is an essential part of the wireless power transmission and is extensively described in Qi specifications.

STWLC38 is also capable to function as a transmitter to provide power up to 5W.

2 Block diagram

Figure 1. **Simplified block diagram**



3 Device pin out

Figure 2. **Pin assignment (through top view)**

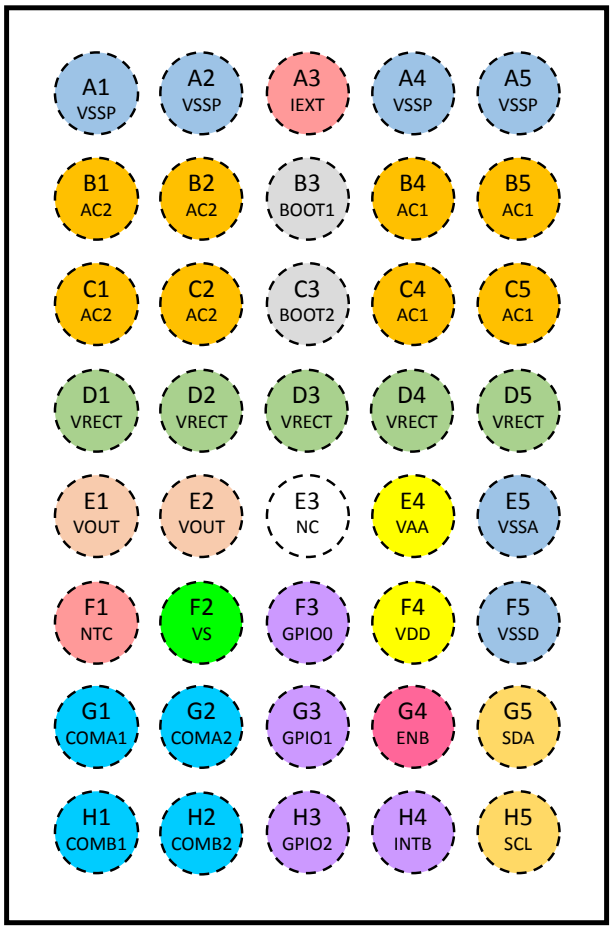


Table 1. **Pin description**

Pin name	Pin location	Pin function
VSSA	E5	Analog ground. Power return for the main LDO and the analog circuitry.
VSSD	F5	Digital ground. Reference for digital input and output signals.
VSSP	A1, A2, A4, A5	Power ground. Power return for the synchronous rectifier.
AC1	B4, B5, C4, C5	AC power input: input of the synchronous rectifier. Connect to RX series resonant circuit.
AC2	B1, B2, C1, C2	AC power input: input of the synchronous rectifier. Connect to RX series resonant circuit.
BOOT1	B3	Synchronous rectifier bootstrap capacitor connection: a 47 nF (typ.) ceramic capacitor is connected between this pin and AC1.
BOOT2	C3	Synchronous rectifier bootstrap capacitor connection: a 47 nF (typ.) ceramic capacitor is connected between this pin and AC2.
COMA1	G1	Modulation switches connection: capacitors between COMA1 and AC1 pin and between COMA2 and AC2 pin are used to implement ASK modulation.
COMA2	G2	

Pin name	Pin location	Pin function
COMB1	H1	Auxiliary modulation switches connection: capacitors between COMB1 and AC1 and between COMB2 and AC2 are used to implement additional ASK modulation. These pins are optionally used, in conjunction with COMA1 and COMA2 pins, to modify the ASK modulation index in specific operating conditions.
COMB2	H2	
VRECT	D1, D2, D3,D4, D5	Synchronous rectifier output and input for the main LDO linear regulator. A suitable capacitor between these pins and VSSA ensures residual AC ripple filtering and energy storage for proper load-transient response.
VS	F2	ASK de-modulation input;
NTC	F1	Coil temperature-sensing input: this pin is connected to the center tap of a resistor divider having an NTC in the low-side position. If this function is not used, the pin must be pulled-up to VAA through a 10 kΩ resistor to prevent triggering the coil over-temperature protection. If not used as temperature-sensing pin, it can be used as ADCIN2 sampling input pin
VOUT	E1,E2	Main LDO linear regulator output voltage. Connect a suitable filtering capacitor between these pins and VSSA to ensure stable operation and proper load transient response in all operating conditions.
NC	E3	Not connected (To be left floating)
VDD	F4	1.1 V LDO output and supply rail for the digital core, the ADC, and the analog circuitry. Connect a 1 µF filtering capacitor between this pin and ground.
VAA	E4	2.5 V LDO output and supply rail for the auxiliary circuitry. Connect a 4.7 µF filtering capacitor between this pin and ground.
ENB	G4	Chip-enable input. If set high, the device is disabled. This pin is eventually used by the host controller to control the power transfer process. Connect to ground if not used.
IEXT	A3	Internal pull-down switch for active (dissipative) over-voltage clamper: a resistor with adequate power dissipation capability must be connected between this pin and VRECT to damp excessive voltage developing at the output of the rectifier.
SCL	H5	I2C bus, clock line input. A pull-up resistor to the supply rail of the host controller is required to ensure correct digital levels.
SDA	G5	I2C bus, data line I/O. A pull-up resistor to the supply rail of the host controller is required to ensure correct digital levels.
GPIO0	F3	Programmable general-purpose I/Os: the function of these pins depends on the configuration of the device.
GPIO1	G3	
GPIO2	H3	
INTB	H4	Interrupt output (active low). Programmable open-drain output used to generate an interrupt on specific events for the host controller.

4 Electrical and thermal specifications

4.1 Absolute maximum ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other condition above those indicated in Table 2 is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Table 2. Absolute maximum ratings

Parameter	Pin(s)	Min.	Max.	Unit
Pin voltage range	AC1, AC2, COMA1, COMA2, COMB1 and COMB2 respect to ground (VSSA, VSSD and VSSP pins)	-0.9	20	V
	BOOT1 to AC1	-0.3	2.75	
	BOOT2 to AC2			
	BOOT1 and BOOT2 respect to ground (VSSA, VSSD and VSSP pins)	-0.3	22.5	
	VRECT, VOUT and IEXT respect to ground (VSSA, VSSD and VSSP pins)	-0.9	20	
	VDD respect to ground (VSSA, VSSD, and VSSP pins)	-0.3	1.21	
	VAA, VS, and NTC respect to ground (VSSA, VSSD, and VSSP pins)	-0.3	2.75	
	GPIO0, GPIO1, GPIO2, INTB, ENB, SDA and SCL respect to ground (VSSA, VSSD, and VSSP pins)	-0.3	3.6	
	Relative voltage between any ground pin (VSSA, VSSD, VSSP)	-0.3	0.3	
RMS pin current	AC1, AC2, VRECT, VOUT		2	A
	COMA1, COMA2, COMB1, COMB2, IEXT		0.5	
HBM ESD susceptibility JEDEC JS001-2012	All pins		2000	V
CDM ESD susceptibility JEDEC JS002-2012			500	
Latch-Up EIA/JESD78E		-200	200	mA

4.2 Thermal characteristics

Table 3. Thermal characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$T_{A,OP}$(1)	Operating ambient temperature		-40		85	°C
$T_{J,OP}$	Operating junction temperature		0		125	
$R_{\Theta JA}$(2)	Junction to ambient thermal resistance	2s2p		48		°C/W
T_{SHDN}	Thermal shutdown threshold			125		°C
$T_{SHDN,HYST}$	Thermal shutdown hysteresis			10		

1. *$T_{A,OP}$ -40°C to +85°C, limits over the operating range guaranteed by design and characterization, if not otherwise specified.*
2. *Device mounted on a standard JESD51-5 test board*

4.3 Electrical characteristics

0 °C < T_A < 85 °C; V_{VRECT} = 5 V to 10 V. Typical values are at T_J = 25 °C, if not otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Supply section						
$V_{VRECT,UVLO}$	VRECT Under-Voltage Lock-Out upper (turn-on) threshold	VRECT pin voltage, rising edge		2.5		V
	VRECT Under-Voltage Lock-Out lower (turn-off) threshold	VRECT pin voltage, falling edge		2.3		
$V_{VRECT,MAX}$	VRECT maximum operating supply voltage	Voltage on VRECT pin			HOVP setting	V
$I_{VOUT,Q}$	VOUT current consumption in shut-down mode	ENB High for more than 1 ms, supply voltage (5 V) applied to VOUT		500		µA
$I_{VRECT,OP}$	Operating current consumption (not considering the programmed dummy-load current)	ENB low, supply voltage applied to VRECT		5		mA
$I_{VOUT,OP}$		ENB low, supply voltage applied to VOUT		5		
1.1V supply voltage LDO linear regulator						
VDD	LDO1 output voltage	I_{VDD} = 5 mA	1.05	1.10	1.15	V
	LDO1 under-voltage lock-out upper threshold		0.85	0.9	0.95	V
2.5V supply voltage LDO linear regulator						
V AA	LDO2 output voltage	I_{VAA} =10 mA	2.4	2.5	2.6	V
	LDO2 under-voltage lock-out upper threshold		2.0	2.1	2.2	V
$I_{VAA,EXT}$	Maximum current allowed for external load				20	mA
Synchronous rectifier						
$R_{DSON,ACx}$	Synchronous rectifier switches on-resistance	low resistance mode (dynamically selected)		50		m Ω
ASK modulator						
$R_{DSON,COMMx}$	COMAx-COMBx modulation switches on-resistance	V_{VRECT} = 5 V		0.5	1	Ω
$I_{COMxx,MAX}$	COMAx-COMBx modulation switches current capability	RMS value		0.25		A
Main LDO linear regulator						
V_{OUT}	Output voltage	VOUT_SET=5V 0x00B2 = 2D I_{VOUT}=0.1A	4.95	5.0	5.05	V
		VOUT_SET=12V 0x00B2=49 I_{VOUT}=0.1A	11.95	12	12.05	
	VOUT Line regulation	I_{VOUT} = 0.1 A, V_{OUT} = 5 V, 5.1 V < V_{VRECT}< 12 V		30	50	mV
	VOUT Load regulation	V_{VRECT} = 5.5 V, V_{OUT} = 5 V, 1 mA < I_{VOUT} < 1A		50	70	mV

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{OUT_STEP}	Programmable step size			25		mV
V_{DROP}	Linear regulator drop-out voltage	I_{OUT} = 1 A		80		mV
I_{OUT_CL}	Linear regulator over current protection			1.75		A
Thermal protection (external NTC)						
$V_{NTC,OTP}$	External over-temperature NTC pin upper threshold		0.55	0.59	0.65	V
	External over-temperature NTC pin hysteresis		50	125	150	mV
$I_{NTC,BIAS}$	NTC pin bias current	V_{NTC} = 1.5 V		1	2	µA
Over-Voltage Protection						
$V_{VRECT,OVPH}$	Hard OVP (AC1-AC2 short to VSSP) upper threshold	HOVP threshold	12		18	V
	Hard-OVP step size	HOVP threshold step size		2.0		
$V_{VRECT,OVPS}$	Soft OVP (IEXT clamping) upper threshold	SOVP threshold	9		16	V
		SOVP threshold step size		0.2		
		Hysteresis		1		
$I_{IEXT,MAX}$	IEXT clamping switch current capability	Non-repetitive 100 ms rectangular pulse			0.3	A
$R_{IEXT,ON}$	IEXT switch on-resistance	I_{IEXT} = 250 mA		1	2	Ω
Digital signals						
V_{IL}	Low level input voltage				0.54	V
V_{IH}	High level input voltage		1.26			
V_{OH}	GPIOx high level output voltage	Output high, I_{SOURCE} = 2mA	1.4			
I_{OH}	GPIOx pin current capability	Output high	3			mA
V_{OL}	Low level output voltage	Output low, I_{SINK}=3mA			0.4	V

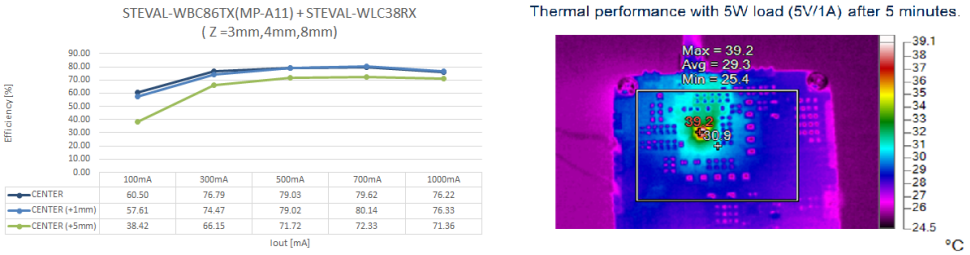
4.4 Recommended operating conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC characteristics						
$V_{VRECT,OP}$	Operating VRECT supply voltage range		4.5		13	V
$V_{VRECT,BPP}$	Operating VRECT supply voltage range in BPP mode	V_{VOUT} = 5 V, I_{VOUT} = 0.5 A	5.1	5.2	8	
AC characteristics						
V_{ACIN}	AC peak-to-peak voltage between AC1 and AC2 input pins				14	V
$I_{AC,MAX}$	AC1 and AC2 pins maximum RMS current capability	Sinusoidal waveform at AC1-AC2 terminals			1.25	A
f_{AC}	AC synchronous rectifier input frequency range		100		800	kHz

4.5 Typical characteristics

Measurements performed at room temperature (25°C) using evaluation boards STEVAL-WBC86 TX (MP-A11a) and STEVAL-WLC38RX (8uH Coil).

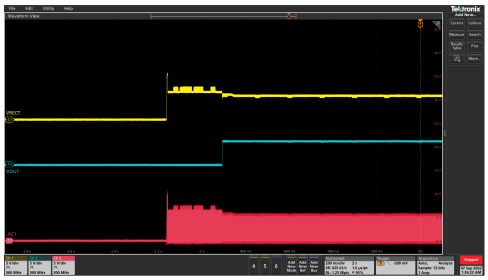
Figure 3. System efficiency and Thermal Performance 5V,1A



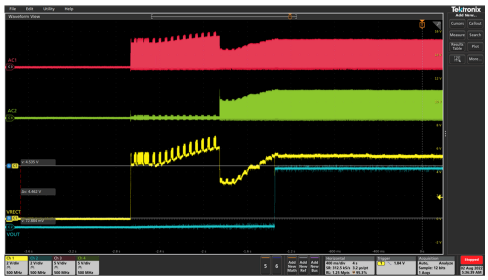
4.6 Start up waveforms

This section shows typical waveforms measured on AC1,AC2,VRECT,VOUT pins during receiver power up and ARC mode operation.

Figure 4. STWLC38 Power Up and ARC mode waveforms



Power-up of STEVAL-WLC38RX and STEVAL-WBC86TX.
Transmitter and Receiver coils are in aligned and with 500mA resistive load.



Functionality of ARC mode with Z gap (13mm).The ARC mode is active (AC2 is grounded) until VRECT threshold exceeds (6V by default), the ARC mode is disabled ,the rectifier operation mode changes and VOUT is enabled.

Color	Signal
YELLOW	VRECT
BLUE	VOUT
RED	AC1
GREEN	AC2

5 Device description

5.1 Chip-Enable Pin

When Chip-enable pin is set to HIGH , the device is in reset mode. Both rectifier low-side switches are turned-on while high-side switches are turned-off. After releasing the enable pin, STWLC38 can resume normal operational mode.

5.2 Synchronous rectifier

The synchronous rectifier of the STWLC38 is a key block in charge of converting the AC input power from the receiving coil into a DC supply rail for the following linear regulator.

In principle it consists of four N-channel MOSFETs arranged in an H-bridge, conveniently driven by a control block that monitors the voltage at the AC1 and AC2 pins to optimize the commutations and to charge the external bootstrap capacitors for the high-side switches.

Different driving schemes are possible for the switches of the rectifier and the MCU core dynamically selects the optimal one to maximize the overall efficiency as a function of the operating point.

When designing the filtering capacitor at the output of the synchronous rectifier, it must be taken into account that it has to minimize the AC residual ripple and to provide energy storage to sustain load transients, without impacting on the ASK communication with the transmitter.

5.3 ASK and FSK communication

Robust and reliable in-band ASK modulation is critical to the operation of any Qi compliant devices.

STWLC38 has dedicated hardware on top of the firmware algorithm to improve the performance of the in-band communication.

STWLC38 allows for two sets of modulation capacitors, namely COMA1/2 and COMB1/2. These 2 sets of ASK communication capacitors can be used in parallel or individually according to the load condition of the device. This allows for high level of flexibility to cater for a wide range of wireless transmitters.

STWLC38 comes with an advanced FSK demodulation filter which is able to remove any glitches present in the rectifier input.

The filter comes with a programmable masking pulse which is controlled by the firmware. This allows the firmware to adaptively control the filter to cater to different rectifier modes thereby ensuring robust FSK demodulation across the operating range.

5.4 ARC (Adaptive Rectifier Configuration) Mode

ARC (Adaptive Rectifier Configuration) mode improves the ping up and power transfer spatial freedom of the system in both X and Y direction.

Without any change in hardware or optimization of the coil, the ping up distance is enhanced by up to 50% in all directions by enabling ARC mode. This transforms the whole surface of the Tx to a usable area. Further enhancement is possible by customization of the coil.

Coil parameter tolerance requirements are widely relaxed due to ARC mode ping up feature. This is critical to wearables and hearables application where coils are of smaller and thinner dimensions, and it is relatively costlier to keep coil parameters within tight tolerances.

5.5 Protections

Over-voltage protection

The STWLC38 integrates different Over-Voltage Protection circuits to protect itself, the load connected to its output rail and the external components from damage due to overheating and/or exceeding AMR condition.

Under normal operating conditions the voltage at the output of the synchronous rectifier is slightly higher than the output one thanks to the communication with the transmitter.

A sudden change in the coupling factor between transmitting and receiving coils, for example due to abrupt reciprocal repositioning of the coils, easily leads to unpredictable voltage peaks at the AC input terminals: the TX-RX regulation loop is not fast enough to prevent such an event and additional precautions must be taken.

There are 3 over voltage protections, which are POVP, SOVP and HOVP.

- POVP (Ping Over Voltage Protection)
  During power-up when VAA and VDD are lower than UVLO threshold, POVP is triggered when VRECT > 14V, both rectifier low-side switches are turned-on while high-side switches are turned-off. POVP is released when VRECT < 11V.
- SOVP (Soft over voltage protection)
  When VRECT > VOUT + SOVP threshold, IEXT switch will be turned-on. SOVP threshold is programmable and can be set by PC GUI tool.
  SOVP is released when VRECT < SOVP threshold - 1V.
- HOVP (Hard Over voltage Protection)
  When VRECT > HOVP threshold, both rectifier low-side switches are turned on while high-side switches are turned-off. HOVP threshold is set by internal register. HOVP is released when VRECT < VOUT + SOVP release threshold, which is SOVP threshold - 1V.

Over-temperature protection

The STWLC38 is equipped with over-temperature detection circuits based on different sources:

- Internal temperature sensor
- external NTC temperature sensor
- TSHUT (hardware)

Over temperature protection(Software) The signals coming from the internal temperature sensors are conditioned and routed to the ADC. The temperature can be monitored in dedicated register. When the temperature exceeds set threshold level , it can turn off Main Voltage regulator (VOUT) , EPT can be sent to TX to stop power transfer.

The external sensor (NTC), typically placed very close to the coil to detect the over temperature of the coil , low-sided NTC of a resistor divider whose center tap is connected to the NTC pin(analog input), while the high-side resistor is connected to the VAA pin.

The temperature threshold is programmable by GUI.

If this function is not used, the pin must be pulled-up to VAA through a 10 kΩ resistor to prevent triggering the coil over-temperature protection.

TSHUT comparator monitor die temperature and turns off Main voltage regulator (VOUT) when temperature exceed set threshold level. The temperature threshold is programmable by GUI from 105 °C to 135 °C with 10 °C step (10 °C hysteresis).

When TSHUT is triggered both rectifier low-side switches are turned on while high-side switches are turned-off.

Over current Protection

The current limit is programmable (1.25A, 1.5A, 1.75A, 1.93A) , when output current exceed the set current limit , it can turn off Main Voltage regulator (VOUT) , EPT can be sent to TX to stop power transfer.

5.6 GPIOx and INTB pins

The GPIO0 through GPIO2 pins are programmable general-purpose I/O pins whose functions can be assigned in NVM memory. These pins can be configured both as inputs and outputs (either push-pull or open-drain) according to the selected function.

The INTB (GPIO3) pin is an interrupt output line that can be associated to any internal interrupt condition and used to inform the host system about specific events. The INTB pin is programmed as open-drain type.

5.7 RRAM (Resistive Random Access Memory)

STWLC38 has a 32kB RRAM which allows for multiple erase/re-write cycles.

This provides flexibility for custom firmware needed for various applications like proprietary protocols or field firmware upgrades.

RRAM also offers design in flexibility during preproduction optimization.

RRAM programming can be done in standalone mode, applying 5V (USB-VBUS 5V) to VOUT pin.

Using USB-I2C interface to PC GUI tool.

6 TX Mode

STWLC38 can be configured to Tx mode, it is capable of delivering output power up to 5W (coil dependent).

Input Voltage

The device can support wide range of input voltage of 5V up to 12V.

The power is applied to VOUT pin (VIN), which is the same VOUT pin when in Receiver Mode

Tx Inverter

The power transmitter uses a Full Bridge inverter, four N-channel MOSFETs arranged in an H-bridge.

The inverter converts the DC input into AC waveform that drives resonant circuit, which consists of Primary coil plus series capacitor.

The power transmitted to the coil is regulated by varying the switching frequency of the bridge.

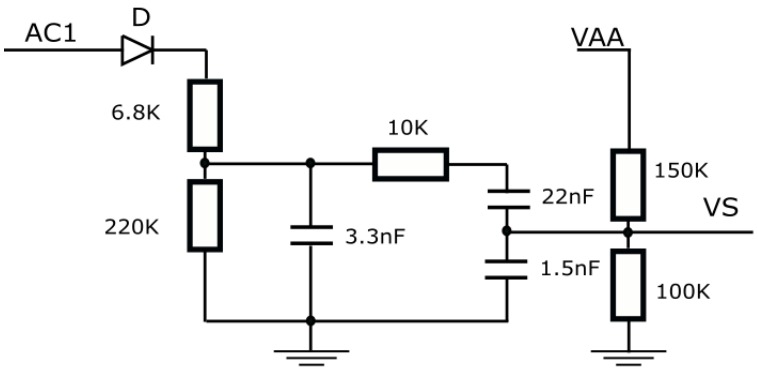
A higher the operating frequency (example 200kHZ) for lower transmitted power, while a lower operating frequency (example 110kHZ) for higher transmitted power.

ASK Demodulation

Using ASK (Amplitude Shift Keying) modulation, the power receiver regularly sends Control error Packets to tune operating point to match Load requirements.

Tx receives this modulated signal from AC1 input, the coil signal is conditioned using discrete filter circuit as shown below and fed into VS pin for demodulation.

Figure 5. ASK Demodulator Circuit



7 Wireless power interface

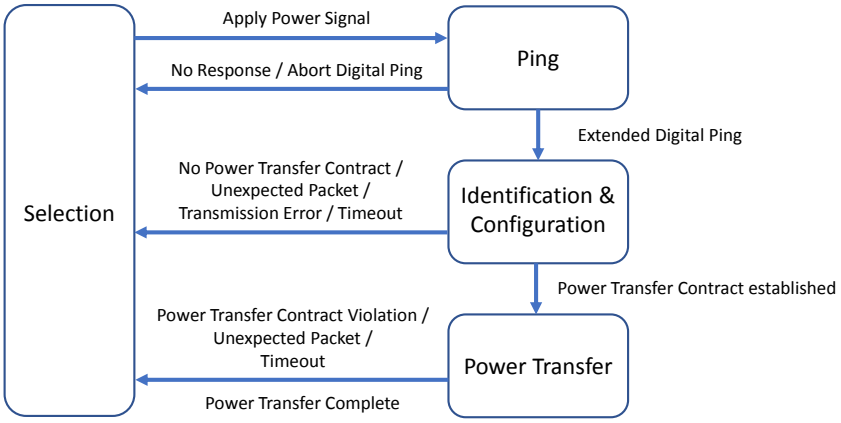
The blocks that refer to the wireless power interface are the synchronous rectifier, the main LDO linear regulator and the ASK modulator, as well as the digital core as supervisor. The power transfer from the transmitter to the receiver is established as a result of a procedure which consists of several distinct stages.

The power transfer begins after the transmitter has properly detected a valid receiver and a specific communication has been established between the two parts.

Power transfer phases

The flow-chart in Figure 6 reports the whole process of power transfer in Baseline Power Profile (BPP up to 1A@5V)

Figure 6. Power transfer phases for Baseline Power Profile



BPP power transfer phases

- Digital ping: this phase is an interrogation session based on a more energetic AC burst during which the potential receiver is expected to reply through amplitude shift-keying (ASK) modulation, the receiver device sends Signal strength packet.
- Identification & configuration: this phase is aiming to identify the receiver and to gather information about its power transfer capability. The transmitter generates a so-called “Power Transfer Contract” tailoring some parameters that will characterize the following power transfer phase.
- Power transfer: this is the final step, where the transmitter initially increases and subsequently modulates the transmitted power in response to the control (feedback) data from the receiver.

The flow-chart in below shows the whole process leading to a power transfer in Extended Power Profile (EPP) up to 1.25A@12V

Figure 7. Power transfer phases for Extended Power Profile

EPP power transfer phases

Without entering the details of the different phases, the basic sequence of events taking place when a receiver is properly placed on the transmitting coil are summarized as:

- Digital ping: this phase is an interrogation session based on a more energetic AC burst during which the potential receiver is expected to reply through amplitude shift-keying (ASK) modulation, the receiver device sends Signal strength packet.
- Identification & configuration: this phase is aiming to identify the receiver and to gather information about its power transfer capability. The transmitter generates a so-called “Power Transfer Contract” tailoring some parameters that will characterize the following power transfer phase.
- Negotiation: in this phase the Power Receiver negotiates with the Power Transmitter to fine tune the Power Transfer Contract.
- Power transfer: this is the final step, where the transmitter initially increases and subsequently modulates the transmitted power in response to the control (feedback) data from the receiver

STWLC38 goes autonomously through Selection, Ping, Identification & Configuration phases, entering Power Transfer phase if no error occurs.

During the Power Transfer phase, the device sends Received-Power and Control-Error packets periodically as feedback information for the transmitter.

If a critical event like over-voltage, over-current or over-temperature occurs, the STWLC38 automatically sends the End-Power-Transfer packet.

When the Power Transfer is up and running, the End-Power-Transfer packet (with any response value) or any custom packet (e.g. Proprietary packet or Charge-Status packet) can be sent to the transmitter simply through commands via I^2C interface.

Sending a custom packet may result in a reply (either a data packet or a pattern response from the transmitter) or no reply at all: if a response is received, the content is captured and stored in specific I^2C registers.

Important notes:

- Changing the output voltage must respect the overall system design (selected coil, transmitter type, etc.).
- Output load transient response strongly depends on a correct design of the output capacitors. Severe load transients may lead to temporary output voltage collapse due to the overall TX-RX response time.
- A minimal output load significantly helps in increasing the signal-to-noise ratio during digital ping and is advisable to ensure interoperability with all transmitters. For this purpose, the STWLC38 allows the user to set a dummy load (reservoir current) which is dynamically managed to fade-out when an output load is applied.
- The initial load at power-up should not exceed 2.5 W, smoothly ramping-up to full power subsequently.

8 I2C interface

The STWLC38 can operate fully independently, i.e. without being interfaced with a host system.

In applications in which the STWLC38 has to be a part of peripherals managed by the host system, the two SDA and SCL pins could be connected to the existing I²C bus.

The device works as an I²C slave and supports standard (100 kbps) fast (400 kbps) data transfer modes.

The STWLC38 has been assigned 0x61 7-bit hardware address. The pins are up to 3.3 V tolerant and the pull-up resistors should be selected as a trade-off between communication speed (lower resistors lead to faster edges) and data integrity (the input logic levels have to be guaranteed to preserve communication reliability).

When the bus is idle, both SDA and SCL lines are pulled HIGH.

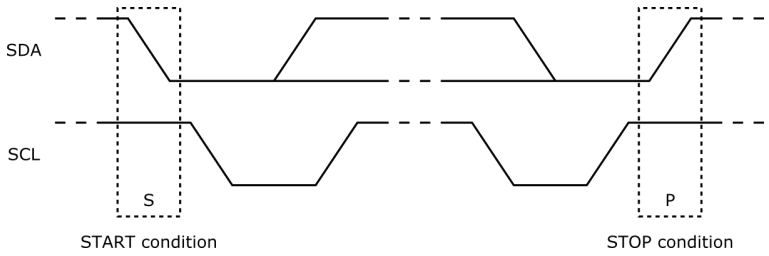
Data Validity

The data on the SDA line must be stable during the high period of the clock. The high and low states of the SDA line can only change when the SCL clock signal is low.

Start and Stop Conditions

Both the SDA and the SCL lines remain high when the I^2C bus is not busy. A START condition is a high-to-low transition of the SDA line when SCL is HIGH, while the STOP condition is a low-to-high transition of the SDA line when SCL is HIGH. A STOP condition must be sent before each START condition.

Figure 8. Start and Stop Condition on the I2C Bus



Byte format

Every byte transferred over the SDA line must contain 8 bits. Each byte received by the STWLC38 generally is followed by an acknowledge (ACK) bit. The MSB is transferred first. One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high state of each SCL clock pulse.

The device generates the ACK pulse (by pulling-down the SDA line during the acknowledge clock pulse) to confirm the correct device address or received data bytes.

Interface protocol

The interface protocol consists of

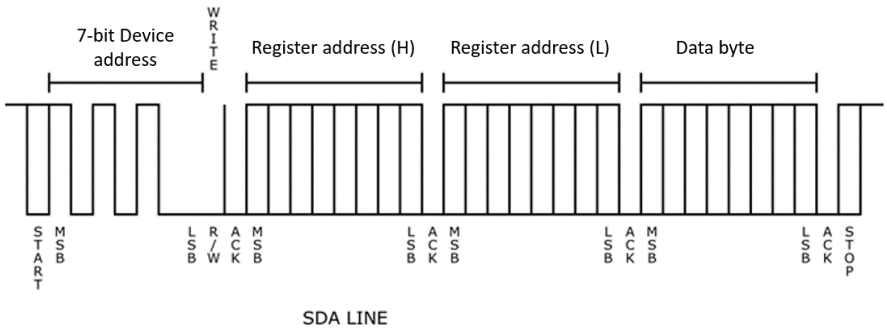
- Start condition (START)
- 7-bit device address (0x61) + R/W bit (read = 1 / write = 0)
- Register pointer, high-byte
- Register pointer, low-byte
- Data sequence: N x (data byte + ACK)
- Stop condition (STOP)

The register pointer (or address) byte defines the destination register to which the read or write operation applies. When the read or write operation is finished, the register pointer is automatically incremented.

Writing to a single register

Writing to a single register begins with a START condition followed by device address 0xC2 (7-bit device address plus R/W bit cleared), two bytes of the register pointer and the data byte to be written in the destination register. Each transmitted byte is acknowledged by the STWLC38 through an ACK pulse.

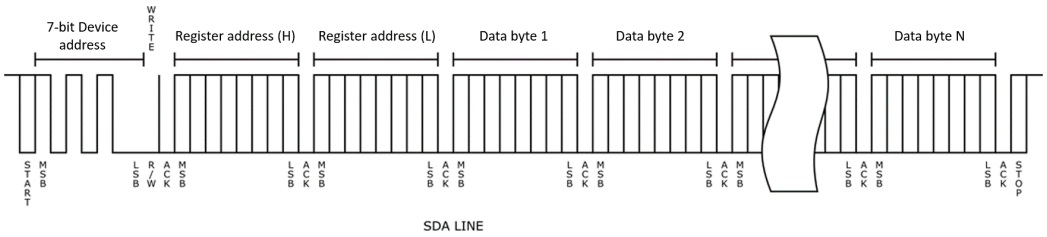
Figure 9. **Writing to single register byte**



Writing to multiple registers (page write)

The STWLC38 supports writing to multiple registers with auto-incremental addressing. When data is written into a register, the register pointer is automatically incremented, therefore transferring data to a set of subsequent registers (also know as page write) is a straightforward operation.

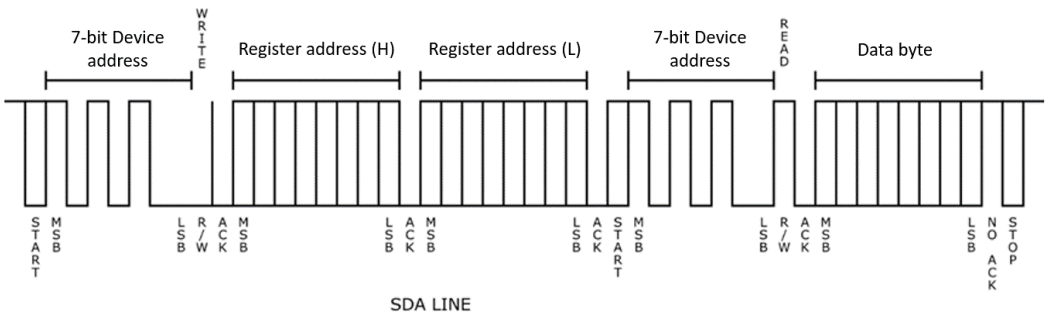
Figure 10. **Writing multiple register bytes**



Reading from a single register

Reading from a single register begins with a START condition followed by the device address byte 0xC2 (7-bit device address plus R/W bit cleared) and two bytes of register pointer, then a re-START condition is generated and the device address 0xC3 (7-bit device address plus R/W bit asserted) is sent, followed by data reading. ACK pulse is generated by the STWLC38 at the end of each byte, but not for data bytes retrieved from the register. A STOP condition is finally generated to terminate the operation.

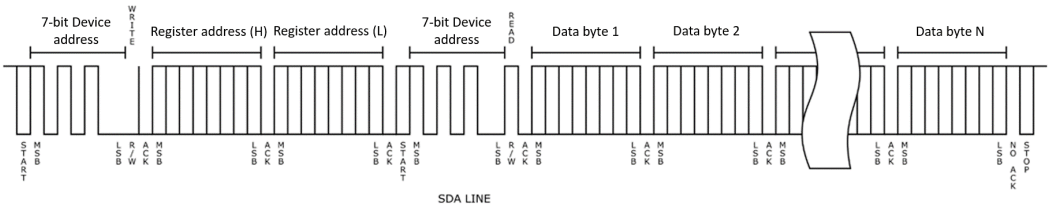
Figure 11. **Reading single register byte**



Reading from multiple registers (page reading)

Similarly to multiple (page) writing, reading from subsequent registers relies on an auto-increment of the register: the master can extend data reading to the following registers by generating and an ACK pulse at the end of each byte. Data reading starts immediately and the stream is terminated by a NMAK pulse at the end of the last data byte, followed by a STOP condition.

Figure 12. Reading multiple bytes



9 I2C register map

The STWLC38 can be monitored and controlled by accessing the internal registers via I^{2}C interface. The following registers map reports the accessible addresses. Addresses not shown in the map and blank bits have to be considered reserved and not altered as well.

These CFG parameters are accessible using the GUI tool, a new memh file needs to be generated after customized changes and to be Programmed in to NVM.

Table 5. Register abbreviations

Register type	Description
R/W	can read and write the bits
R	can read only
W	can write only
CFG	For customizing Configuration, accessible through GUI only.

Table 6. Chip information

Address	Register name	R/W	Default	Description
0x0000	Chip ID [Byte 0]	R	0x26	Chip ID [7..0]
0x0001	Chip ID [Byte 1]	R	0x00	Chip ID [15..8]
0x0002	Chip revision	R	0x03	Chip revision [7..0]
0x0003	Customer ID	R	0x00	Customer ID [7..0]
0x0004	ROM ID [Byte 0]	R	0x61	ROM ID [7..0]
0x0005	ROM ID[Byte 1]	R	0x00	ROM ID [15..8]
0x0006	NVM Patch ID[Byte 0]	R	-	NVM patch ID [7..0]
0x0007	NVM Patch ID[Byte 1]	R	-	NVM patch ID [15..8]
0x0008	RAM patch ID[Byte 0]	R	-	RAM patch ID [7..0]
0x0009	RAM patch ID[Byte 1]	R	-	RAM patch ID [15..8]
0x000A	Configuration ID[Byte 0]	R	-	Configuration ID [7..0]
0x000B	Configuration ID[Byte 1]	R	-	Configuration ID [15..8]
0x000C	Production ID[Byte 0]	R	0x07	PE ID [7..0]
0x000D	Production ID[Byte 1]	R	0x00	PE ID [15..8]
0x000E	Operation mode	R	0x02	0x1: Standalone (debug) mode 0x2: Qi RX mode 0x3: Qi TX mode
0x0010 ..0x001F	Device ID[Bytes 0 ..15]	R	-	Device ID Bytes 0 ...15

Table 7. System information

Address	Register name	R/W	Default	Description
0x0020	System command[Byte 0]	RW	-	Bit 0: Switch to TX command Write 1 to switch to Qi TX mode

Address	Register name	R/W	Default	Description
0x0020	System command[Byte 0]	-	-	Bit 1..7 Reserved
0x002C	System error information [Byte 0]	R	-	Bit 0: Core hard fault error 0: No hard fault error detected 1: Hard fault error detected
		R	-	Bit 1: HW WDT trigger latch 0: HW WDT not triggered 1: HW WDT triggered
		R	-	Bit 2: NVM IP error 0: No NVM IP error detected 1: NVM IP error detected
		R	-	Bit 3: Reserved Bit 4: NVM Boot error Bit 5..7 : Reserved
0x002D	System error [Byte 1]	R	-	Bit [1..0] NVM PE error 0: No error 1: Section header error 2: Section CRC failed 3: Reserved
		R	-	Bit [3..2] NVM Configuration error 0: No error 1: Section header error 2: Section CRC failed 3: Reserved
		R	-	Bit [5..4] NVM Patch error 0: No error 1: Section header error 2: Section CRC failed 3: Reserved
		R	-	Bits [7..6] NVM Production Information error 0: No error 1: Section header error 2: Section CRC failed 3: Reserved
		R		
0x002E	System error[Byte 2]	R	-	Reserved
0x002F	System error[Byte 3]	R	-	Reserved

Table 8. Communication

Address	Register name	R/W	Default	Description
0x00D8	RX DTS SEND LEN Byte 0,1	RW	-	DTS ADS number of data bytes in stream Byte 0 [7..0]
0x00D9				Byte 1 [7..0]
0x00DA	RX DTS SEND RQ Byte2	RW	-	Send ADC request Byte 2 Bits [4..0]

Address	Register name	R/W	Default	Description
				Bits[5..7] Reserved
0x00DC	RX DTS RCV LEN Byte 0 ,1	RW	-	DTS ADS number of bytes in stream received Byte 0 [7..0]
0x00DD				Byte 1 [7..0]
0x00DE	DTS RCV RQ[Byte 3]	R	-	Received ADC request Bits [4..0] Bits[5..7] Reserved
0x0090	RX SEND DTS	R		Bit 5 : Start sending DTS transaction , DTS send register specify the data to be send
0x0200 ..0 x27F	DTS SEND	RW	-	Total number of bytes can be sent 128. First 11Bytes shown in GUI
0x0280 ..0 x2FF	DTS RECV	R	-	Total number of bytes can be received 128. First 11Bytes shown in GUI

Table 9. Commands

Address	Register name	R/W	Default	Description
0x0020	Command	RW	-	SWITCH TO TX Bit 0: Switch to TX command Write 1 to switch to Qi TX mode

Table 10. Mode monitor

Address	Register name	R/W	Default	Description
0x0092	VRECT [Byte 0..1]	R	-	Rectifier voltage in mV [7..0]
0x0093				[15..8]
0x0094	VOUT[Byte 0..1]	R	-	Main LDO Voltage output in mV [7..0]
0x0095				Main LDO Voltage output in mV [15..8]
0x0096	ICUR[Byte 0..1]	R	-	Output current in mA [7..0]
0x0097				[15..8]
0x0098	TMEAS[Byte 0..1]	R	-	Chip temperature in deg C [7..0]
0xx099				[15..8]
0x009A	OP FREQ[Byte 0..1]	R	-	Operating frequency in kHz [7..0]
0x009B				[15..8]
0x009C	NTC [Byte 0 ..1]	R	-	NTC temperature measurement [7..0]
0x009D				[15..8]
0x00A4	RX VOLT DIFF [Byte 0..1]		-	Control Error: Rx voltage difference target and measured VRECT in mV [7..0]
0x00A5				[15..8]
0x00A6	POWER RX[Byte 0..1]	R	-	RX received power in mW [7..0]
0x00A7				[15..8]
0x00A8	SIG STREN[Byte0..1]	R	-	Signal strength measured in Rx [7..0]
0x00A9				[15..8]
	POWER TX	CFG		Power transferred to RX
	RX NEG STATE	CFG		Qi Power transfer Indicates BPP or EPP power transfer

Address	Register name	R/W	Default	Description
0x012A	TX DUTY	R		TX operating duty cycle [7..0]
	TX POWER RPP	CFG		Last value sent in Received Power Packet
	TX RECENT CEP	CFG		Last CEP value received from RX

Table 11. GPIO

Address	Register name	R/W	Default	Description
0x30	GPIO0 Func	RW	-	Please refer to GPIO configuration description.
0x31	GPIO1 Func	RW	-	Please refer to GPIO configuration description.
0x32	GPIO2 Func	RW	-	Please refer to GPIO configuration description.
0x33	GPIO3 Func	RW		Interrupt pin - INTB

GPIO configuration - alternate functions

- 0x00: GPIO configured as Input , FLOATING (Default)
- 0x01: GPIO configured as Input , Pull up resistor to internal 1.8V.
- 0x02: GPIO configured as Input ,Pull down resistor to Internal Ground.
- 0x03:GPIO configured as Interrupt pin , Open Drain output.
- 0x04:GPIO configured as Interrupt pin , Push pull output.
- 0x05:Initialization complete, FW ready (Active High).
- 0x06: Input to turn-off Main LDO block (Active High).
- 0x07:Input to Disable ASK communication (Active High).
- 0x0B: Input to Disable RX_POWEROUT after Negotiation- Push pull (Active High).
- 0x0C: Input to Disable RX_POWEROUT after Negotiation- Push pull (Active Low).
- 0x0D:Input to Disable RX_POWEROUT after Negotiation- Open Drain.
- 0x29: GPIO configured as Output , Open Drain (Active Low).
- 0x2A:GPIO configured as Output , Open Drain (Active High).
- 0x2B: GPIO configured as Output , Push pull (Active Low).
- 0x2C:GPIO configured as Output , Push pull (Active High).

Receiver mode (Rx) registers

Table 12. RX interrupts enable

Address	Register name	R/W	Default	Description
0x0080	RX Interrupt Enable[Byte 0]	RW	-	Bit 0:RX OVTP EN over temperature protection enable 0: disable 1: enable
		RW	-	Bit 1: RX OCP EN over current protection enable 0: disable 1: enable
		RW	-	Bit 2:RX OVP EN over voltage protection enable 0: disable 1: enable

Address	Register name	R/W	Default	Description
0x0080	RX Interrupt Enable[Byte 0]	RW	-	Bit 3: RX SYS ERROR EN system error enable 0: disable 1: enable
		RW	-	Bit4:Reserved
		RW	-	Bit5: RX MSG RCVD EN message received from TX enable 0: disable 1: enable
		RW	-	Bit6: RX OUTPUT ON EN output on interrupt enable 0: disable 1: enable
		RW	-	Bit7: RX OUTPUT OFF EN Output off interrupt enable 0: disable 1: enable
0x0081	RX Interrupt Enable[Byte 1]	RW	-	Bit0: RX SENT PACKET EN Packet sent interrupt enable 0: disable 1: enable
		RW	-	Bit1:RX SENT PKT TO EN Packet sending timeout interrupt enable 0: disable 1: enable
		RW	-	Bit2:RX SIG STR EN Signal Strength sent interrupt enable 0: disable 1: enable
		RW	-	Bit3:RX VRECT RDY EN VRECT ready interrupt enable 0: disable 1: enable
		RW	-	Bit4:RX UVLO EN under voltage protection interrupt enable 0: disable 1: enable
				Bit5,6,7: RESERVED
0x0082	RX Interrupt Enable[Byte 2]	RW	-	Bit0:RX DTS SEND SUCCESS EN DTS sending data stream successfully interrupt enable 0: disable 1: enable
		RW	-	Bit1: RX DTS SEND TO END EN DTS stopped sending due to timeout error interrupt enable

Address	Register name	R/W	Default	Description
0x0082	RX Interrupt Enable[Byte 2]			0: disable 1: enable
		RW	-	Bit2 : RX DTS SEND RESET END EN DTS stopped due to reset interrupt enable 0: disable 1: enable
		RW	-	Bit3: RESERVED
		RW	-	Bit4:RX DTS RCVD SUCCESS EN DTS received data stream successful interrupt enable 0: disable 1: enable
		RW	-	Bit 5:RX DTS RCVD TO END EN DTS stopped receiving due to timeout error interrupt enable 0: disable 1: enable
				Bit6:RX DTS RCVD RESET END EN DTS stopped receiving due to reset interrupt enable 0: disable 1: enable
		-	-	Bit 7: Reserved
0x0083	RX Interrupt Enable[Byte 3]	-	-	Reserved

Table 13. RX interrupt Clear

Address	Register name	R/W	Default	Description
0x0084	RX interrupt Clear[Byte 0]	R	-	Bit 0:RX OVTP CLR Over temperature protection clear 1: clear
		R	-	Bit 1:RX OCP CLR Over current protection clear 1: clear
		R	-	Bit 2:RX OVP CLR Over voltage protection clear 1: clear
		R	-	Bit 3:RX SYS ERROR CLR system error clear 1: clear
		R	-	Bit 4: Reserved
		R	-	Bit5:RX MSG RCVD CLR message received from TX clear 1: clear
		R	-	Bit6:RX OUTPUT ON CLR Output on interrupt clear

Address	Register name	R/W	Default	Description
				1: clear
0x0084	RX interrupt Clear[Byte 0]	R	-	Bit7: RX OUTPUT OFF CLR Output off interrupt clear 1: clear
0x0085	RX interrupt Clear[Byte 1]	R	-	Bit0:RX SENT PACKET CLR Packet sent interrupt clear 1: clear
		R	-	Bit1:RX SENT PKT TO CLR Packet sending timeout interrupt clear 1: clear
		R	-	Bit2:RX SIG STR CLR Signal Strength sent interrupt clear 1: clear
		R	-	Bit3:RX VRECT RDY CLR VRECT ready interrupt clear 1: clear
		R	--	Bit4: RX UVLO CLR under voltage protection interrupt clear 1: clear
		R	-	Bit5,6,7: RESERVED
0x0086	RX interrupt Clear[Byte 2]	R	-	Bit0:RX DTS SEND SUCCESS CLR DTS sending data stream successfully interrupt clear 1: clear
		R	-	Bit1:RX DTS SEND TO END CLR DTS stopped sending due to timeout error interrupt clear 1: clear
		R	-	Bit2:RX DTS SEND RESET END CLR DTS stopped due to reset interrupt clear 1: clear
		R	-	Bit3: RESERVED
		R	-	Bit4: RX DTS RCVD SUCCESS CLR DTS received data stream successful interrupt clear 1: clear
		R	-	Bit5:RX DTS RCVD TO END CLR DTS stopped receiving due to timeout error interrupt clear 1: clear
		R	-	Bit6:RX DTS RCVD RESET END CLR DTS stopped sending due to reset interrupt clear 1: clear
		-	-	Bit7: Reserved
0x0087	RX interrupt Clear[Byte 3]	-	-	Reserved

Table 14. **RX interrupt latch**

Address	Register name	R/W	Default	Description
0x0088	RX interrupt latch[Byte 0]	R	-	Bit 0:RX OVTP LTCH over temperature protection latch
		R	-	Bit 1: RX OCP LTCH over current protection latch
		R	-	Bit 2: RX OVP LTCH over voltage protection latch
		R	-	Bit 3:RX SYS ERROR LTCH system error latch
		R	-	Bit4: Reserved
		R	-	Bit5:RX MSG RCVD LTCH message received from TX latch
		R	-	Bit6:RX OUTPUT ON LTCH Output on interrupt latch
		R	-	Bit7: RX OUTPUT OFF LTCH Output off interrupt latch
0x0089	RX interrupt latch[Byte 1]	R	-	Bit0:RX SENT PACKET LTCH Packet sent interrupt latch
		R	-	Bit1:RX SENT PKT TO LTCH Packet sending timeout interrupt latch
		R	-	Bit2:RX SIG STR LTCH Signal Strength sent interrupt latch
		R	-	Bit3:RX VRECT RDY LTCH VRECT ready interrupt latch
		R	-	Bit4:RX UVLO LTCH under voltage protection interrupt latch
		R	-	Bit5,6,7: RESERVED
0x008A	RX interrupt latch[Byte 2]	R	-	Bit0:RX DTS SEND SUCCESS LTCH DTS sending data stream successfully interrupt latch
		R	-	Bit1:RX DTS SEND TO END LTCH DTS stopped sending due to timeout error interrupt latch
		R	-	Bit2:RX DTS SEND RESET END LTCH DTS stopped due to reset interrupt latch
		R	-	Bit3: RESERVED
		R	-	Bit4:RX DTS RCVD SUCCESS LTCH DTS received data stream successful interrupt latch
		R	-	Bit 5:RX DTS RCVD TO END LTCH DTS stopped receiving due to timeout error interrupt latch
		R	-	Bit6:RX DTS RCVD RESET END LTCH DTS stopped sending due to reset interrupt latch
		-	-	Bit 7 : Reserved
0x008B	RX interrupt latch[Byte 3]	-	-	Reserved

Table 15. **RX interrupt status**

Address	Register name	R/W	Default	Description
0x008C	RX interrupt status[Byte 0]	R	-	Bit 0: RX OVTP STAT over temperature protection status
		R	-	Bit 1:RX OCP STAT over current protection status
		R	-	Bit 2:RX OVP STAT over voltage protection status
		R	-	Bit 3:RX SYS ERROR STAT system error status
		R	-	Bit4:Reserved
		R	-	Bit5:RX MSG RCVD STAT message received from TX status
		R	-	Bit6:RX OUTPUT ON STAT Output on interrupt status
		R	-	Bit7:RX OUTPUT OFF STAT Output off interrupt status
0x008D	RX interrupt status[Byte 1]	R	-	Bit0: RX SENT PACKET STAT Packet sent interrupt status
		R		Bit1:RX SENT PKT TO STAT Packet sending timeout interrupt status
		R	-	Bit2:RX SIG STR STAT Signal Strength sent interrupt status
		R	-	Bit3:RX VRECT RDY STAT VRECT ready interrupt status
		R	-	Bit4: RX UVLO STAT under voltage protection interrupt status
		R		Bit5,6,7: RESERVED
0x008E	RX interrupt status[Byte 2]	R	-	Bit0:RX DTS SEND SUCCESS STAT DTS sending data stream successfully interrupt status
		R	-	Bit1:RX DTS SEND TO END STAT DTS stopped sending due to timeout error interrupt status
		R	-	Bit2:RX DTS SEND RESET END STAT DTS stopped due to reset interrupt status
			-	Bit3: RESERVED
		R	-	Bit4:RX DTS RCVD SUCCESS STAT DTS received data stream successful interrupt status
		R	-	Bit 5:RX DTS RCVD TO END STAT DTS stopped receiving due to timeout error interrupt status
		R	-	Bit6:RX DTS RCVD RESET END STAT DTS stopped sending due to reset interrupt status
		-	-	Bit7: Reserved
0x008F	RX interrupt status[Byte 3]	-	-	Reserved

Table 16. **RX commands**

Register address	Register name	R/W	Default	Description
0x00CF	RX command	RW	-	RX EPT MSG
			-	EPT reason to be included when sending EPT packet 0x0 : EPT/nul
			-	use if none of the other codes is appropriate.
			-	0x1: EPT/cc
			-	charge complete; use to indicate that the battery is full.
			-	0x2: EPT/if
			-	internal fault; use if an internal logic error has been encountered.
			-	0x3: EPT/ot
			-	over temperature, use if (e.g.) the battery temperature exceeds a limit.
			-	0x4: EPT/ov
				over voltage; use if a voltage exceeds a limit. 0x5: EPT/oc
				over current; use if the current exceeds a limit.
				0x6: EPT/bf
				battery failure: use if the battery cannot be charged.
				0x8:EPT/nr
				no response: use if the target operating point cannot be reached.
				0xA:EPT/an
				aborted negotiation: use if a suitable Power Transfer Contract cannot be negotiated.
				0xB: EPT/rst
				restart; use to restart the power transfer
0x0090		RW	-	Bit0: RX VOUT ON Turn on the VOUT. If both VOUT_ON and VOUT_OFF are set to 1, this command is ignored and both requests are cleared.
		RW	-	Bit1: RX VOUT OFF Turn off the VOUT. If both VOUT_ON and VOUT_OFF are set to 1, this command is ignored and both requests are cleared.
		RW	-	Bit4:RX SEND EPT Send End of Power Packet to TX
		-	-	Bits [3,5,6,7] Reserve

Table 17. **RX Configuration**

Address	Register name	R/W	Default	Description
0x00B1	RX BPP VOUT SET[Byte 0]	RW	-	Bits [7..0] RX VOUT_SET Low Bits [7..6] lower 2 bits of VOUT set 00 : 0mV 01:25mV

Address	Register name	R/W	Default	Description
				10:50mV 11 : 75mV Bits [5..0] Reserved
0x00B2	RX BPP VOUT SET[Byte 1]	RW	-	Bits [7..0] RX VOUT_SET High Program VOUT output voltage 0.5V to 13.2V, step size 0.1V, step0 --> 0.5V 1 --> 0.6V..5 --> 1.0V.. 15 --> 2.0V.. 45 --> 5.0V.. 73 --> 12V
	RX EPP VOUT SET[Byte 0]	CFG	-	Bits [7..0] RX VOUT_SET Low Bits [7..6] lower 2 bits of VOUT set 00 : 0mV 01:25mV 10:50mV 11 : 75mV Bits [5..0] Reserved
	RX EPP VOUT SET[Byte 1]	CFG	-	Bits [7..0] RX VOUT_SET High Program VOUT output voltage 0.5V to 13.2V, step size 0.1V , step0 --> 0.5V 1 --> 0.6V..5 --> 1.0V.. 15 --> 2.0V.. 45 --> 5.0V.. 73 --> 12V
	RX Dummy LOAD configuration	CFG	-	Bit[7..5]:RX ILOAD BALAST ILOAD ballast mode current 00:8mA 01:16mA 10:24mA 11:32mA
	RX ARC Mode configuration	CFG	0x3C	Bit[7..0]:RX ARC THRES ARC mode auto off VRECT threshold steps of 10mV Default : 0x3C --> 6V Maximum : 0x82 --> 13V
	RX VOUT configuration[Byte1]	CFG	-	Bit 7:RX IVL EN Enable Input voltage loop
	RX VOUT configuration[Byte2]	CFG	-	Bit [4..0]:RX IVL THRES IVL threshold setting u = 0 .. 15 steps 3V +u * 0.5
	RX VOUT configuration[Byte1]	CFG	-	Bit 4:RX UVLO EN VRECT UVLO detection enable
	RX VOUT configuration[Byte1]	CFG	-	Bit [3..0]:RX UVLO THRES VRECT UVLO Threshold setting u = 0 .. 15 steps 3.5V + u*0.5
	RX VOUT configuration	CFG	-	Bit0:RX VOUT AUTO EN Allow VOUT turn on when no feature is blocking it. If disabled, VOUT must be enabled manually by I2C command
	RX VOUT configuration	CFG	-	Bit[7..0]:RX VRECT RDY THRES

Address	Register name	R/W	Default	Description
				VRECT must be higher by this value. Otherwise VOUT cannot be enabled

Example :
VOUT SET = 5V ; 0x00B2 = 2D ; 0x00B1 [7..6] = 00
VOUT SET = 5.075V ; 0x00B2 = 2D; 0x00B1[7..6] = 11

Table 18. RX LDO configuration

Address	Register name	R/W	Default	Description
0x00C8	RX LDO DROP 0	RW	-	Bits[7..0] LDO target voltage drop at 0mA IOUT. Specified in 16mV units. Set point 0
0x00C9	RX LDO DROP 1	RW	-	Bits[7..0] LDO target voltage drop at ldo_cur_thres1 IOUT. Specified in 16mV units. Set point 1
0x00CA	RX LDO DROP 2	RW	-	Bits [7..0] LDO target voltage drop at ldo_cur_thres2 IOUT. Specified in 16mV units. set point 2
0x00CB	RX LDO DROP 3	RW	-	Bits [7..0] LDO target voltage drop at ldo_cur_thres3 IOUT. Specified in 16mV units. set point 3
0x00CC	RX LDO CUR TH1	RW	-	Bits [7..0] LDO voltage drop IOUT current threshold 1. Specified in 8mA units.
0x00CD	RX LDO CUR TH2	RW	-	Bits [7..0] LDO voltage drop IOUT current threshold 2. Specified in 8mA units.
0x00CE	RX LDO CUR TH3	RW	-	Bits [7..0] LDO voltage drop IOUT current threshold 3. Specified in 8mA units.

Table 19. RX BPP FOD configuration

Address	Register name	R/W	Default	Description
	RX BPP FOD CUR THR1	CFG	-	Bits [7..0] FOD current threshold 1, in units of 10mA.
	RX BPP FOD CUR THR2	CFG	-	Bits [7..0] FOD current threshold 2, in units of 10mA.
	RX BPP FOD CUR THR3	CFG	-	Bits [7..0] FOD current threshold 3, in units of 10mA.
	RX BPP FOD CUR THR4	CFG	-	Bits [7..0] FOD current threshold 4, in units of 10mA.
	RX BPP FOD CUR THR5	CFG	-	Bits [7..0] FOD current threshold 5, in units of 10mA.
	RX BPP FOD OFFSET 0	CFG	-	Bits [7..0] FOD offset at current 0, in units of 8mW.
	RX BPP FOD OFFSET 1	CFG	-	Bits [7..0] FOD offset at current 1, in units of 8mW.
	RX BPP FOD OFFSET 2	CFG	-	Bits [7..0] FOD offset at current 2, in units of 8mW.
	RX BPP FOD OFFSET 3	CFG	-	Bits [7..0] FOD offset at current 3, in units of 8mW.
	RX BPP FOD OFFSET 4	CFG	-	Bits [7..0] FOD offset at current 4, in units of 8mW.
	RX BPP FOD OFFSET 5	CFG	-	Bits [7..0] FOD offset at current 5, in units of 8mW.
	RX BPP FOD RSER	CFG	-	Bits [7..0] Coil series resistance, in units of 4mOhm.

Table 20. RX EPP FOD configuration

Address	Register name	R/W	Default	Description
	RX EPP FOD CUR THR1	CFG	-	Bits [7..0] EPP FOD current threshold 1, in units of 10mA.
	RX EPP FOD CUR THR2	CFG	-	Bits [7..0] EPP FOD current threshold 2, in units of 10mA.
	RX EPP FOD CUR THR3	CFG	-	Bits [7..0] EPP FOD current threshold 3, in units of 10mA.
	RX EPP FOD CUR THR4	CFG	-	Bits [7..0] EPP FOD current threshold 4, in units of 10mA.
	RX EPP FOD CUR THR5	CFG	-	Bits [7..0] EPP FOD current threshold 5, in units of 10mA.
	RX EPP FOD OFFSET 0	CFG	-	Bits [7..0] EPP FOD offset at current 0, in units of 8mW.
	RX EPP FOD OFFSET 1	CFG	-	Bits [7..0] EPP FOD offset at current 1, in units of 8mW.
	RX EPP FOD OFFSET 2	CFG	-	Bits [7..0] EPP FOD offset at current 2, in units of 8mW.
	RX EPP FOD OFFSET 3	CFG	-	Bits [7..0] EPP FOD offset at current 3, in units of 8mW.
	RX EPP FOD OFFSET 4	CFG	-	Bits [7..0] EPP FOD offset at current 4, in units of 8mW.
	RX EPP FOD OFFSET 5	CFG	-	Bits [7..0] EPP FOD offset at current 5, in units of 8mW.
	RX BPP FOD RSER	CFG	-	Bits [7..0] Coil series resistance, in units of 4mOhm.

Table 21. RX protections

Address	Register name	R/W	Default	Description
	RX protections[Byte 0]	CFG	-	Bit 0: RX ADC OVTP EN PROT Enable to compare chip temperature against VTMEAS threshold. AC1/2 will be shorted to ground.
				Bit1 : Reserved
			-	Bit2:RX ADC NTC EN PROT Enable to compare NTC temperature against NTC threshold. If enabled, interrupt status and latch OVTP_INTR are updated on threshold reach.
			-	Bit3:RX TSHUT EN PROT Enable to compare temperature against TSHUT threshold. AC1/2 will be shorted to ground
			-	Bit4: Reserved
				Bits [5..7] Reserved
	RX Protections [Byte 1]	CFG	-	Bit0: RX ADC OVP EN PROT Enable to compare VRECT voltage against OVP threshold. If enabled, interrupt status and latch OVP_INTR are updated on threshold reach.
				Bit1: Reserved
			-	Bit 2:RX SOVP EN PROT Enable to compare VRECT against SOVP threshold.
				Bit [3..4] Reserved
			-	Bit5:RX SCP EN PROT Enable VOUT short detection. If enabled, interrupt status and latch OVP_SCP are updated on detection.
			-	Bit 6:RX UVLO EN PROT Under voltage protection. Enable to compare voltage against UVLO threshold. If enabled, interrupt status and latch UVLO_INTR are updated on threshold reach.
			-	Bit7:Reserved

Address	Register name	R/W	Default	Description
	RX Protections [Byte 2]	CFG	-	Bit0:RX ADC OCP EN PROT Enable to compare current against OCP threshold. If enabled, interrupt status and latch OCP_INTR are updated on threshold reach.
			-	Bit1:RX OCP EN PROT Enable to compare VOUT current against current threshold. Interrupt status and latch OCP_INTR are updated on threshold reach.
				Bits[2..7] Reserved
	RX Protections [Byte 3]			Reserved
	RX Protections (EPT) [Byte 0]	CFG	-	Bit0:RX ADC OVTP EPT Send EPT when OVTP ADC threshold is reached. RX OVTP ADC EN PROT must be enabled for this to work.
			-	Bit1: Reserved
			-	Bit2:RX ADC NTC EPT Send EPT when NTC ADC threshold is reached. RX NTC ADC EN PROT must be enabled for this to work.
			-	Bit3:RX TSHUT EPT Send EPT when TSHUT threshold is reached. RX TSHUT EN PROT must be enabled for this to work.
				Bits[4..7] Reserved
	RX Protections (EPT) [Byte 1]	CFG	-	RX ADC OVP EPT Bit0 Send EPT when OVP ADC threshold is reached. RX OVP ADC EN PROT must be enabled for this to work.
				Bit 1 : Reserved
				Bit2: RX SOVP EPT Send EPT when SOVP threshold is reached. RX SOVP EN PROT must be enabled for this to work.
				Bit4: Reserved
			-	Bit4:RX SCP EPT Send EPT when VOUT short is detected. RX SCP EN PROT must be enabled for this to work.
			-	Bit5:RX UVLO EPT Send EPT when UVLO threshold is reached. RX UVLO EN PROT must be enabled for this to work.
			-	Bit6: Reserved
			-	Bit7:RX HOVP EPT Send EPT when HOVP threshold is reached. RX HOVP PROT must be enabled for this to work.
	RX Protections (EPT) [Byte 2]	CFG	-	Bit0:RX ADC OCP EPT Send EPT when OCP ADC threshold is reached. RX OCP ADC EN PROT must be enabled for this to work.
			-	Bit1:RX OC EPT Send EPT when OCP threshold is reached. RX OCP EN PROT must be enabled for this to work.
				Bits[2..7] Reserved
	RX Protections (EPT) [Byte 3]			Reserved

Address	Register name	R/W	Default	Description
	RX Protection (VOUT)[Byte 0]	CFG	-	Bit0:RX ADC OVTP VOUT OFF Turns VOUT OFF when OVTP ADC threshold is reached. RX OVTP ADC EN PROT must be enabled for this to work.
				Bit1: Reserved
		CFG	-	Bit2:RX ADC NTC VOUT OFF Turns VOUT OFF when NTC ADC threshold is reached. RX NTC ADC EN PROT must be enabled for this to work.
		CFG	-	Bit3:RX TSHUT VOUT OFF Turns VOUT OFF when TSHUT threshold is reached. RX TSHUT EN PROT must be enabled for this to work.
		CFG	-	Bit4:Reserved
		-	-	Bits[5..7] Reserved
	RX Protection (VOUT)[Byte 1]	CFG	-	Bit0:RX ADC OVP VOUT OFF Turns VOUT OFF when OVP ADC threshold is reached. RX OVP ADC EN PROT must be enabled for this to work.
				Bit1 : Reserved
		CFG	-	Bit2:RX SOVP VOUT OFF Turns VOUT OFF when SOVP threshold is reached. RX SOVP EN PROT must be enabled for this to work.
				Bits3: Reserved
		CFG	-	Bit4:RX SCP VOUT OFF Turns VOUT OFF when VOUT short is detected. RX SCP EN PROT must be enabled for this to work.
		CFG	-	Bit5:RX UVLO VOUT OFF Turns VOUT OFF when UVLO threshold is reached. RX UVLO EN PROT must be enabled for this to work.
		-	-	Bit6: Reserved
		CFG	-	Bit7:RX HOVP VOUT OFF Turns VOUT OFF when HOVP threshold is reached. RX HOVP EN PROT must be enabled for this to work.
	RX Protection (VOUT)[Byte 2]	CFG	-	Bit0:RX ADC OCP VOUT OFF Turns VOUT OFF when OCP ADC threshold is reached. RX OCP ADC EN PROT must be enabled for this to work.
			-	Bit1:RX OCP VOUT OFF Turns VOUT OFF when OCP threshold is reached. RX OCP EN PROT must be enabled for this to work.
				Bits [2..7] Reserved
	RX Protection (VOUT)[Byte 3]	CFG	-	Bits [7..0] Reserved

Table 22. RX Power transfer contract

Address	Register name	R/W	Default	Description
0x00AA	Rx Power Transfer Contract [Byte 0]			Bits[7..0] Reserved
0x00AB	Rx Power Transfer Contract [Byte 1]	RW	-	Bit[5..0]:RX MAX POWER Qi 1.3 Reference Power Field. This value should be 2x of power in watt. Qi spec max is 63/2 watt.

Address	Register name	R/W	Default	Description
0x00AB	Rx Power Transfer Contract [Byte 1]	RW	-	Bits[6..7] Reserved
	Rx Power Transfer Contract [Byte 2]	CFG	-	Bits[3..0] Reserved
			-	Bit4:RX OB Qi Power transfer contract. Out-of-band communications functionality. 1: supported 0: not supported
			-	Bit5 :Reserved
			-	Bit6:RX AI Qi Power transfer contract. Authentication functionality . 1: supported 0: not supported
			-	Bit 7 Reserved
	Rx Power Transfer Contract [Byte 3]	CFG	-	Bit[2..0]:RX WIN OFFSET Received Power window offset. Specified in units of 4ms. Keep default value (changing requires system level review).
		CFG	-	Bit[7..3]:RX WIN SIZE Received Power window size. Specified in units of 4ms. Keep default value (changing requires system level review).
	Rx Power Transfer Contract [Byte 4]	CFG		Bit0:RX DUP Qi Power transfer contract. Simultaneous incoming and outgoing data streams. 1: supported 0: not supported
		CFG		Bit [3..1]:RX BUF SIZE Qi Power Transfer Contract. The size of the transport-layer buffer for receiving a data transport stream. The number of bytes in the buffer is equal to 16*2^n, with n the value contained in the Buffer Size field.\n Range 16 to 2048 bytes.
		CFG		Bit[5..4]:RX FSK MOD DEPTH Qi Power Transfer contract. FSK modulation depth. The value is 1/fmod - 1/fop in ns. Depends on configured fsk polarity. Stated as MINIMUM~MAXIMUM (for positive polarity)/MINIMUM~MAXIMUM (for negative polarity)
		CFG	-	Bit6:RX POL Qi Power transfer contract. The requested FSK polarity is positive (ZERO) or negative (ONE).
		CFG	-	Bit7:RX NEG Qi Power transfer contract. The Extended Protocol is supported (ONE) or not supported (ZERO). If the Neg bit is set to ZERO, all bits of the AI, OB, Pol, and Depth fields shall be set to ZERO as well.

Table 23. RX configuration Qi

Address	Register name	R/W	Default	Description
	RX configuration Qi	CFG	-	Bit[7..0]:RX BPP FOD QF

Address	Register name	R/W	Default	Description
	RX configuration Qi			Reference Quality factor which will be sent during negotiation in FOD/qf packet. Determination of this value is defined in Qi specification
		CFG	-	Bit[7..0]:RX BPP FOD RF Reference Resonance frequency which will be sent during negotiation in FOD/rf packet. Determination of this value is defined in Qi specification.
		CFG	-	Bit[2..0]:RX CE DENOM Control error denominator. Value is set value +1
		CFG	-	Bit[5..3]:RX CE NUM Control error numerator. Value is set value +1
		-	-	Bits[7..6] : Reserved
		CFG	-	Bit[2..0]:RX DTS PKT LEN Number of bytes in each DTS transaction. DTS ADT packet message length for outgoing stream.
		-	-	Bits[7..3] Reserved
		CFG	-	Bit[6..0]:RX CE MAX Maximal abs value of control error. 0 = no limitation.
		CFG	-	Bit6:RX RP24 REPLY RP24 request FSK reply
		CFG	-	Bit7:RX RP24 NACK LDO OFF Turn off LDO automatically when TX send NACK to RP24
		CFG	-	Bit[2..0]:RX SS DENOM Signal strength denominator. Value is set value +1
		CFG	-	Bit[5..3]:RX SS NUM Signal strength numerator. Value is set value +1
		-	-	Bit [7..6] Reserved
		CFG	-	Bit[7..0]:RX SS MIN Minimal value of signal strength

Table 24. RX ASK configuration

Address	Register name	R/W	Default	Description
	RX ASK MOD IOUT THRES	CFG	120mA	Bit [7..0] Setting current threshold to switch ASK modulation capacitors Step size 8mA
	RX ASK MOD IOUT HYST	CFG		Bit[7..0] Hysteresis for Current threshold to switch modulation capacitors configurations. The current must be lower than (threshold-hysteresis to switch from high current config to low current config.
	RX ASK MOD VOUT THRES	CFG	8V	Bit[7..0] Setting voltage threshold to switch ASK modulation capacitors Step size 100mV

Address	Register name	R/W	Default	Description
				Maximum : 0x0D : 13V
	ASK MOD Setting[Byte 0]	CFG	1	Bit4:LC HV ASK MOD A1 Modulation capacitor used for under current higher voltage state of mod A
		CFG	1	Bit5:LC HV ASK MOD B1 Modulation capacitor used for under current higher voltage state of mod B
		-	-	Bits 0,1,2,3,6,7 : Reserved
	ASK MOD Setting[Byte 1]	CFG	1	Bit4:LC LV ASK MOD A1 Modulation capacitor used for under current and voltage state of mod A
		CFG	1	Bit5:LC LV ASK MOD B1 Modulation capacitor used for under current and voltage state of mod B
		-	-	Bits 0,1,2,3,6,7 : Reserved
	ASK MOD Setting[Byte 2]	CFG	0	Bit4:NC HV ASK MOD A1 Modulation capacitor used for normal current and higher voltage state of mod A
		CFG	1	Bit5:NC HV ASK MOD B1 Modulation capacitor used for normal current and higher voltage state of mod B
		-	-	Bits 0,1,2,3,6,7 : Reserved
	ASK MOD Setting[Byte 3]	CFG	0	Bit4:NC LV ASK MOD A1 Modulation capacitor used for normal current and under voltage state of mod A
		CFG	1	Bit5:NC LV ASK MOD B1 Modulation capacitor used for normal current and under voltage state of mod B
		-	-	Bits 0,1,2,3,6,7 : Reserved

The default settings are optimized for light and high load conditions.

Table 25. RX Protection threshold

Address	Register name	R/W	Default	Description
	RX Protection threshold	CFG	1.75A	RX OCP SEL Over current protection threshold 0x00 : 1.25A 0x01 : 1.5A 0x02 : 1.75A 0x03 : 1.93A
		CFG	16V	RX THRES HOVP Bits [2..0] Hard Over voltage protection 0x00 : 6.0V 0x01 : 8.0V …... 0x06 : 16V 0x07:18V
		CFG	4V	RX SOVP THRES Bits [6..3] Soft Over voltage protection 0x00 : VOUTSET +2.0V 0x01 :VOUTSET + 2.2V …... 0x0F : VOUTSET+ 5.0V
		CFG		RX THRES NTC Bits [15..0] NTC ADC threshold setting
		CFG		RX THRES OCP ADC Bits [15..0] Over current protection ADC threshold setting
		CFG		RX THRES OVTP Bits [15..0] Over temperature protection ADC threshold setting
		CFG		RX THRES VRECT Bits[15..0] VRECT Over voltage protection ADC threshold setting
		CFG	115°C	RX TSHUT SEL Bits [1..0] 0x00 : 105°C 0x01 : 115°C 0x02 : 125°C 0x03 : 135°C

Table 26. RX Qi chip ID

Address	Register name	R/W	Default	Description
	RX 01 MFR ID H[Byte 1]	RW	-	Bit[15..8] Manufacturer ID high byte in ID packet
	RX 02 MFR ID L [Byte 0]	RW	-	Bit[7..0] Manufacturer ID low byte in ID packet
	RX 03 BDID HH [Byte 1]	RW	-	Bit[6..0] Basic device ID, byte 1.(only 7bit available).
		RW	-	Bit7: XID EN Enables extended id.
	RX 04 BDID HL [Byte 2]	RW	-	Basic device ID, byte 2.
	RX 05 BDID LH [Byte 3]	RW	-	Basic device ID, byte 3.
	RX 06 BDID LL [Byte 4]	RW	-	Basic device ID, byte 4.
	RX 07 XID HHH [Byte 1]	RW	-	Extended device ID, byte 1.

Address	Register name	R/W	Default	Description
	RX 08 XID HHL[Byte 2]	RW	-	Extended device ID, byte 2.
	RX 09 XID HLH [Byte3]	RW	-	Extended device ID, byte 3.
	RX 10 XID HLL [Byte 4]	RW	-	Extended device ID, byte 4.
	RX 11 XID LHH [Byte5]	RW	-	Extended device ID, byte 5.
	RX 12 XID LHL [Byte 6]	RW	-	Extended device ID, byte 6.
	RX 13 XID LLH [Byte 7]	RW	-	Extended device ID, byte 7.
	RX 14 XID LLL [Byte 8]	RW	-	Extended device ID, byte 8.

Transmitter mode (TX) registers

Table 27. TX Commands

Address	Register name	R/W	Default	Description
0x0110	TX command [Byte 0]	RW	-	Bit0: TX EN Enable the TX. Write 1 to start Ping
		RW	-	Bit1: TX DIS Disable the TX. Write 1 to stop the inverter and cut the power to Rx
0x0111	TX command [Byte 1]	-		Reserved

Table 28. TX Interrupt enable

Address	Register name	R/W	Default	Description
0x0108	TX Interrupt enable[Byte 0]	RW	-	Bit 0:TX OVTP EN over temperature protection enable 0: disable 1: enable
		RW	-	Bit 1:TX OCP EN over current protection enable 0: disable 1: enable
		RW	-	Bit 2: TX OVP EN over voltage protection enable 0: disable 1: enable
		RW	-	Bit 3: TX SYS ERR EN system error enable 0: disable 1: enable
		RW	-	Bit4: TX RP PKT RCVD EN RP packet received interrupt enable

Address	Register name	R/W	Default	Description
0x0108	TX Interrupt enable[Byte 0]			0: disable 1: enable
		RW	-	Bit5:TX CE PKT RCVD EN CE packet received interrupt enable 0: disable 1: enable
		RW	-	Bit6:TX SEND PKT SUC EN Packet sent interrupt enable 0: disable 1: enable
		RW	-	Bit7: TX EXT MON EN Ext TX Detect interrupt enable 0: disable 1: enable
0x0109	TX Interrupt enable[Byte 1]	RW	-	Bit0:TX CEP TO EN CEP Timeout interrupt enable 0: disable 1: enable
		RW	-	Bit1:TX RPP TO EN RPP Timeout interrupt enable 0: disable 1: enable
		RW	-	Bit2: TX EPT EN AC powered down interrupt enable 0: disable 1: enable
		RW	-	Bit3:TX START PING EN Ping started interrupt enable 0: disable 1: enable
		RW	-	Bit4:TX SS PKT RCVD EN SS ID packet received interrupt enable 0: disable 1: enable
		RW	-	Bit5:TX ID PKT RCVD EN ID packet received interrupt enable 0: disable 1: enable
		RW	-	Bit6: TX CFG PKT RCVD EN Configuration packet received interrupt 0: disable 1: enable
		RW	-	Bit7:TX PP PKT RCVD EN PP packet received interrupt enable

Address	Register name	R/W	Default	Description
0x0109	TX Interrupt enable[Byte 1]			0: disable 1: enable
0x010A	TX Interrupt enable[Byte 2]	RW	-	Bit0:TX BRIDGE MD EN Bridge mode (half/full) changed interrupt. 0: disable 1: enable
		RW	-	Bit1:TX FOD DET EN TX FOD detect interrupt enable 0: disable 1: enable
		RW	-	Bit2: TX PTC UPDATE EN The power transfer contract is successfully updated after negotiation/renegotiation 0: disable 1: enable
		-	-	Bits [3..7] Reserved
0x010B	TX Interrupt enable[Byte 3]	-	-	Reserved

Table 29. TX Interrupt clear

Address	Register name	R/W	Default	Description
0x0104	TX Interrupt clear[Byte 0]	R	-	Bit 0: TX OVTP CLR over temperature protection clear 1: clear
		R	-	Bit 1:TX OCP CLR over current protection clear 1: clear
		R	-	Bit 2: TX OVP CLR over voltage protection clear 1: clear
		R	-	Bit 3:TX SYS ERR CLR system error clear 1: clear
		R	-	Bit4:TX RP PKT RCVD CLR RP packet received interrupt clear 1: clear
		R	-	Bit5:TX CE PKT RCVD CLR CE packet received interrupt clear 1: clear
		R	-	Bit6: TX SCLRD PKT SUC CLR Packet sent interrupt clear 1: clear
		R	-	Bit7: TX EXT MON CLR Ext TX Detect interrupt clear

Address	Register name	R/W	Default	Description
0x0104	TX Interrupt clear[Byte 0]			1: clear
0x0105	TX Interrupt clear[Byte 1]	R	-	Bit0:TX CEP TO CLR CEP Timeout interrupt clear 1: clear
		R	-	Bit1:TX RPP TO CLR RPP Timeout interrupt clear 1: clear
		R	-	Bit2:TX EPT CLR AC powered down interrupt clear 1: clear
		R	-	Bit3:TX START PING CLR Ping started interrupt clear 1: clear
		R	-	Bit4:TX SS PKT RCVD CLR SS ID packet received interrupt clear 1: clear
		R	-	Bit5: TX ID PKT RCVD CLR ID packet received interrupt clear 1: clear
		R	-	Bit6:TX CFG PKT RCVD CLR Configuration packet received interrupt clear 1: clear
		R	-	Bit7: TX PP PKT RCVD CLR PP packet received interrupt clear 1: clear
0x0106	TX Interrupt clear[Byte 2]	R	-	Bit0:TX BRIDGE MD CLR Bridge mode (half/full) changed interrupt clear 1: clear
		R	-	Bit1:TX FOD DET CLR TX FOD detect interrupt clear 1: clear
		R	-	Bit2: TX PTC UPDATE CLR The power transfer contract is successfully updated after negotiation/renegotiation clear 1: clear
		-	-	Bits [3..7] Reserved
0x0107	TX Interrupt clear[Byte 3]	-	-	Reserved

Table 30. TX interrupt latch

Address	Register name	R/W	Default	Description
0x0100	TX interrupt latch[Byte 0]	R	-	Bit 0:TX OVTP LTCH over temperature protection latch 1: latch

Address	Register name	R/W	Default	Description
0x0100	TX interrupt latch[Byte 0]	R	-	Bit 1: TX OCP LTCH over current protection latch 1: latch
		R	-	Bit 2:TX OVP LTCH over voltage protection latch 1: latch
		R	-	Bit 3:TX SYS ERR LTCH system error latch 1: latch
		R	-	Bit4:TX RP PKT RCVD LTCH RP packet received interrupt latch 1: latch
		R	-	Bit5:TX CE PKT RCVD LTCH CE packet received interrupt latch 1: latch
		R	-	Bit6:TX SLTCHD PKT SUC LTCH Packet sent interrupt latch 1: latch
		R	-	Bit7:TX EXT MON LTCH Ext TX Detect interrupt latch 1: latch
0x0101	TX interrupt latch[Byte 1]	R	-	Bit0:TX CEP TO LTCH CEP Timeout interrupt latch 1: latch
		R	-	Bit1: TX RPP TO LTCH RPP Timeout interrupt latch 1: latch
		R	-	Bit2:TX EPT LTCH AC powered down interrupt latch 1: latch
		R	--	Bit3:TX START PING LTCH Ping started interrupt latch 1: latch
		R	-	Bit4:TX SS PKT RCVD LTCH SS ID packet received interrupt latch 1: latch
		R	-	Bit5:TX ID PKT RCVD LTCH ID packet received interrupt latch 1: latch
		R	-	Bit6:TX CFG PKT RCVD LTCH Configuration packet received interrupt latch 1: latch
		R	-	Bit7: TX PP PKT RCVD LTCH

Address	Register name	R/W	Default	Description
0x0101	TX interrupt latch[Byte 1]			PP packet received interrupt latch 1: latch
0x0102	TX interrupt latch[Byte 2]	R	-	Bit0:TX BRIDGE MD LTCH Bridge mode (half/full) changed interrupt latch
		R	-	Bit1:TX FOD DET LTCH TX FOD detect interrupt latch
		R	-	Bit2: TX PTC UPDATE LTCH The power transfer contract is successfully updated after negotiation/renegotiation latch
		-	-	Bits [3..7] Reserved
0x0103	TX interrupt latch[Byte 3]	-	-	Reserved

Table 31. TX Interrupt status

Address	Register name	R/W	Default	Description
0x010C	TX Interrupt status[Byte 0]	R	-	Bit 0:TX OVTP STAT over temperature protection status
		R	-	Bit 1:TX OCP STAT over current protection status
		R	-	Bit 2: TX OVP STAT over voltage protection status
		R	-	Bit 3:TX SYS ERR STAT system error status
		R	-	Bit4:TX RP PKT RCVD STAT RP packet received interrupt status
		R	-	Bit5:TX CE PKT RCVD STAT CE packet received interrupt status
		R	-	Bit6: TX SEND PKT SUC STAT Packet sent interrupt status
		R	-	Bit7:TX EXT MON STAT Ext TX Detect interrupt status
0x010D	TX Interrupt status[Byte 1]	R	-	Bit0: TX CEP TO STAT CEP Timeout interrupt status
		R	-	Bit1:TX RPP TO STAT RPP Timeout interrupt status
		R	-	Bit2: TX EPT STAT AC powered down interrupt status
		R	-	Bit3:TX START PING STAT Ping started interrupt status
		R	-	Bit4:TX SS PKT RCVD STAT SS ID packet received interrupt status
		R	-	Bit5:TX ID PKT RCVD STAT

Address	Register name	R/W	Default	Description
0x010D	TX Interrupt status[Byte 1]			ID packet received interrupt status
		R	-	Bit6:TX CFG PKT RCVD STAT Configuration packet received interrupt status
		R	-	Bit7: TX PP PKT RCVD STAT PP packet received interrupt status
0x010E	TX Interrupt status[Byte 2]	R	-	Bit0:TX BRIDGE MD STAT Bridge mode (half/full) changed interrupt status
		R	-	Bit1:TX FOD DET STAT TX FOD detect interrupt status
		R	-	Bit2: TX PTC UPDATE STAT The power transfer contract is successfully updated after negotiation/renegotiation status
		-	-	Bits [3..7] Reserved
0x010F	TX Interrupt status[Byte 3]	-	-	Reserved

Table 32. TX configuration

Address	Register name	R/W	Default	Description
0x0112	TX FREQ MAX[Byte 0..1]	RW	-	Bits [7…0] Max frequency specified in units of 16Hz
0x0113				Bits [15…8] Max frequency specified in units of 16Hz
0x0114	TX FREQ MIN[Byte 0..1]	RW	-	Bits [7…0] Min frequency specified in units of 16Hz
0x0115				Bits [15…8] Min frequency specified in units of 16Hz
0x0116	TX FREQ PING[Byte 0..1]	RW	-	Bits [7…0] Ping frequency specified in units of 16Hz
0x0117				Bits [15…8] Ping frequency specified in units of 16Hz
0x0118	TX DC MAX	RW	-	Bits [7…0] Max TX duty cycle %. Max value is 50. Must be >= TX_MIN_DC
0x0119	TX DC MIN	RW	-	Bits [7…0] Min TX duty cycle %. Must be <= TX_MAX_DC
0x011A	TX DC PING	RW	-	Bits [7…0] Ping duty cycle in percentage
0x011B	TX PING INTERVAL	RW	-	Bits [7…0] Interval between ping (in 10ms)
0x011C	TX PING DURATION	RW	-	Bits [7…0] TX ping duration in ms.
0x0120	TX PLOSS FOD THR	RW	-	Bits [7…0]

Address	Register name	R/W	Default	Description
				TX PLOSS FOD detection threshold in 32mW units. 0 - Disable 1 - 32mW … 255 - 8160mW
0x0121	TX FOD DBNC CNT	RW	-	Bits [7…0] Continuous PLOSS based RP de bounce count before FOD EPT. 0 - EPT immediately
0x0122	TX CE TO MAX	RW	-	Bits [7…0] Max count TX retries with different frequency after failing to listen to CE packet within time frame
0x0123	TX RP TO MAX	RW	-	Bits [7…0] Max count TX retries after failing to listen to RP packet within time frame
0x0124	TX FHOP	RW	-	Bits [7…0] Define the step size (in Hz) for every frequency hop. Internally it is multiplied with 128 1: 128Hz step size 2: 256Hz step size 3: 384Hz step size ….
0x0125	TX PID MAX CURR	RW	-	Bits [7…0] TX max current for PID control target in units of 16mA. 0 - Unlimited 1 - 16mA …. 255 - 4080mA
0x012B	TX custom control	RW	-	Bits [1...0]:TX BRDG MODE TX power transfer half bridge / full bridge mode control. 0 - No change (same as ping) 1 - Manual half bridge mode 2 - Manual full bridge mode 3 - Auto switch
		RW	-	Bit 2:TX PING HALF BRDG TX ping in half bridge mode. 0 - Disable (Start ping in full bridge mode) 1 - Enable (Start ping in half bridge mode)
				Bits[3..7] Reserved
	TX configuration [Byte 0]	CFG	-	Bit 0:TX AUTO PING The device can start pinging automatically after starting to TX mode(enable) or it can wait for host I2C command(disable)
		CFG	-	Bit2:TX CE TO FHOP On CE timeout, frequency hop to try decoding ASK again.
	TX configuration [Byte 1]	CFG	-	Bit 1: FOD EPT Enables TX to terminate power transfer when FOD detected. TX will generate FOD interrupt. This bit controls whether EPT decision is automatic or by I2C master

Table 33. TX EPT reason

Address	Register name	R/W	Default	Description
0x0127	EPT reason [Byte 0]	RW	-	Bit 0: TX OVTP over temperature triggered
		RW	-	Bit 1: TX OCP over current protection triggered
		RW	-	Bit 2:TX OVP over voltage protection triggered
		RW	-	Bit 3:TX FOD

Address	Register name	R/W	Default	Description
0x0127	EPT reason [Byte 0]			Foreign object detected
		RW	-	Bit4: TX HOST Host issued EPT command
		RW	-	Bit5: TX RX EPT EPT Source Rx EPT packet
		RW	-	Bit6: TX CEP TO Control error packet timeout
		RW	-	Bit7: TX RPP TO Received power packet timeout
0x0128	EPT reason [Byte 1]	RW	-	Bit0: TX RX RST Rx send SS/ID/CFG at wrong time , probably because of RX RESET
		RW	-	Bit1: TX SYS ERR System error
			-	Bit2:TX SS TO Signal strength timeout
		RW	-	Bit3:TX SS ERR Signal strength packet error
		RW	-	Bit4:TX ID ERR Identification packet error
		RW	-	Bit 5: TX CFG Error in configuration packet
		RW	-	Bit 6: TX CFG CNT Number optional packets received doesn't match with number in configuration packet
		RW	-	Bit 7:TX PCH ERR Power control hold-off packet error
0x0129	EPT reason [Byte 2]	RW	-	Bit 0: TX XID ERR Extended identification packet error
		RW	-	Bit 1:TX NEG ERR Negotiation error
		RW	-	Bit 2: TX NEGO TO Negotiation Packet Time out
		-	-	Bits[3..7] Reserved

Table 34. TX power transfer contract

Address	Register name	R/W	Default	Description
0x0130	PTC [Byte 0]	R	-	Bit[3..0]:RX MINOR VER Power Transfer Contract Qi spec minor version number.
		R	-	Bits[4..5] Reserved
		R		Bit6:RX OB Qi Power transfer contract. Out-of-band communications functionality.

Address	Register name	R/W	Default	Description
0x0130	PTC [Byte 0]			1: supported 0: not supported
		R	-	RX AI Bit7 Qi Power transfer contract. Authentication functionality. 1: supported 0: not supported
0x0131	PTC [Byte 1]	R	-	Bit[7..0]: RX PCH Qi Power Transfer Contract. Power Control Hold-off Time (in ms)\in the range of 5 ms up to (and including) 205 ms.
0x0132	PTC [Byte 2]	R	-	Bit[7..0]:RX RPR HDR Qi Power Transfer Contract. Received Power Reporting Header.
0x0133	PTC [Byte 3]	R	-	Bit[7..0] :RX GUA POWER Qi 1.3 Reference Power Field. This value should be 2x of power in watt. Qi spec max is 63/2 watt.
0x0134	PTC [Byte 4]	R	-	RX WIN OFFSET Bit[2..0] Received Power window offset. Specified in units of 4ms. Keep default value (changing requires system level review).
		R	-	RX WIN SIZE Bit[7..3] Received Power window size. Specified in units of 4ms. Keep default value (changing requires system level review).
0x0135	PTC [Byte 5]	R	-	RX DUP Bit0 Qi Power transfer contract. Simultaneous incoming and outgoing data streams are supported (ONE) or not supported (ZERO).
		R	-	RX BUF SIZE Bit[3..1] Qi Power Transfer Contract. The size of the transport-layer buffer for receiving a data transport stream. The number of bytes in the buffer is equal to 16*2^n, with n the value contained in the Buffer Size field. Range 16 to 2048 bytes.
		R	-	RX MOD DEPTH Bit[5..4] Qi Power Transfer contract. FSK modulation depth. The value is 1/fmod - 1/fop in ns. Depends on configured fsk polarity. Stated as MINIMUM~MAXIMUM(for positive polarity)/MINIMUM~MAXIMUM(for negative polarity).
		R	-	RX POL Bit6 Qi Power transfer contract. The requested FSK polarity is positive (ZERO) or negative (ONE).
		R	-	RX NEG Bit7

Address	Register name	R/W	Default	Description
0x0135	PTC [Byte 5]			Qi Power transfer contract. The Extended Protocol is supported (ONE) or not supported (ZERO). If the Neg bit is set.
0x0136	PTC [Byte 6]	R	-	RX GUA PWR Bit[7..0] Qi 1.3 Guaranteed Power Field. This value should be 2x of power in watt. Qi spec max is 63/2 watt.
0x0137	PTC [Byte 7]	R	-	REPING Bit[7..0] Qi 1.3 Power Transfer Contract re-ping delay. In units of 200ms, Max is 12.6s.

Table 35. TX protections

Address	Register name	R/W	Default	Description
0x011D	TX OVP THRES	RW	-	Bit [7…0] Specify TX OVP threshold in 500mV units.
0x011E	TX OCP THRES	RW	-	Bit [7…0] Specify TX OCP current in 100mA units.0 - Disable1 - 100mA…
0x011F	TX OVTP THRES	RW	-	Bit [7 …0] Over temperature protection threshold in degree C. If transmitter die temperature rises above this value, then OTP triggered.
	TX Configuration [Byte 0]	CFG	-	Bit 4:TX ADC OVP EN PROT TX stops transmitting upon TX THRES OVP threshold reached. :
		CFG	-	Bit 5:TX ADC OCP EN PROT TX stops transmitting upon TX THRES OCP threshold reached.
		CFG	-	Bit 6:TX ADC OVTP EN PROT TX stops transmitting upon TX THRES OVTP threshold reached.

10 Application information

This chapter is aimed to provide some application hints. The reference schematic, the PCB layout guidelines, the minimum components to properly run the application and other aspects.

10.1 Reference application

STWLC38 typical application schematic for Rx and Tx modes are shown below.

Figure 13. STWLC38 basic application diagram in Rx mode

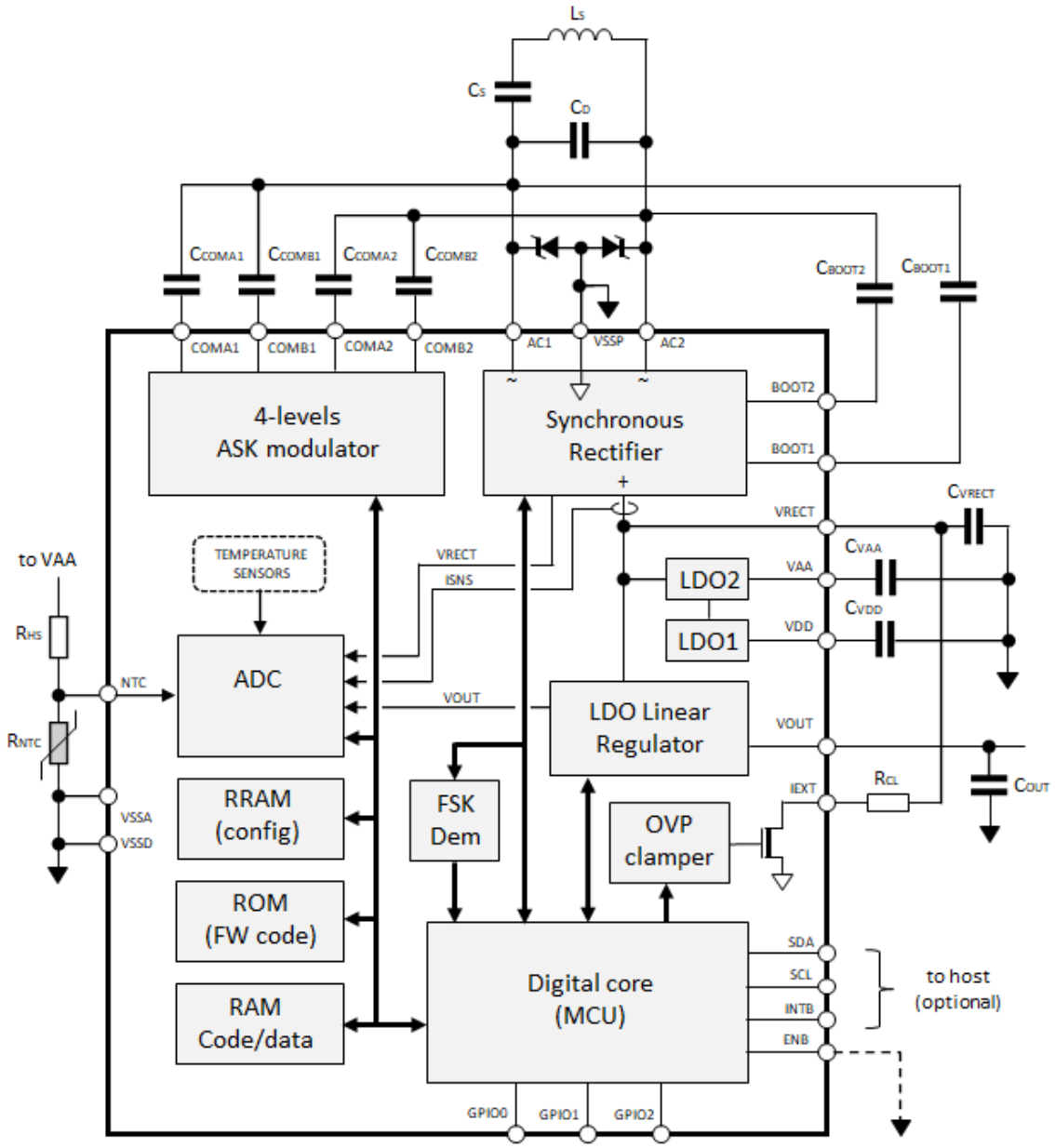
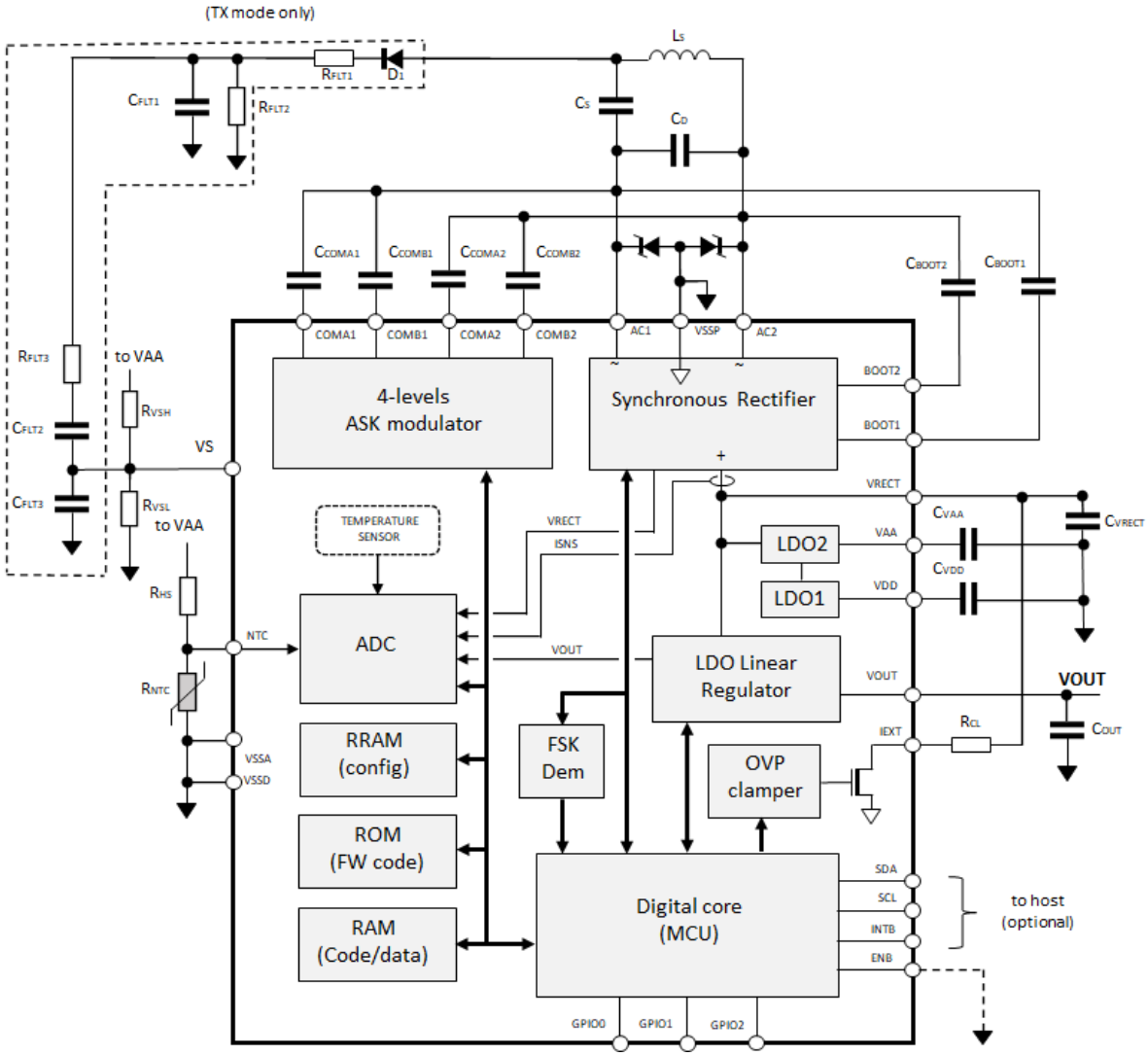


Figure 14. **STWLC38 basic application diagram in RTx mode**



10.2 Reference BOM

Typical key component values are listed in the tables below.

Table 36. **Typical components list for a 15 W RTx application**

Component	Value	Manufacturer	Part Number	Notes
LS	8µH	Luxshare	ICTR-QS5858029L-MW032	Receiving coil
CS	100nF/50V	Wurth	5x 885012206095	Series resonant capacitor
CD	3.3nF/50V	Wurth	885012206086	Parallel resonant capacitor
CBOOT1, CBOOT2	47nF/50V	Wurth	885012206093	Boot strap capacitor
COMB1,COMB 2	22nF/50V	Wurth	885012206091	ASK modulation capacitors
COMA1,COMA 2	10nF/50V	Wurth	885012206089	ASK modulation capacitors
CVAA	4.7uF/25V	Murata	GRM188R61E475KE11D	V5V0 filtering capacitor

Component	Value	Manufacturer	Part Number	Notes
CVDD	1µF/16V	Wurth	885012206052	V1V8 filtering capacitor
CRECT	10µF/25V	Murata	3x GRM188R61E106MA73D	VRECT filter capacitor, rating depending on application
COUT	10µF/25V	Murata	2x GRM188R61E106MA73D	OUT filter capacitor, rating depending on application
Z1,2	TVS	Littlefuse	SMF13A	TVS protection diodes
RCL	300R	Panasonic	2xERJ-P06F30R0V	clamping resistor
RHS,RNTC	10K,100K			Optional
RFLT1,2,3			6K8,220K,10K	ASK demod filter resistors
D1		Rohm	1N4448HLP	ASK demod circuit
CFLT1		Wurth	885012206086	ASK demod filter capacitors
CFLT2		Wurth	885012206091	
CFLT3		Wurth	885012206084	

Values for a 2.5W wireless power receiver application are listed in the table below.

Table 37. Typical components list for a Wearable and TWS Rx application

Component	Value	Manufacturer	Part Number	Notes
LS	13 µH	Luxshare		Receiving coil TWS
LS	11.8uH	Wurth	760308101219	Wearable
CS(TWS)	100nF/25V	Wurth	3 x 885012205085R(TWS) 2 x 885012205085R(WA)	Series resonant capacitor TWS and WA
CS(WA)	47nF/25V	Wurth	885012205054	Series resonanat caapcitor Wearable application
CD	1nF/25V	Wurth	885012205044	Parallel resonant capacitor
CBOOT1, CBOOT2	47nF/25V	Wurth	885012205054	Bootstrap capacitors
COMB1/ COMB2	10nF/25V	Wurth	885012205050	ASK modulation capacitors
COMA1/ COMA2	22nF/25V	Wurth	885012205052	ASK modulation capacitors
CVAA	4.7µF/6.3V	Wurth	885012105008	V2V5 filtering capacitor
CVDD	1µF/6.3V	Wurth	885012105006	V1V1 filtering capacitor
COUT	10µF/25V	Murata	2x GRM21BR61E106KA73L	VOUT filtering capacitors
CRECT	10µF/25V	Murata	2x GRM21BR61E106KA73L	filtering capacitors

Note: All of the components listed above refer to a typical application. Operation in the application may be limited by a choice of these external components (voltage ratings, current and power dissipation capability, etc.).

The basic application schematic is relatively simple, since STWLC38 does not require many external parts to operate. Anyway, there are different aspects that must be carefully considered to properly design a customized application. In most cases the main constrains are limited PCB size/room and thickness, that unavoidably lead to crowded solutions with a far-from-optimal electrical and thermal performance.

10.3 PCB routing guidelines

1. Auxiliary 2V5 (VAA) and 1V1 (VDD) LDO filtering capacitors should be placed as close as possible to the STWLC38. Connection traces should be short and placed in the top layer. Capacitors ground can be connected directly to the GND plane.
2. C_{RECT} and C_{OUT} capacitors should be placed close to STWLC38 with higher priority than R_{CL} resistor.
3. Power traces (AC1, AC2, VRECT, VOUT) should be kept wide enough to sustain high current. Duplicating these traces in inner layers is advisable wherever possible.
4. AC1 and AC2 tracks should be routed closely to minimize the area of the resulting loop.
5. Thermal performance and grounding should be always optimized by preserving bottom layer (usually assigned to ground) integrity.

10.4 External components selection

RX series resonant circuit components

Series resonant circuit, both Cs and Cd should show excellent quality factor, relatively high RMS current capability and superior capacitance stability in the frequency range of interest. Multi-Layer Ceramic capacitors (MLCCs) are inherently good devices in terms of RMS current capability and quality factor. Capacitance tolerance and stability strongly depend on the dielectric type.

Dielectrics such as X5R ,X7R,COG are used to achieve higher capacitance per volume at the cost of lower accuracy and undesired dependencies (e.g. DC-biasing, temperature, etc.). In practice, the C_S(most critical) usually consists of a few smaller, low-profile X5R/X7R/COG capacitors connected in parallel. The parallel connection also helps to increase RMS current capability and mitigate the effect of capacitance tolerance due to production spread. The voltage rating for these capacitors is usually maximized to take into account the voltage developed in proximity to resonance: 50V-rated capacitors are generally a good choice.

ASK modulation capacitors

The capacitors at the COMAx/COMBx pins are connected to the AC1-AC2 terminals through controlled switches (ASK modulator): the de-tuning effect of closing these switches results in an amplitude modulation detected by the transmitter and also visible at the rectified voltage. Positive or negative modulation may occur, depending on the operating frequency and other factors. The ASK modulation index clearly depends on the capacitance value of these capacitors, whose value has to be adjusted in case of a heavy negative modulation at VRECT (that is generally undesirable). The same considerations made above for the resonant capacitors is also applicable here, where capacitance tolerance is less critical: X5R dielectric-type are a good choice and an initial value of 22 nF and 10nF is typically doing the job.

VRECT over-voltage clamping resistor

The voltage at the VRECT pin is primarily dictated by the transmitter, whose operating point is linked to the feedback information received via ASK modulation. Unexpected conditions, however, may increase the VRECT voltage to dangerous values (close to AMR levels). A sudden change in relative alignment between the transmitting and receiving coils, for example, could result in a dramatic change in coupling factor and, in turn, a fast-rising voltage. Since the reaction of the transmitter is relatively slow, the STWLC38 protects itself by closing the switch internally connected to the IEXT pin. This switch is externally connected to VRECT via a resistor (R_{CL}) to implement an active clamper. The value of R_{CL} is selected so that most of the power is dissipated in the clamper circuit rather than inside of the chip. Special resistors (surge resistors) capable of withstanding higher energy pulses are recommended.

ESD protection diodes

Since the receiving coil is a easy entry point for ESD (relatively large area with remarkable capacitive coupling), a good application design should consider protections for the most exposed pins: AC1 and AC2. Uni-directional Transient Voltage Suppression (TVS) diodes at both pins are recommended. ESDs have essentially a common-mode nature and, although the receiving coil has low DC-resistance, its AC impedance may appear quite high to fast voltage spikes: independent clamping at AC1 and AC2 pins is thus mandatory. The knee-voltage of the TVS diodes should be selected considering the maximum VRECT voltage plus some margin to avoid non-negligible leakage current at higher temperature, while their energy dissipation capability should be maximized considering the size of the package.

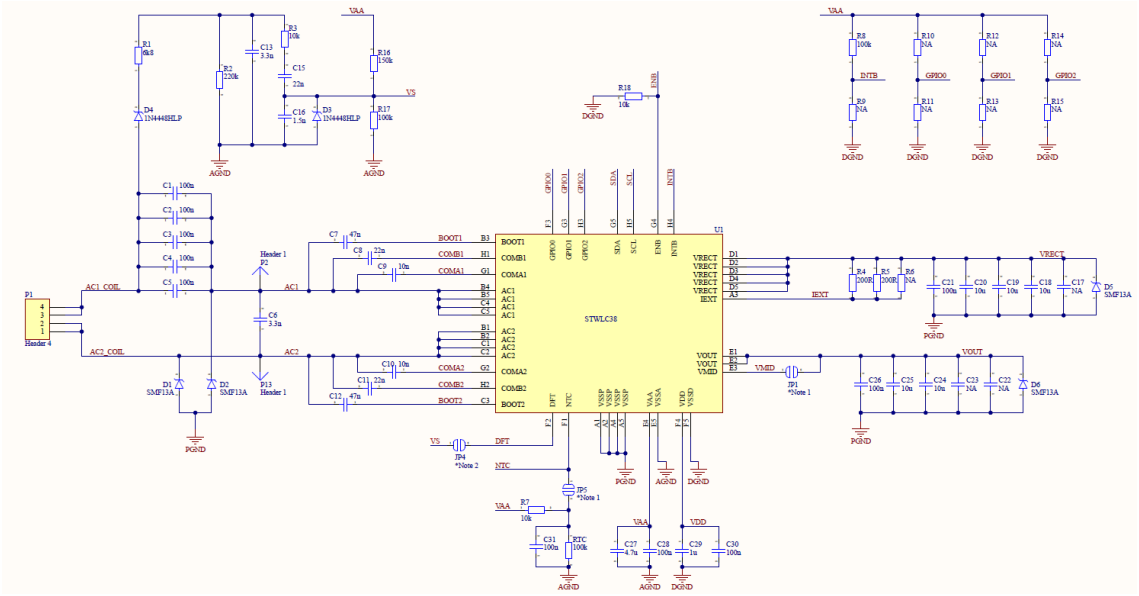
Coil thermal protection

Maximizing the amount of transferred power is ofter desirable, but also limited by operating conditions : applications in which the wireless power receiver has poor power dissipation capability and/or the power loss in the receiving coil is relevant (e.g. very tiny and slim coils with relatively high DC-resistance) may require some thermal protection. This feature is implemented with STWLC38 thanks to its NTC pin. A channel of the internal ADC is routed to the NTC pin, allowing the user to read the voltage across an external NTC thermistor.

11 Reference schematic

Figure 8. shows typical application schematic for the STWLC38.

Figure 15. STWLC38 basic schematic diagram



Note: All of the components listed above refer to a typical application. Operation in the application may be limited by a choice of these external components (voltage ratings, current and power dissipation capability, etc.)

12 Glossary/Abbreviations

- ADC: Auxiliary Data Control
- ADT : Auxiliary Data Transport
- ASK: Amplitude Shift Keying
- BPP : Baseline Power Profile
- CHS : Charge Status
- CEP: Control Error Packets
- CFG : Configuration
- DSR : Data Stream Response
- EPP: Extended Power Profile
- EPT: End Power Transfer
- FOD : Foreign Object Detection
- FSK: Frequency Shift Keying
- ID: Identification
- PCH: Power Control Hold-off
- PP: Proprietary Packet
- RP/RP8: Received Power Packet
- SRQ : Specific Request
- SS/SIG : Signal Strength Packet
- XID : Extended Identification

13 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

13.1 Package information

Figure 16. WLCSP40 2.126x3.327x0.546 0.4 Pitch 0.25 Ball package outline

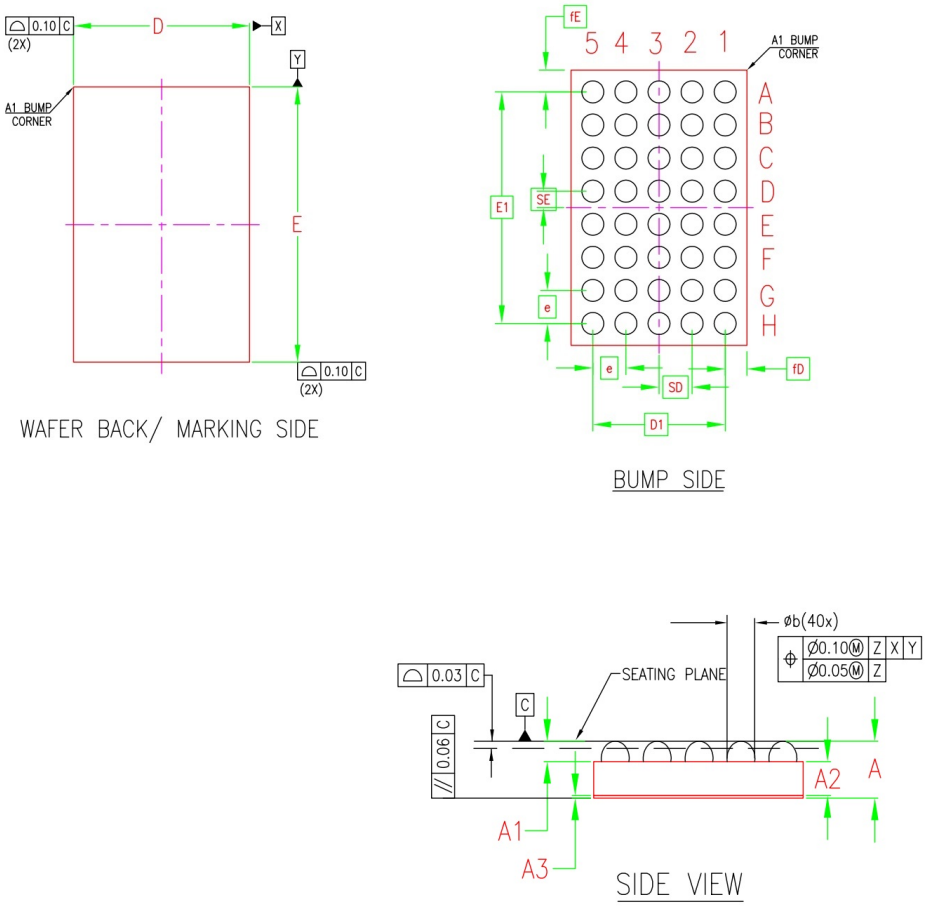


Table 38. **WLCSP40 2.126x3.327x0.546 0.4 Pitch 0.25 Ball mechanical data**

Ref	Data range (mm)		
	Min	Typ	Max
A	0.525	0.546	0.567
A1	0.181	0.196	0.211
A2	0.305	0.325	0.345
A3	0.022	0.025	0.028
b	0.243	0.268	0.293
D	2.106	2.126	2.146
D1		1.60	
E	3.307	3.327	3.347
E1		2.80	
e		0.400	
SE		0.200	
SD		0.400	
fD		0.263	
fE		0.263	
ccc		0.03	

Figure 17. **Recommended footprint**

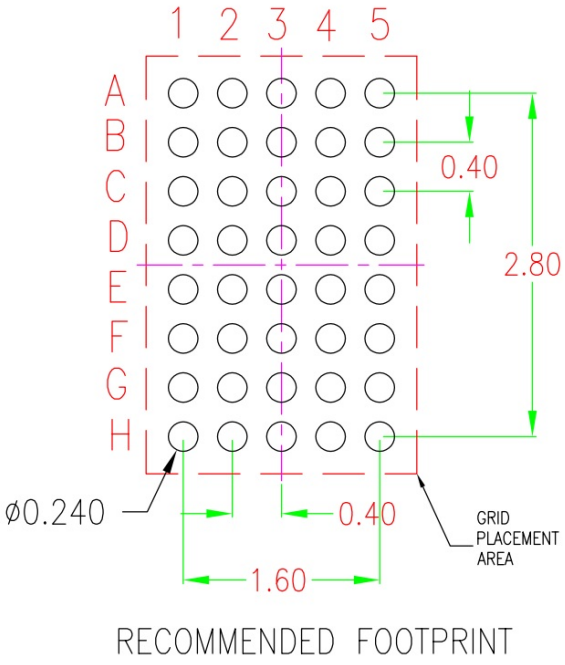
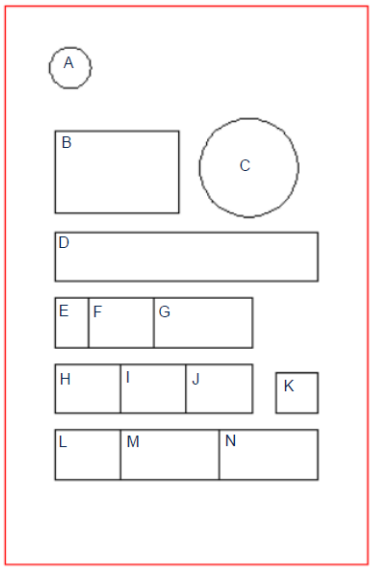


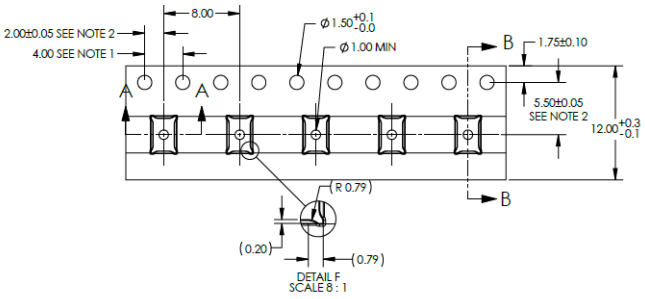
Figure 18. **Device marking , Tape and reel information**

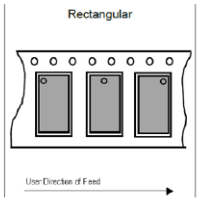


Device Marking Information

A – Stripe (PIN 1 Identifier)
B - Standard ST Logo
C - Second Level Interconnect
D – Marking Area – max 8 characters
E - Assembly Year (Y) - 1 character
F - Assembly Week (WW) - 2 characters

Tape and Reel information





Revision history

Table 39. **Document revision history**

Date	Version	Changes
20-Sep-2022	1	Initial release.

Contents

List of tables

List of figures

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