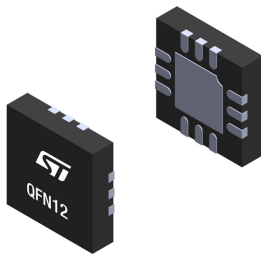


## USB-C overvoltage protection for VBUS and CC lines



Product link and summary	
Order code	TCPP01-M12
Package	QFN12
Packing	Tape and reel
Description	PPS compliant USB Type-C port protection

Companion chip	
USB Type-C	Any general purpose MCU (example: STM32 or STM8)
USB Type-C with power delivery	STM32 with UCPD support, example STM32L5, STM32G0, STM32G4
Evaluation board	X-Nucleo-USBPD1 with Nucleo-STM32G071RB or Nucleo-STM32G474RE
ST development board with TCPP01-M12	NUCLEO-L552ZE-Q, STM32L562E-DK, STM32L552E-EV
ST reference design	USB-C power adaptor STEVAL-USBPD27S

### Features

- VBUS overvoltage protection, adjustable from 5 V up to 22 V, with external N-channel MOSFET
- 6.0 V overvoltage protection (OVP) on CC lines against short-to-VBUS
- System-level ESD protection for USB Type-C connector pins (CC1, CC2), compliant with IEC 61000-4-2 level 4 ( $\pm 8$  kV contact discharge,  $\pm 15$  kV air discharge)
- Integrated gate driver and charge pump for an external N-channel MOSFET, (featuring lower  $R_{DS(ON)}$  than a P-channel MOSFET) for low BOM cost
- Null quiescent current when no USB charging cable is attached for battery-operated "consumer/sink" applications
- Integrated "dead battery" ( $R_D$  resistors)
- Over temperature protection (OTP)
- Operating junction temperature from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$
- Complies with the latest USB Type-C and USB power delivery standards
- Compliant with programmable power supply (PPS) for fast battery charging
- Open-drain fault reporting
- ECOPACK2 compliant
- USB-IF certification as power sinking device with TID: 3036 on X-Nucleo-USBPD1 and Nucleo-STM32G071RB

### Applications

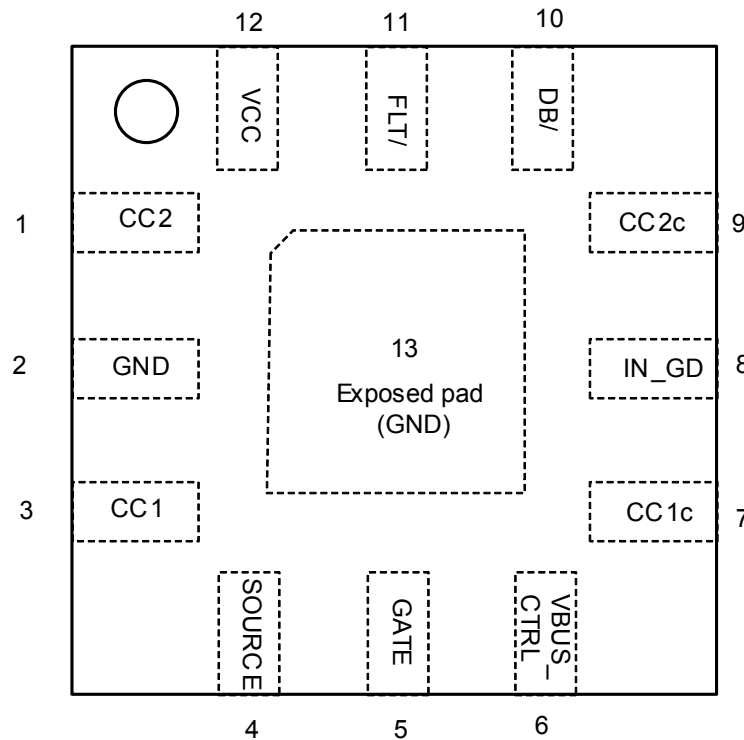
- Any USB Type-C device used in UFP/sink configuration using 5 V only or any PDO from USB power delivery, including PPS
- Power sinking devices: POS, gaming, healthcare, USB hub, IoT gateways
- Smart speakers, earphones, smart glasses, power tools, etc.

### Description

The TCPP01-M12 (Type-C port protection) is a single chip solution for USB Type-C port protection that facilitates the migration from USB legacy connectors type-A or type-B to USB Type-C connectors. The TCPP01-M12 features 22 V tolerant ESD protection as per IEC61000-4-2 level 4 on USB Type-C connector configuration channel (CC) pins. For a safe and reliable USB Type-C implementation, the TCPP01-M12 provides overvoltage protection on CC1 and CC2 pins when these pins are subjected to short circuit with the VBUS pin that may happen when removing the USB Type-C cable from its receptacle. For sink applications, TCPP01-M12 triggers an external N-MOSFET on VBUS line when a defective power source applies a voltage higher than selected OVP threshold. Also, the TCPP01-M12 integrates a "dead battery" management logic that is compliant with the latest USB power delivery specification. The power supply of the TCPP01-M12 for sink applications operated with a battery can be provided by an MCU 3.3 V GPIO in order to drop the power consumption in "cable not attached" condition down to 0 nA. This low power mode will extend the battery operating life when no source equipment is attached.

The TCPP01-M12 can also be used to protect source (provider) applications, and it can support programmable power supply feature from the USB-C power delivery specification.

# 1 Pinout and functions

**Figure 1. QFN12 pinout (top view)**

**Table 1. Pinout and functions**

Name	Pin #	Type	Description
CC2	1	Input / Output	USB-PD controller side for the CC2 pin (configuration channel)
GND	2	Ground	Ground
CC1	3	Input / Output	USB-PD controller side for the CC1 pin (configuration channel)
SOURCE	4	Power	VBUS N-channel MOSFET's SOURCE
GATE	5	Output	VBUS N-channel MOSFET's GATE
VBUS_CTRL	6	Input	Input voltage setting the VBUS OVP threshold by external resistor bridge
CC1c	7	Input / Output	Connector side for CC1 OVP internal FET
IN_GD	8	Power	VBUS N-channel MOSFET's DRAIN, input of the N-channel MOSFET gate driver
CC2c	9	Input / Output	Connector side for CC2 OVP internal FET
DB/	10	Input	Dead battery resistors management, connected to 3,3 V MCU GPIO
FLT/	11	Output	Fault reporting flag (open-drain), triggered by either OVP (overvoltage protection), OTP (overtemperature protection), or UVLO (undervoltage lockout) event.
V <sub>CC</sub>	12	Input	3.3 V power supply
Exposed pad	13	Ground	Ground



### 3 Characteristics

**Table 3. Absolute maximum ratings ( $T_{amb} = 25^{\circ}\text{C}$ )**

Symbol	Parameter	Pin name	Value		Unit
			Min.	Max.	
$V_{POWER}$	Voltage for Power pins	VCC	-0.3	4	$V_{DC}$
		IN_GD	-0.3	22	$V_{DC}$
$V_{IN}$	Voltage for Input pins	VBUS_CTRL, DB/, CC1, CC2	-0.3	4	$V_{DC}$
$V_{OUT}$	Voltage for Output pins	FLT/, SOURCE	-0.3	5.5	$V_{DC}$
		GATE	-0.3	27	$V_{DC}$
$V_{I/O}$	Voltage for CC1c, CC2c pins	CC1c, CC2c	-0.6	22	$V_{DC}$
$R_{thj-a}$	Junction-to-ambient thermal resistance			150	$^{\circ}\text{C}/\text{W}$
$T_J$	Junction temperature		-40	+125	$^{\circ}\text{C}$
$T_{STG}$	Storage temperature range		-55	+150	$^{\circ}\text{C}$

**Table 4. ESD ratings ( $T_{amb} = 25^{\circ}\text{C}$ )**

Symbol	Description	Pins	Value	Unit
$V_{ESD_c}$	System level ESD robustness on USB Type-C connector side	IN_GD, CC1c, CC2c, VBUS_CTRL <sup>(1)</sup>	15	kV
	IEC61000-4-2 Level 4, air discharge		8	
	IEC61000-4-2 Level 4, contact discharge			
$V_{HBM}$	$V_{ESD}$ ratings Human body model (JESD22-A114D, level 2)		2	kV

1.  $VBUS\_CTRL$  ESD capability is guaranteed by the external resistor  $R1_{min} = 3.8\text{ k}\Omega$

(see Figure 18. Sink applications, without battery, PPS compliant).

Note: for more information on IEC61000-4-2 standard testing, please refer to AN3353.

**Table 5. Electrical characteristics – Power supply and leakage current,  $T_{amb} = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$** 

Symbol	Parameter	Test condition	Value			Unit
			Min.	Typ.	Max.	
$V_{CC}$	Allowable voltage input range	-	3.0	3.3	3.6	V
$I_{VCC}$	$V_{cc}$ supply current	$V_{CC} = 3.0 - 3.6\text{ V}$			120	$\mu\text{A}$
VBUS	Allowable voltage range		3.3		22	V
$I_{L\_VBUS}$	VBUS Supply current at $VBUS = 22\text{ V}$				2	$\text{mA}$

**Table 6. Electrical characteristics – VBUS OVP control, T<sub>OP</sub> = -40 °C to +85 °C**

Symbol	Parameter	Test condition	Value			Unit
			Min.	Typ.	Max.	
V <sub>GS</sub>	GATE to SOURCE voltage	V <sub>CC</sub> = 3.0 - 3.6 V, VBUSc <sup>(1)</sup> = 4.0 V	5.0	5.5	6.0	V
		V <sub>CC</sub> = 3.0 - 3.6 V, VBUSc <sup>(1)</sup> = 3.3 V	4.0		5.0	
t <sub>ON_VBUS</sub>	Turn-on time on VBUS pin	V <sub>CC</sub> = 3.0 - 3.6 V		1		ms
V <sub>ovp_th</sub>	OVP VBUS threshold voltage	V <sub>CC</sub> = 3.0 - 3.6 V	1.20	1.25	1.34	V
V <sub>hyst</sub>	OVP VBUS voltage hysteresis	V <sub>CC</sub> = 3.0 - 3.6 V		0.13		V
t <sub>ovp_VBUS</sub>	OVP VBUS response time	Gate capacitance = 470 pF, V <sub>CC</sub> = 3.0 - 3.6 V			100	ns

1. VBUSc is the VBUS voltage as seen from USB-C connector between VBUS and GND.

**Table 7. Electrical characteristics – DB/ pin and CC lines OVP, T<sub>OP</sub> = -40 °C to +85 °C**

Symbol	Parameter	Test condition	Value			Unit
			Min.	Typ.	Max.	
R <sub>ON</sub>	ON resistance of CC OVP FET	V <sub>CC</sub> = 3.0 - 3.6 V			1.2	Ω
R <sub>ON_FLAT</sub>	ON resistance flatness	0 - 1.2 V		5.0		mΩ
C <sub>ON_CC</sub>	Equivalent ON capacitance	0 - 1.2 V, f = 400 kHz	40		100	pF
V <sub>CL_DB</sub>	Dead battery clamp voltage	I = 200 μA			1.5	V
V <sub>TH_CC</sub>	CC OVP threshold voltage	V <sub>CC</sub> = 3.0 - 3.6 V	5.6	6.0	6.4	V
V <sub>OVP_CC_H</sub>	CC OVP hysteresis	V <sub>CC</sub> = 3.0 - 3.6 V		10		mV
t <sub>ovp_cc</sub>	OVP response time on the CC pins (internal FET) (see Figure 12)	V <sub>CC</sub> = 3.0 - 3.6 V			70	ns
BW_CCx	Bandwidth on CCx pins at -3dB	0 - 1.2 V	10			MHz
R <sub>DB_off</sub>	Equivalent resistor when dead battery is OFF	V <sub>CC</sub> = 3.0 - 3.6 V	170	300	460	kΩ

**Table 8. Electrical characteristics – Fault reporting, T<sub>OP</sub> = -40 °C to +85 °C**

Symbol	Parameter	Test condition	Value			Unit
			Min.	Typ.	Max.	
t <sub>pd</sub>	Propagation time from OVP, OTP or UVLO to FLT/	V <sub>CC</sub> = 3.0 - 3.6 V	-	5	-	μs
R <sub>ON</sub>	FLT/ pin resistance when active		-	250	-	Ω
R <sub>OFF</sub>	FLT/ pin resistance when inactive		-	1	-	MΩ

## 4 Typical electrical characteristics curves

Note:  $T_{op} = 30\text{ }^{\circ}\text{C}$ ,  $V_{CC} = 3.3\text{ V}$ , SOURCE = 5 V, SINK configuration, unless otherwise stated.

Figure 4. CC line bandwidth:  $V_{cm} = 0\text{ V}$

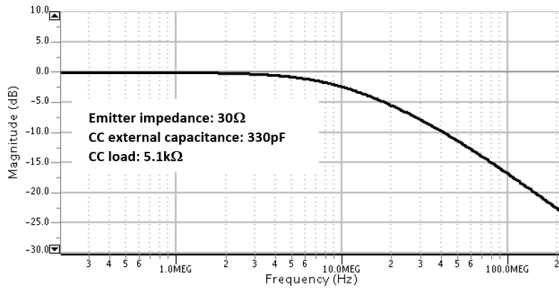


Figure 5. CC line bandwidth:  $V_{cm} = 1.2\text{ V}$

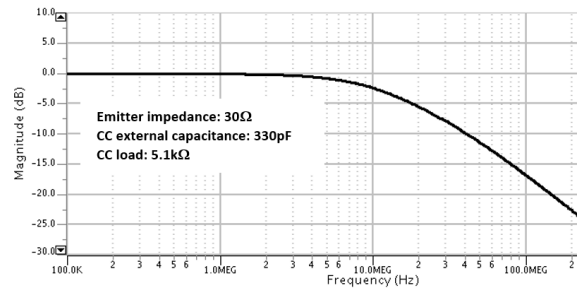


Figure 6. CCx digital communication (eye diagram performed on X-NUCLEO-USBPDM1 and NUCLEO-G071RB)

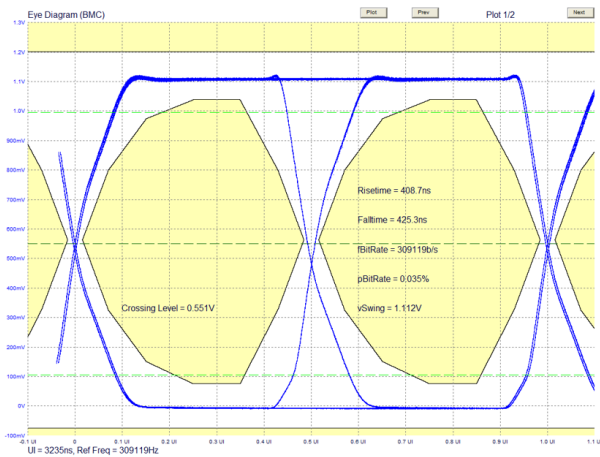


Figure 7. CC1c line short to VBUS (22 V) hot-plug via 1m of USB-C cable, sink configuration

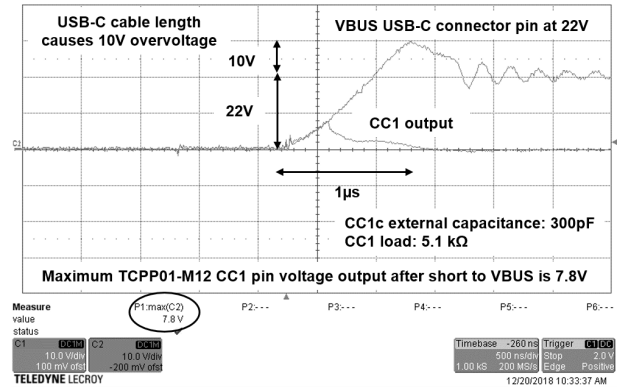


Figure 8. CC line leakage current vs ambient temperature at 5.5 V

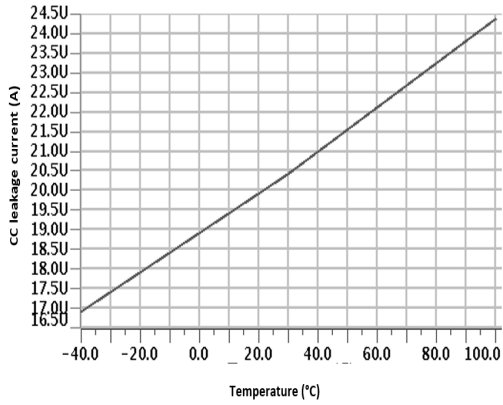


Figure 9. ON resistance of CC OVP FET vs ambient temperature

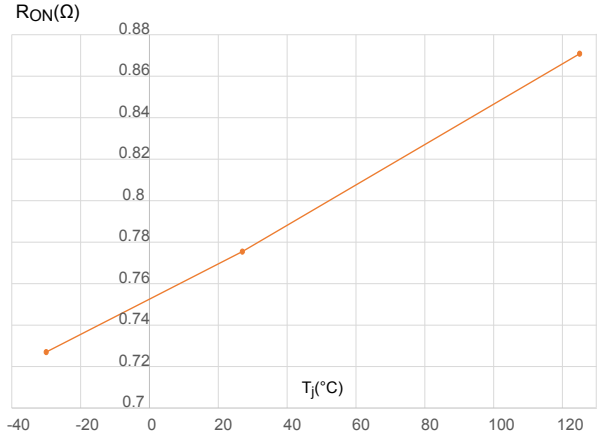


Figure 10. CC line attachment with 20 V source

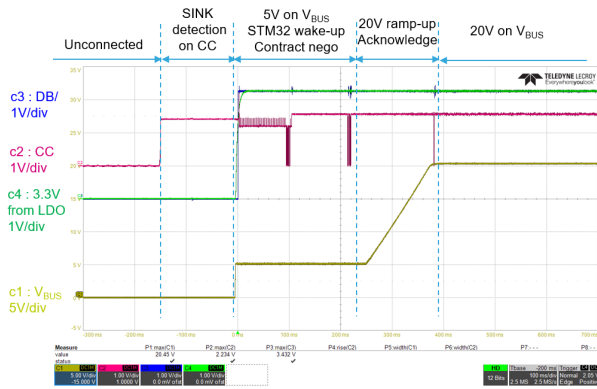


Figure 11. TCPP01-M12 start-up sequence

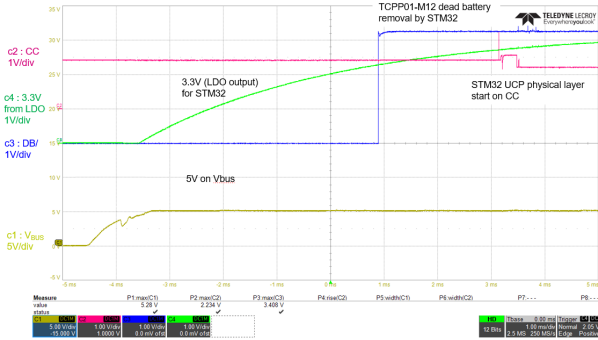


Figure 12. VBUS short to CC line

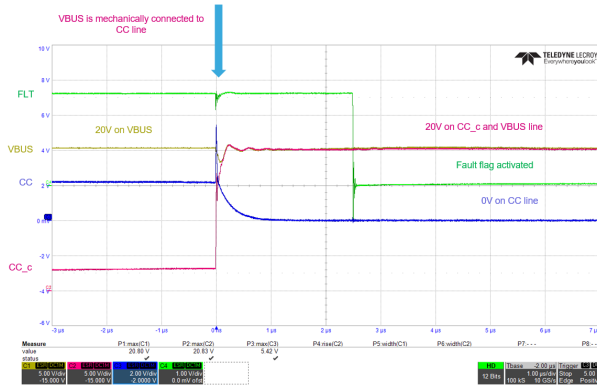


Figure 13. IEC61000-4-2 +8 kV ESD applied on CC1c, response on CC1 pin

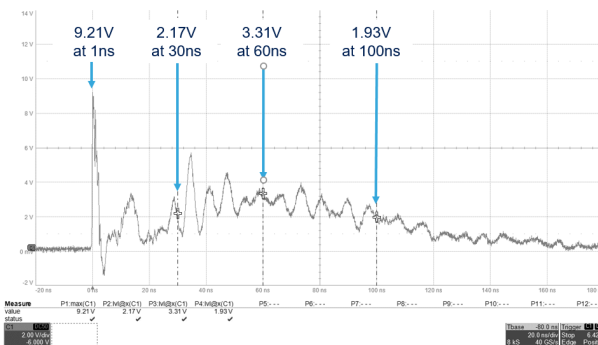


Figure 14. CCx line TLP curve (unpowered)

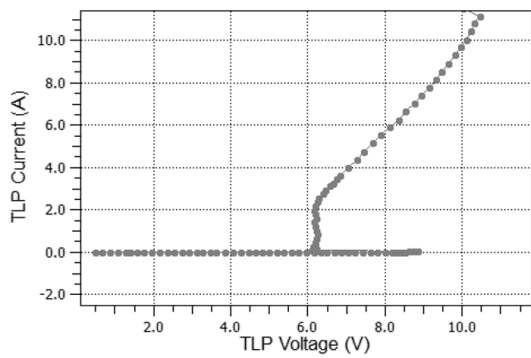


Figure 15. VBUS power-on at 5 V for a sink device

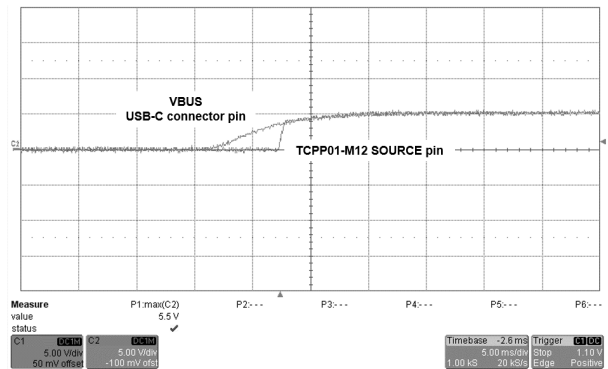
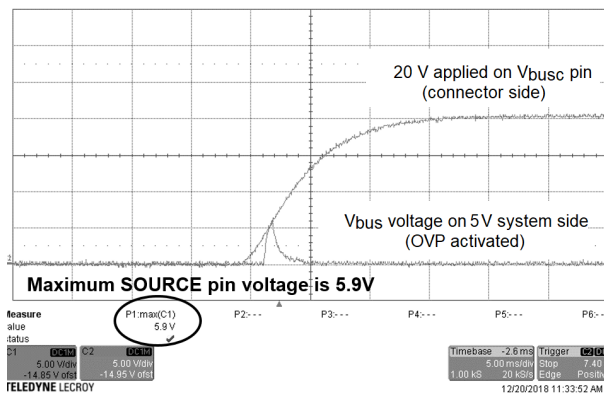


Figure 16. VBUS 5 V overvoltage protection (sink configuration, 20 V applied on VBUS)





## 5 TCPP01-M12 low power mode

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### 5.1 What is TCPP01-M12 low power mode ?

TCPP01-M12 low power mode operation allows TCPP01-M12 to feature 0  $\mu$ A power consumption. This mode applies only for sink applications using the USB-C power delivery protocol.

### 5.2 How to activate TCPP01-M12 low power mode?

To activate low power mode operation, TCPP01-M12 pins  $V_{CC}$  and DB/ must be in OFF state: in this state, TCPP01-M12 presents its dead battery resistors ( $R_D$ ) on CC1 and CC2 lines.

### 5.3 When to activate TCPP01-M12 low power mode?

Low power mode activation may be done when no USB-C cable is attached. We recommend to activate TCPP01-M12 only when contract negotiation is required.

## 6 Application

### 6.1 General information

The sections below are not part of the ST product specification. They are intended to give a generic application overview to be used by the customer as a starting point for further implementations and customizations.

ST does not warrant compliance with customer specifications. Full system implementation and validation are under the customer's responsibility.

The TCPP01-M12 protects USB Type-C™ ports against over-voltage on VBUS and CC lines as well as electrostatic discharges on the connector pins, among other things. TCPP stands for Type-C port protection, and the TCPP01-M12 is unique because it works as a companion chip for our STM32 MCUs with built-in USB-C power delivery (UCPD) controllers on sink configurations. Moreover, using an STM32G0, STM32G4, or an STM32L5, and the TCPP01-M12 is significantly more cost-effective than competing solutions. The TCPP01-M12 also distinguishes itself thanks to a null quiescent current when unplugged and using the device in a sink configuration.

Engineers can separate the low voltage MCU domain and high voltage power path and benefit from all the protections needed. Additionally, the QFN12 package of the TCPP01-M12 can sit really close to the USB Type-C connector itself to maximize protection. Similarly, the fact that the device is compliant with programmable power supplies means that the sink device starts at 3.3 V and increases its request voltage by 20 mV increments until it matches the characteristics of the battery, thus offering quick charging capabilities while safeguarding the system. The TCPP01-M12 also improves the overall efficiency, compared to competing solutions, by offering a low  $R_{DSon}$  and a null quiescent current. The last feature is possible because the device receives power from the GPIO pin of the MCU rather than an internal low-dropout regulator. As a result, when the user unplugs a cable, the TCPP01-M12 doesn't consume any energy at all. This is particularly crucial for companies looking to create tiny products with particularly small batteries, and that must thus limit the system's consumption as much as possible. Many engineers may underestimate it, but when a product is as little as a pen, every microamp counts.

### 6.2 Electrical hazards related to USB Type-C

Applications using an USB Type-C connector must be protected against three kinds of hazards:

#### 6.2.1 CC lines short to VBUS

This happens when VBUS high voltage short circuit to the CC lines when hot unplug is done with a poor mechanical quality connector. Over voltage protection is needed on the CC lines because VBUS typical voltage can be as high as 20 V when CC pins are usually 5 V tolerant I/Os on low voltage USB-PHY controllers. TCPP01-M12 integrate this protection against CC lines short to VBUS thanks to an overvoltage protection (integrated FET).

#### 6.2.2 Defective charger

Until now, it was common to find the protection circuit inside a controller dedicated to USB-C power delivery. However, by supporting USB-C PD with an embedded module inside an MCU and a companion Type-C port protection device, we can lower the bill of material and facilitate the transition from micro-B devices, without requiring an expensive USB-C PD ASIC controller. One of the reasons the MCU and TCPP01-M12 bundle is such a compelling financial proposition is that the latter device integrates the VBUS gate driver, which enables the use of more affordable N-MOSFET, instead of the more expensive P-MOSFET.

This is an added value of TCPP01-M12, specially when VBUS line is compromised if a defective charger is stuck at a high voltage.

Overvoltage protection is always required on the VBUS line to prevent a voltage higher than negotiated is applied on the VBUS.

This use case can occur even when power delivery is not used i.e when VBUS voltage is 5 V.

#### 6.2.3 Electrostatic discharge (ESD)

Electrostatic discharges can be conducted by the USB Type-C connector and damage the electronic circuitry of the application.

The ESD surge waveform is modeled by the international electrotechnical commission in the specification IEC61000-4-2.

For more information on IEC61000-4-2 standard testing, please refer to STMicroelectronics application note [AN3353](#).

### 6.3 USB Type-C protection

Any application using an USB Type-C connector must use a Type-C port protection against above listed electrical hazards.

STMicroelectronics TCPP01-M12 (Type-C port protection housed in QFN12) is a single-chip cost effective solution to protect any application using a USB Type-C connector.

It is especially adapted to SINK (consumer) or SOURCE (provider) applications (see [Section 6.7 Typical USB-C source application](#) for specific usage in source applications).

The TCPP01-M12 provides 20 V short-to-VBUS over-voltage and system-level ESD protection on CC lines, as well as adjustable over-voltage protection for the VBUS line: an external N-channel MOSFET gate driver is integrated inside TCPP01-M12.

Also, TCPP01-M12 integrates dead battery management logic.

For consumer (sink) configurations, TCPP01-M12 features a null quiescent current thanks to TCPP01-M12 VCC pin being directly controlled by a MCU GPIO in this configuration.

TCPP01-M12 is the companion chip for:

- any general purpose MCUs (example: STM32, STM8) used for USB-C charging applications exposed to defective charger and electrostatic discharge.
- any low voltage USB power delivery controller (for example: STM32-UCPD like STM32G0, STM32G4 and STM32L5), exposed to short to VBUS, defective charger and electrostatic discharge.

## 6.4 How to handle dead battery (DB) condition with the TCPP01-M12

Dead battery use case happens when a battery-operated sink (consumer or UFP) application has its battery fully depleted. In this case TCPP01-M12 enters into dead battery operation.

Dead battery behavior is basically a pull down ( $R_D$ ) or a voltage clamp when a USB Type-C source voltage is applied to CC. It is interpreted as a request by the sink to receive VBUS. It thus facilitates the charging of equipment with a fully depleted battery:

- It must be present in most cases
- It must not be present in the case of a (pure) Type-C Source, for example a wall charger

The DB/ or 'dead battery resistor management' pin is a pulled-down active-low TCPP01-M12 input. The DB/ pin can be used in two ways:

- The DB/ pin is connected to VCC or
- The DB/ pin is driven by a 3,3 V MCU GPIO

As long as the DB/ pin is low or high-impedance (an internal 5 k $\Omega$  pull-down sets the level to '0'), the dead-battery resistors are connected and CC switches are open (OFF state).

When the DB/ pin is tied to VCC, the DB/ resistors are disconnected and CC OVP switches are closed (ON state).

DB/ usage in SINK (SNK) applications:

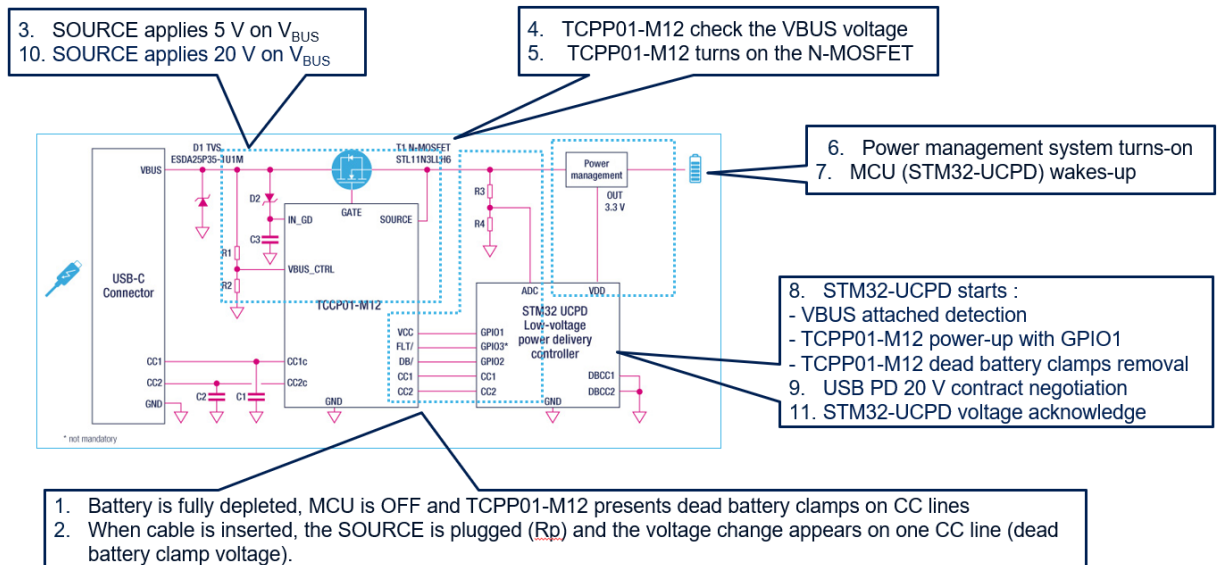
- After system power-up, the DB/ pin must be kept at 0. In this case  $R_D$  is enabled at TCPP01-M12 level.
- Once  $R_D$  is enabled in the UCPD (USB-C power delivery controller), the DB/ pin must be set to the logic level '1'

For DB/ usage in SRC or Source mode, the DB/ pin must be tied to  $V_{CC}$ .

**Table 9. Dead battery logic states**

TCPP01-M12 VCC	TCPP01-M12 DB/	TCPP01-M12 DB clamp present	TCPP01-M12 CC1/CC2 OVP FET state	TCPP01-M12 DB function state
0	0	Yes	Open	Activated
0	1	Yes	Open	Activated
1	0	Yes	Open	Activated
1	1	No	Closed	Inactivated

*Note:* When STM32-UCPD boots,  $R_D$  seen on CC lines are coming from TCPP01-M12. When STM32-UCPD has wake-up,  $R_D$  from TCPP01-M12 are disconnected and STM32-UCPD set  $R_D$  on CC lines from UCPD IP

**Figure 17. Wake-up sequence in dead battery condition**

**Note:**

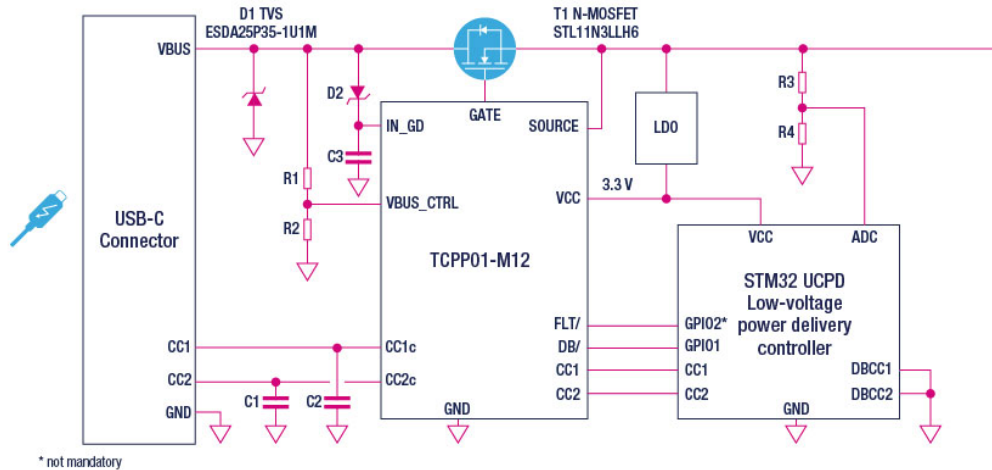
In dead battery condition the sequence below applies:

- TCPP01-M12 dead battery present clamp (1.1 V) on CC1 and CC2 lines
- The source detects the clamp presence and applies 5 V on V<sub>BUS</sub>
- The N-channel MOSFET (T1: STL11N3LLH6) switches to ON state and supplies the application's power management with 5 V
- The MCU wakes-up and applies 3.3 V on GPIO1: this wakes up the TCPP01-M12
- The TCPP01-M12 removes its clamp on the CC lines so that ADC1 or ADC2 can sense the SOURCE power capability with the voltage across R5 or R6 (both resistors are needed)

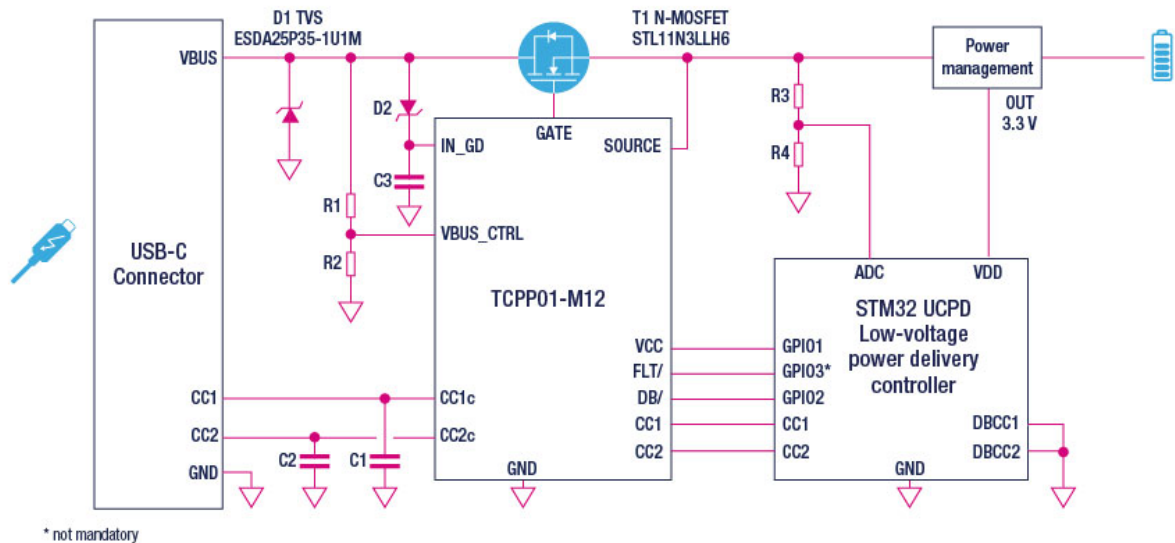
## 6.5 Application example for USB Type-C power delivery for sink (consumer), PPS compliant

In this application case, the system is solely powered via the USB-C connector.

**Figure 18. Sink applications, without battery, PPS compliant**



**Figure 19. Power sinking device PD3.0 application, with battery**



### 6.5.1 ESD capacitor (C3)

The system-level ESD capability of the TCPP01-M12 depends on this capacitor. The two constraints about it is a minimum of 35 V DC rated voltage and an ESL (equivalent serial inductance) as low as possible.

A 50 V X7R 100 nF capacitor is strongly recommended to improve the derating performance (X7R capacitance decreases as it voltage increases). ST recommends to choose a capacitor size equal or lower than 0603.

**Table 10. Capacitance specification**

Capacitor size	Part number
0603	CC0402KRX7R9BB104
0402	GRM188R71H104KA93D

### 6.5.2 Transient Voltage suppressor on VBUS

In the [Figure 18](#), the D1 diode ESDA25P35-1U1M is used to comply with the international electrotechnical commission specification IEC61000-4-5 on the VBUS power line when it is subjected to switching and lightning transients. These surges are defined in 8/20 μs waveform. For more information, please refer to [AN4275](#): IEC61000-4-5 standard overview.

### 6.5.3 CC line capacitance (C1, C2)

USB PD has a specification for the total amount of capacitance for proper operation on CC lines. This specification is given here after.

**Table 11. USB Type-C power delivery specification**

Description	Min.	Max.
CC receiver capacitance	200 pF	600 pF

Therefore, the capacitance added by the TCPP01-M12 and by the MCU or low voltage controller must fall within these limits. The next table shows the analysis involved in choosing the correct external capacitor for the system.

**Table 12. CC line capacitance budget analysis**

CC capacitance	Min.	Max.	Comment
CC line target capacitor	200 pF	600 pF	From USB PD Specification Section 5.8.6
TCPP01-M12 CC1c, CC2c capacitance	40 pF	100 pF	
MCU capacitance	60 pF	90 pF	Typical value. To be adapted following the exact reference used
Proposed capacitance C1, C2	120 pF	390 pF	25 V DC min. of rated voltage 0402 or smaller recommended

### 6.5.4 Sense resistor (R1, R2)

VBUS OVP triggers when VBUS\_CTRL pin rises above 1.25 V typical. Choose R1 from any value between 5 kΩ and 10 kΩ and calculate R2 as follows:

$$R2 = \frac{R1}{\frac{VBUScMAX}{VBUS\_CTRL} - 1}$$

With:

- R1 = arbitrary resistor between 5-10 kΩ
- VBUScMAX = desired VBUS OVP threshold level
- VBUS\_CTRL = 1.25 V (typical)

**Table 13. R2 values when R1 = 10 kΩ**

Power Delivery	VBUS maximum voltage	R2 normalized value in ohm (Ω) when R1 = 10 kΩ
15 W	6 V	2.7 k
27 W	10 V	1.5 k
36 W	13 V	1.1 k
45 W	17 V	820
100 W	22 V	620

### 6.5.5 VBUS detect

R3 and R4 are used to sense the VBUS voltage. Recommended values are R3 = 200 kΩ and R4 = 40.2 kΩ.

As per USB-C PD specification, if the VBUS voltage is lower than 3.0 V, FLT/ pin will go to low state.

### 6.5.6 N-channel MOSFET

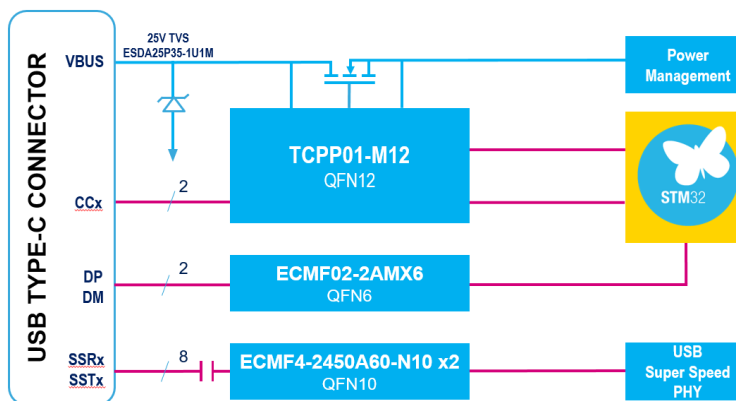
The TCPP01-M12 ensures a  $V_{GS}$  voltage between 5 V and 6 V when the N-channel MOSFET is ON: choose a N-channel MOSFET fully specified (for example: STL11N3LLH6) with 5 V of  $V_{GS}$ . Maximum current in USB-PD applications can raises up to 5 A.

MCU can still close the MOSFET with a MCU GPIO connected to VBUS\_CTRL: in this case, normal mode (i.e TCPP01 overvoltage protection active on VBUS) is ensured with GPIO in HighZ. To close the MOSFET, MCU GPIO must be set at '1'.



**6.5.7 Complementary products for USB dataline protection for pins DP, DM, SSRX, SSTX**

For applications requiring USB dataline protection, STMicroelectronics recommends the implementation shown in picture below:

**Figure 20. USB dataline ESD protection for pins DP, DM, SSRX, SSTX**

**Table 14. Product recommendations**

Part Number	Description	USB-C connector pin	Protection features
TCPP01-M12	Type-C port protection	VBUS, CC1, CC2	ESD protection as per IEC61000-4-2 Level 4 Overvoltage on VBUS CC lines short to VBUS
ESDA25P35-1U1M	Power line transient voltage suppressor (TVS)	VBUS	ESD protection as per IEC61000-4-2 Level 4 IEC61000-4-5 (8/20µs surge waveform)
ECMF02-2AMX6	Common mode filter with integrated ESD protection	D+, D-	ESD protection as per IEC61000-4-2 Level 4 RF antenna desense due to high speed differential link EMI radiation
ECMF4-2450A60N10 (x2)	Common mode filter with integrated ESD protection	TX1+, TX1-, RX1+, RX1- TX2+, TX2-, RX2+, RX2-	ESD protection as per IEC61000-4-2 Level 4 RF antenna desense due to high speed differential link EMI radiation

For more information on USB Type-C protection for datalines, please refer to [AN4871](#), USB Type-C protection and filtering.

For more information on RF antenna desense due to high speed differential link EMI radiation, please refer to [AN4356](#), Antenna desense on handheld equipment.

## 6.6 Typical USB-C battery powered application

### 6.6.1 Power sinking device using PD3.0

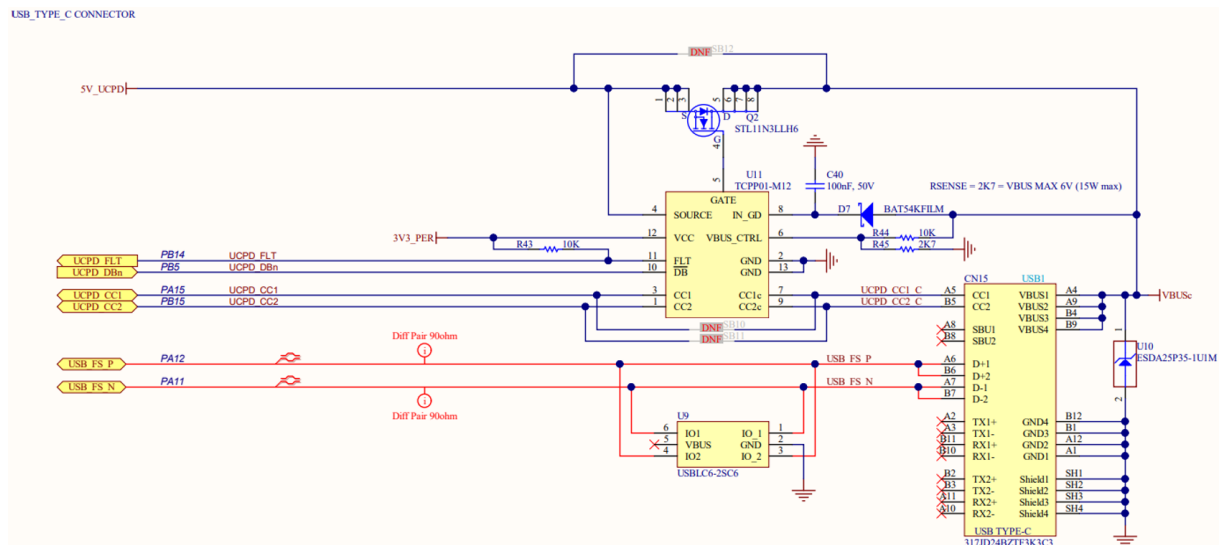
Thanks to its simple implementation and system compliancy with both legacy USB charging (using 5 V only) and latest USB power delivery specification, USB-C applications using the TCPP01-M12 can simply migrate from legacy USB charging (see [Figure 22](#)) to USB power delivery charging (see [Figure 19](#)) by simply swapping their STM32 from general purpose (for example: STM32L0) to general purpose + UCPD (example: STM23G0) and remove C1/C2 and add R5/R6 in the PCB to take benefit of the USB-C power delivery. Empty PCB footprints can be planned earlier in the design to allow this hardware system scalability.

In this application use case, the system is typically powered by embedded batteries and the USB-C connector is used to recharge them.

Compared to the previous case (cf [Figure 18. Sink applications, without battery, PPS compliant](#)), the TCPP01-M12 is now powered via GPIO1: This is possible thanks to the very low TCPP01-M12 biasing current (120  $\mu$ A worst case). In this configuration, the TCPP01-M12 consumes power only during USB attachment. An attachment condition is detected via resistors R3 and R4.

Once a source has detected a SINK attachment, it releases automatically 5 V / 0.5 A on the VBUS. This voltage is detected by the TCPP01-M12 and it turns on the N-channel MOSFET T1 (needed power is drawn from IN\_GD pin). As the VBUS voltage increases, the attachment is detected through ADC.

**Figure 21. Schematic example (extracted from NUCLEO-L552ZE-Q, STM32 Nucleo-144 development board with STM32L552ZE MCU, SMPS, supports Arduino, ST Zio and morpho connectivity)**

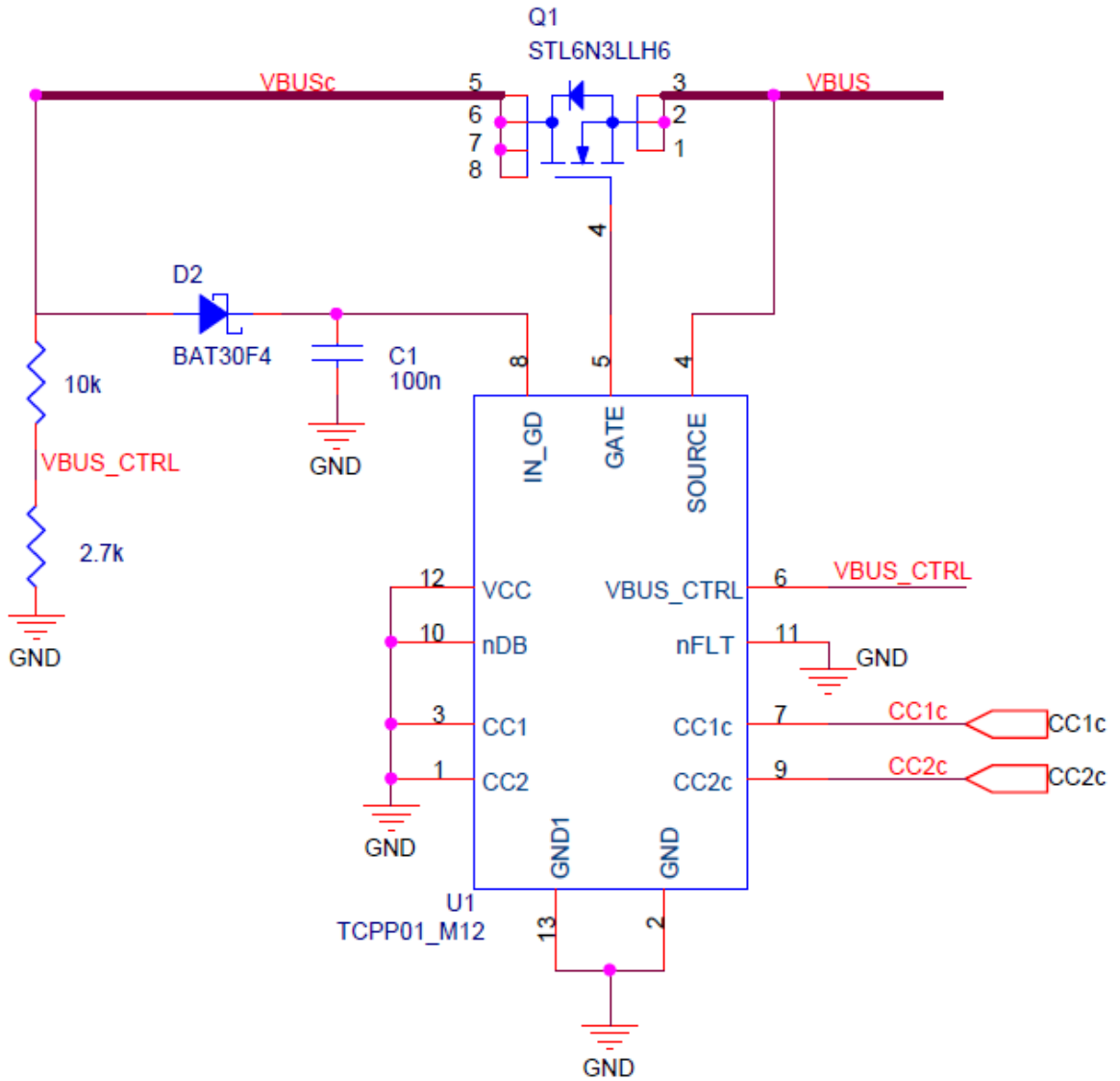


Please refer to [AN5225](#) for more informations related to USB Type-C power delivery using STM32xx Series MCUs and STM32xxx series MPUs.

For more information on EMI filtering and ESD protection of USB datalines, please refer to [AN4871: USB Type-C protection and filtering](#).



Figure 23. Schematic example for USB-C at 2.5 W with TCPP01-M12

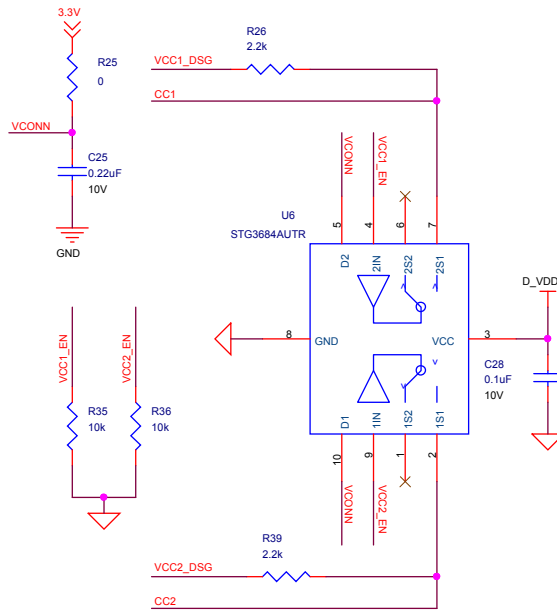


At 2.5 W, USB Type-C is used at 5 V, 0.5 A. Therefore capacitors on CC lines are not needed anymore (they are needed only for power delivery) . Also TCPP01-M12 VBUS OVP is set at 6 V with the resistor bridge on VBUS\_CTRL.

In this configuration, TCPP01-M12 internally presents the  $R_D$  resistors because the DB/ pin is tied to GND.



Figure 25. CC lines



- U6 : power mux for VCONN

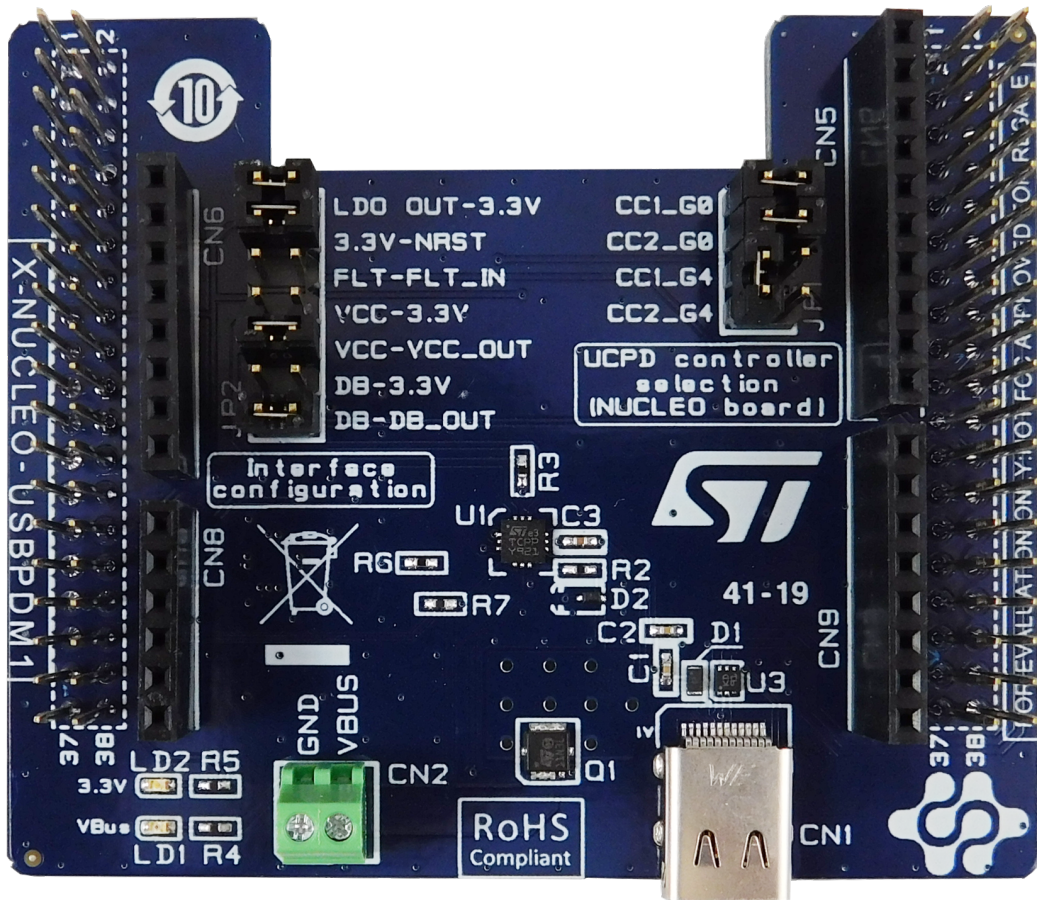
## 6.8 Development tools

The X-NUCLEO-USBPDM1 is an expansion board for the NUCLEO-G071RB and NUCLEO-G474RE development boards. It provides a straightforward means for evaluating USB Type-C power delivery in SINK mode based on TCPP01-M12.

The X-Nucleo-USBPDM1 associated with the Nucleo-G071RB have been certified by the USB-IF (TID: 3036) as a power sinking device, up to 100 W, with programmable power supply (PPS).

The USB Type-C connector can supply the STM32 Nucleo development board thanks to a 3.3 V LDO. Quick start guide and HW/SW prerequisites are listed [here](#).

Figure 26. X-Nucleo-USBPDM1 picture





## 7 PCB design recommendations

When routing the TCPP01-M12, please respect the following recommendations:

- Place the circuit as close as possible of the USB connector
- Place the ESD capacitor as close as possible of the TCPP01-M12

An example of routing with two layer board is shown here after.

For more informations on ESD protection layout and placement, please refer to [AN576: PCB layout optimization](#).

Figure 27. layer board for sink mode

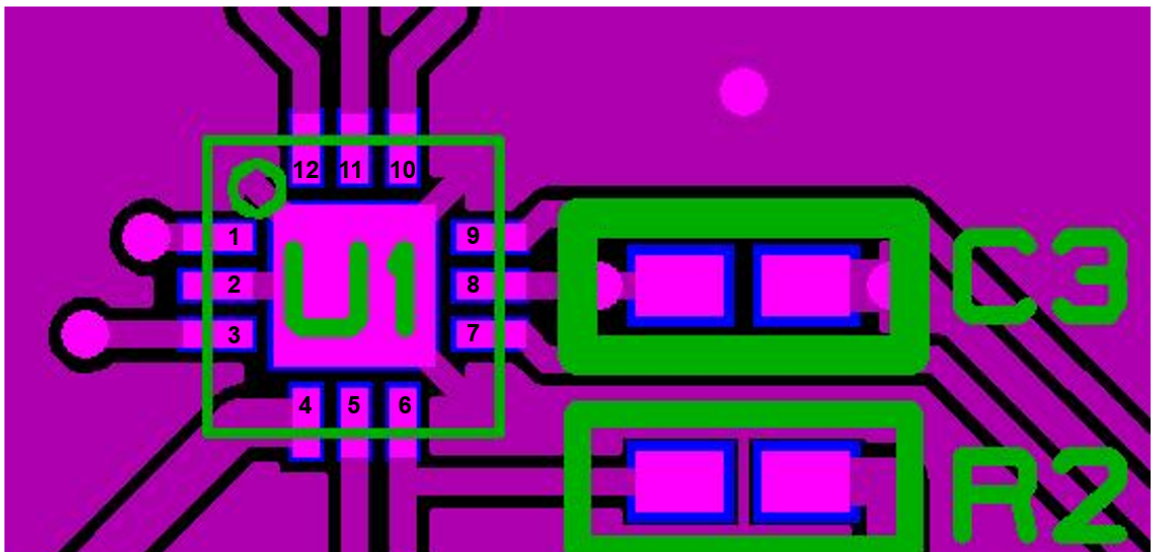
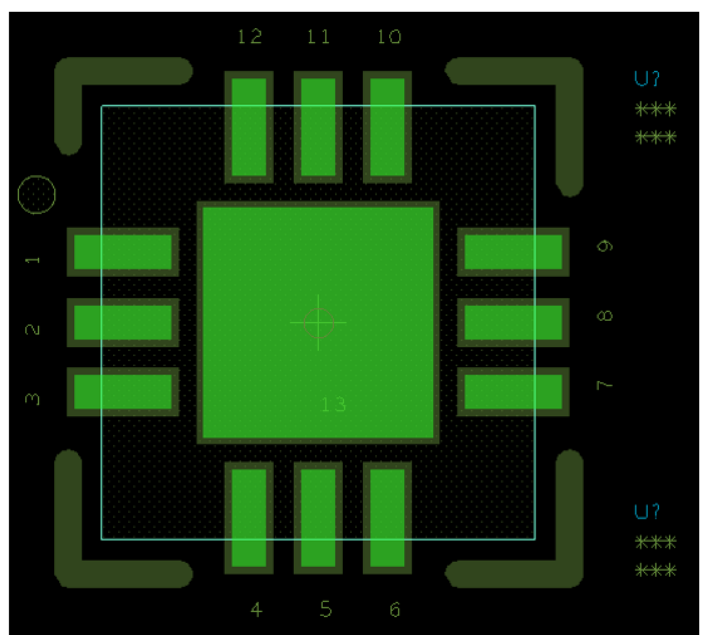
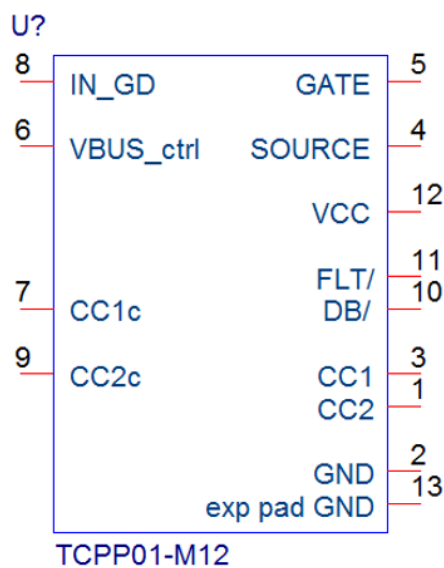


Figure 28. TCPP01-M12 symbol and footprint





## 8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 8.1 QFN12 package information

**Figure 29. QFN12 package outline**

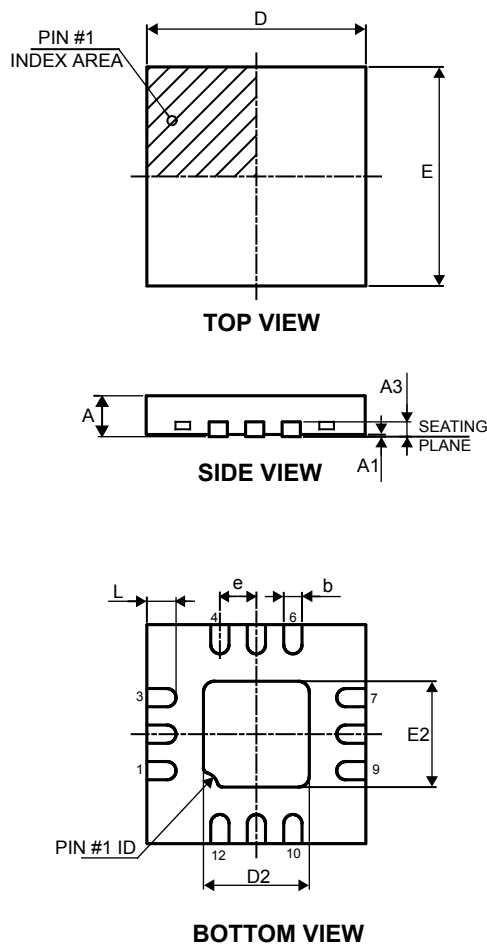


Table 15. QFN12 package mechanical data

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.20	
b	0.18	0.25	0.30
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D2	1.30	1.45	1.55
E2	1.30	1.45	1.55
e		0.50	
K	0.20		
L	0.30	0.40	0.50

Figure 30. QFN12 recommended footprint

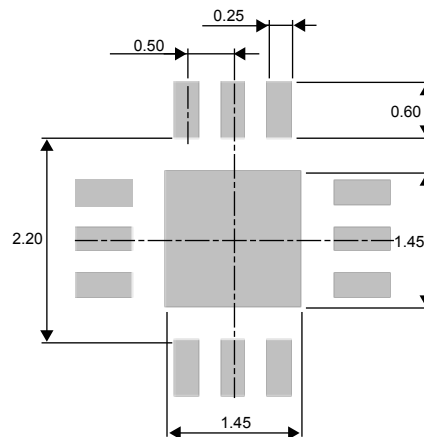
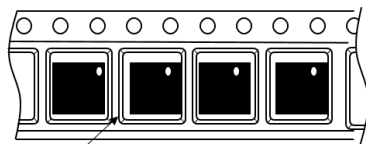


Figure 31. Package orientation in reel



Pin 1 located according to EIA-481

Note: Pocket dimensions are not on scale  
Pocket shape may vary depending on package

Figure 32. Tape and reel orientation

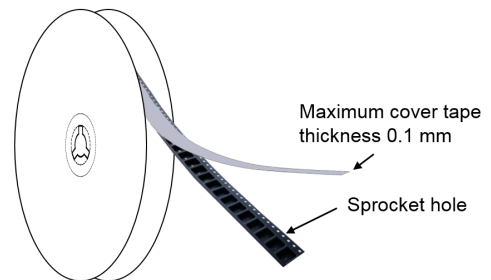


Figure 33. Reel dimensions (mm)

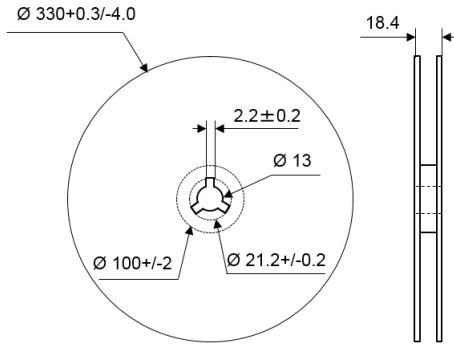


Figure 34. Inner box dimensions (mm)

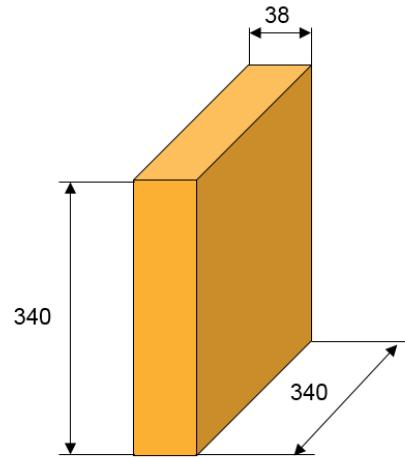
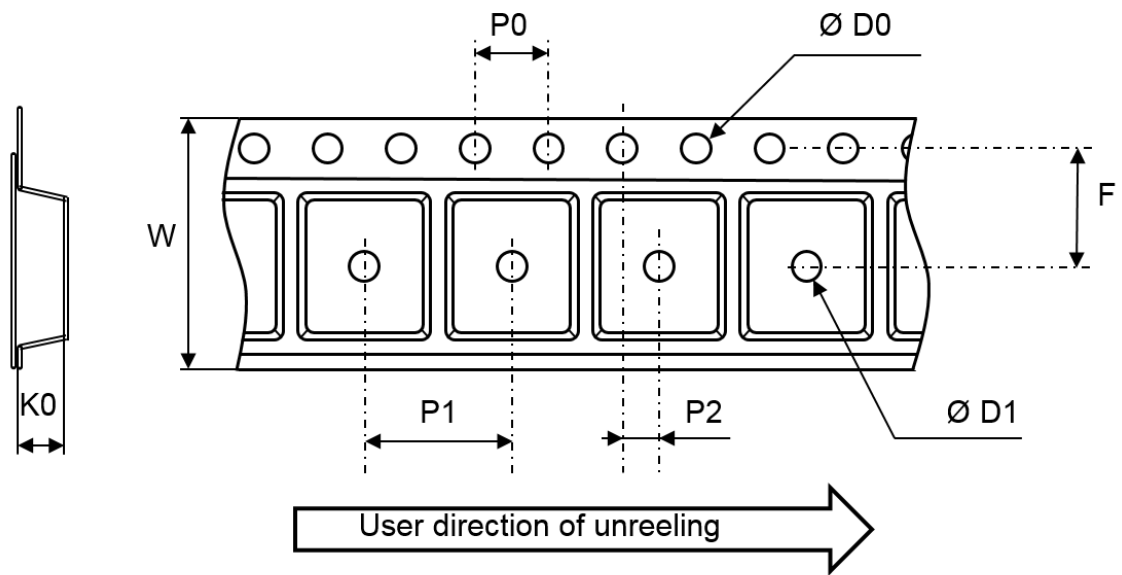


Figure 35. Tape and reel outline



Note: Pocket dimensions are not on scale  
Pocket shape may vary depending on package

**Table 16. Tape and reel mechanical data**

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
D0	1.50	1.55	1.60
D1	1.50		
F	5.45	5.50	5.55
K0	1.00	1.10	1.20
P0	3.90	4.0	4.10
P1	7.90	8.00	8.10
P2	1.95	2.00	2.05
W	11.70	12.00	12.30

## 9 Ordering information

Table 17. Ordering information

Order code	Marking	Package	Weight	Base qty.	Delivery mode
TCPP01-M12	TCPP	QFN12	23 mg	3000	Tape and reel

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## Revision history

**Table 18. Document revision history**

Date	Revision	Changes
06-Sep-2019	1	Initial release.
29-Jun-2020	2	Updated Section Product status / summary, Section Features, Figure 3, Figure 9, Figure 23 and Section 5.5.4 . Added Figure 10, Figure 11, Figure 24, Figure 16, Figure 18 and Figure 21. Added Table 12 and Table 14.
29-Sep-2020	3	Updated , Section 5.1 , Section 5.2.1 , Section 5.2.2 , Section 5.5.5 and Section 5.8 Development tools.
18-Dec-2020	4	Added <a href="#">Figure 9</a> and <a href="#">Section 5</a> .



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