TS27M2, TS27M2A, TS27M2B

Low-power CMOS dual operational amplifiers

Features

- Wide supply voltage range: 3 to 16 V
- Ultra-low consumption: 150 µA/op typ
- Output voltage swing to ground
- Excellent phase margin on capacitive load
- Gain bandwidth product: 1 MHz typ
- Vio down to 2 mV max. (B version)

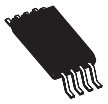
Description

The TS27x2 series are low-cost and low-power dual operational amplifiers designed to operate with high-voltage single or dual supplies. These operational amplifiers use the ST silicon gate CMOS process, providing an excellent consumption-speed ratio thanks to three different power consumptions, making them ideal for low-consumption applications:
I_{CC} = 10 µA/amp: TS27L2 (very low power),
I_{CC} = 150 µA/amp: TS27M2 (low power) and
I_{CC} = 1 mA/amp: TS272 (high speed)

The devices also offer a very high input impedance and extremely low input currents. Their main advantage compared to JFET devices is the very low input current drift with temperature (*Figure 3*).

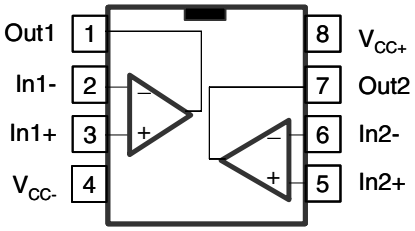
N
DIP8
(Plastic package)

D
SO-8
(Plastic micropackage)



P
TSSOP8
(Thin shrink small outline package)

Pin connections (top view)



1 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

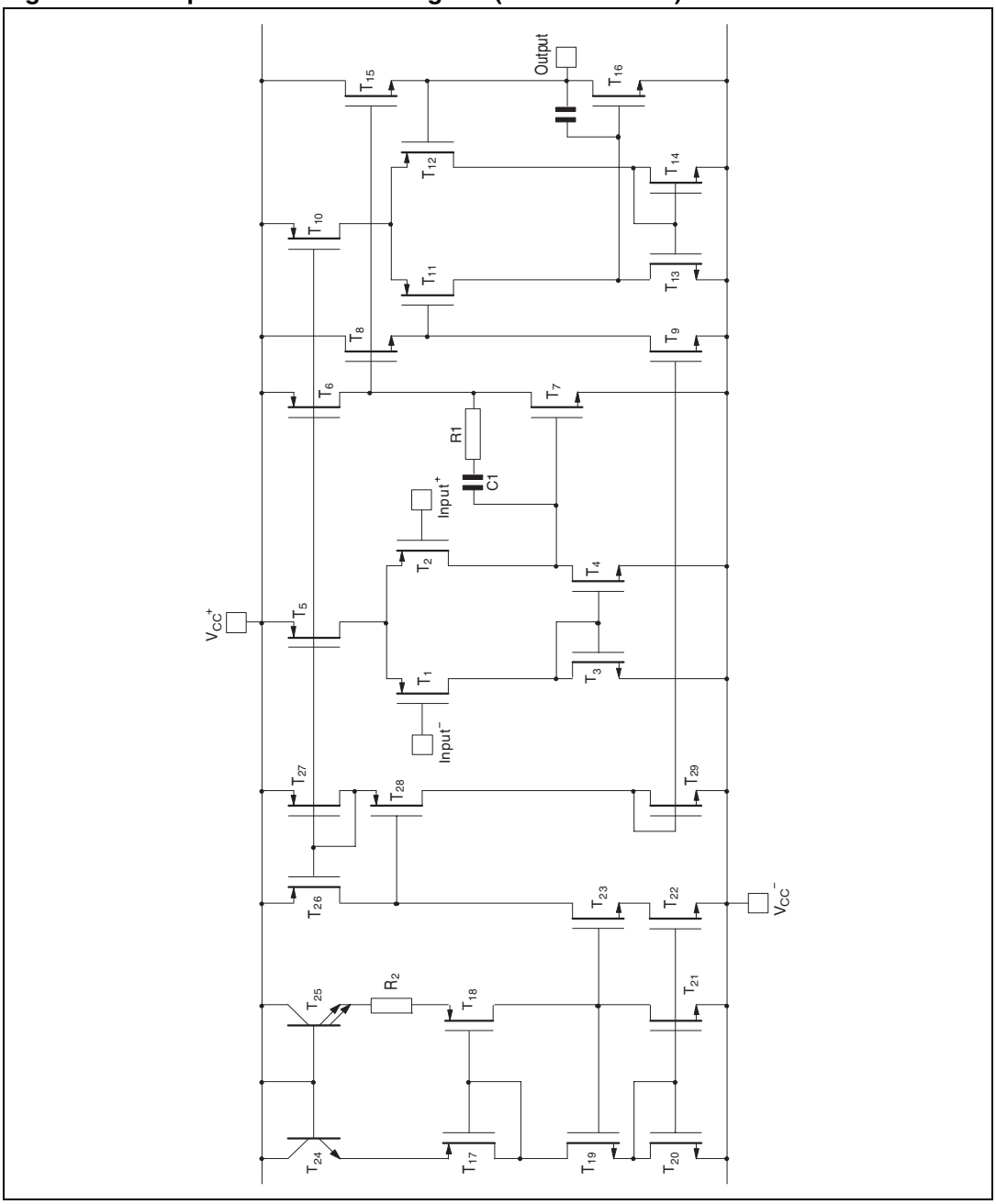
Symbol	Parameter	TS27M2x/Ax/Bx	Unit
V_{CC}^+	Supply voltage (1)	18	V
Vid	Differential input voltage (2)	±18	V
V_i	Input voltage (3)	-0.3 to 18	V
I_o	Output current for $V_{CC}^+ \geq 15V$	±30	mA
I_{in}	Input current	±5	mA
R_{thja} (4)(5)	SO-8 DIP8 TSSOP8	125 85 120	°C/W
T_{stg}	Storage temperature range	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
ESD	HBM: human body model(6)	500	V
	MM: machine model(7)	100	V
	CDM: charged device model(8)	1.5	kV

1. All values, except differential voltage are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input and the output voltages must never exceed the magnitude of the positive supply voltage.
4. Short-circuits can cause excessive heating and destructive dissipation.
5. R_{th} are typical values.
6. Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
7. Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.
8. Charged device model: all pins and the package are charged together to the specified voltage and then discharged directly to the ground through only one pin. This is done for all pins.

Table 2. Operating conditions

Symbol	Parameter	Value			Unit
		TS27M2C/AC/BC	TS27M2I/AI/BI	TS27M2M/AM/BM	
V_{CC}^+	Supply voltage	3 to 16			V
V_{icm}	Common mode input voltage range	0 to V_{CC}^+ - 1.5			V
Toper	Operating free air temperature range	0 to +70	-40 to +125	-55 to +125	°C

Figure 1. Simplified schematic diagram (for 1/2 TS27M2)



2 Electrical characteristics

Table 3. Electrical characteristics at V_{CC}+ = +10 V, V_{CC}- = 0 V, T_{amb} = +25° C (unless otherwise specified)

Symbol	Parameter	TS27M2xC			TS27M2xI TS27M2xM			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
DC performance								
V_{io}	Input offset voltage V_O = 1.4 V, V_{ic} = 0 V TS27M2 TS27M2A TS27M2B $T_{min} \leq T_{amb} \leq T_{max}$ TS27M2 TS27M2A TS27M2B		1.1 0.9 0.25	10 5 2 12 6.5 3		1.1 0.9 0.25	10 5 2 12 6.5 3.5	mV
DV_{io}	Input offset voltage drift		2			2		µV/°C
I_{io}	Input offset current (1) V_{ic} = 5 V, V_O = 5 V $T_{min} \leq T_{amb} \leq T_{max}$		1	 100		1	 200	pA
I_{ib}	Input bias current (1) V_{ic} = 5 V, V_O = 5 V $T_{min} \leq T_{amb} \leq T_{max}$		1	 150		1	 300	pA
V_{OH}	High level output voltage V_{id} = 100 mV, R_L = 100 lΩ $T_{min} \leq T_{amb} \leq T_{max}$	8.7 8.6	8.9		8.7 8.5	8.9		V
V_{OL}	Low level output voltage V_{id} = -100 mV			50			50	mV
A_{vd}	Large signal voltage gain V_{iC} = 5 V, R_L = 100 kΩ, V_o = 1 V to 6 V $T_{min} \leq T_{amb} \leq T_{max}$	30 20	50		30 10	50		V/mV
CMR	Common mode rejection ratio V_{iC} = 1 V to 7.4 V, V_o = 1.4 V	65	80		65	80		dB
SVR	Supply voltage rejection ratio V_{CC}^+ = 5 V to 10 V, V_o = 1.4 V	60	80		60	80		dB
I_{CC}	Supply current (per amplifier) A_v = 1, no load, V_o = 5 V $T_{min} \leq T_{amb} \leq T_{max}$		150	200 250		150	200 300	µA
I_o	Output short circuit current V_o = 0 V, V_{id} = 100 mV	45	60			60		mA
I_{sink}	Output sink current V_o = V_{CC}, V_{id} = -100 mV	34	45			45		mA

Table 3. Electrical characteristics at V_{CC}+ = +10 V, V_{CC}- = 0 V, T_{amb} = +25° C (unless otherwise specified) (continued)

Symbol	Parameter	TS27M2xC			TS27M2xI TS27M2xM			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
AC performance								
GBP	Gain bandwidth product A_v = 40 dB, R_L = 100 kΩ, C_L = 100 pF, f_{in} = 100 kHz	0.5	1		0.5	1		MHz
SR	Slew rate at unity gain R_L = 100 kΩ, C_L = 100 pF, V_i = 3 to 7 V	0.3	0.6		0.3	0.6		V/µs
ϕm	Phase margin at unity gain A_v = 40 dB, R_L = 100 kΩ, C_L = 100 pF		45			45		Degrees
K_{OV}	Overshoot factor		30			30		%
e_n	Equivalent input noise voltage f = 1 kHz, R_s = 100 Ω		38			38		$\frac{nV}{\sqrt{Hz}}$
V_{o1}/V_{o2}	Channel separation		120			120		dB

1. Maximum values including unavoidable inaccuracies of industrial tests.

3 Typical characteristics

Figure 2. Supply current (each amplifier) versus supply voltage

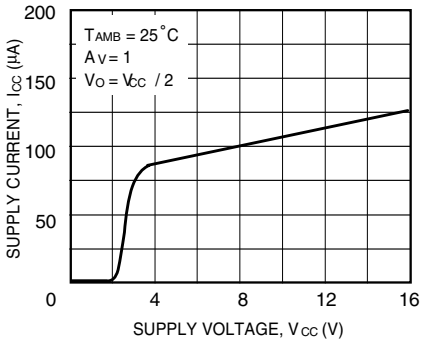


Figure 3. Input bias current versus free air temperature

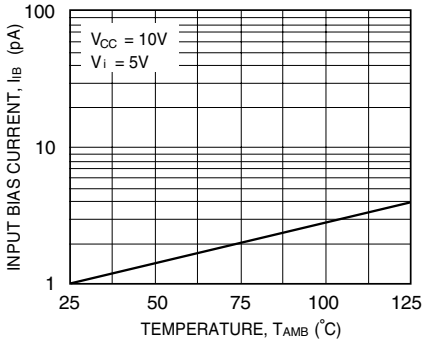


Figure 4. High level output voltage versus high level output current

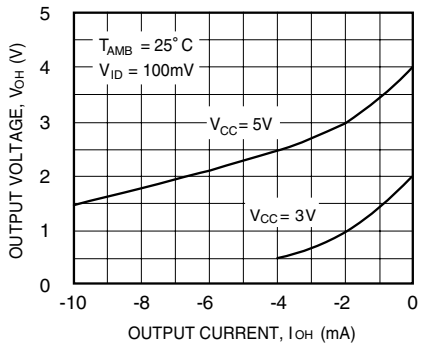


Figure 5. High level output voltage versus high level output current

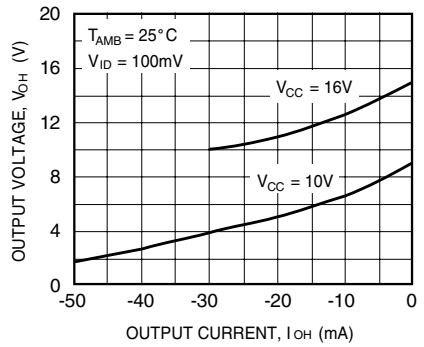


Figure 6. Low level output voltage versus low level output current

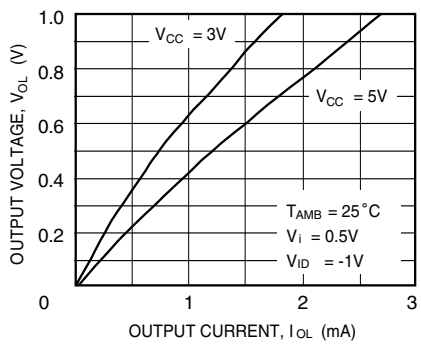


Figure 7. Low level output voltage versus low level output current

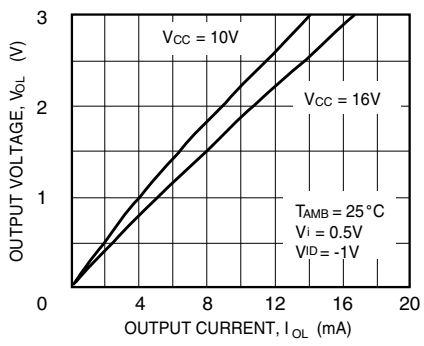


Figure 8. Open-loop frequency response and phase shift

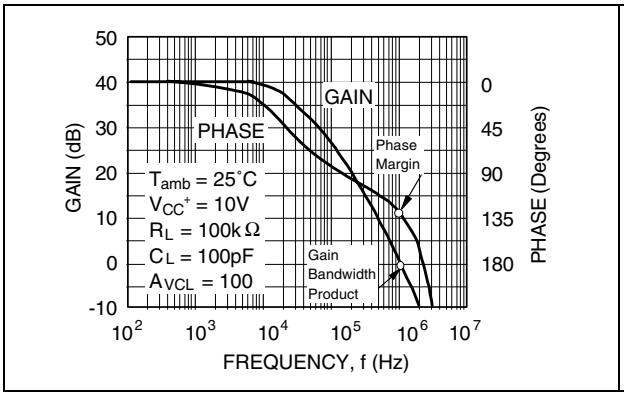


Figure 9. Gain bandwidth product versus supply voltage

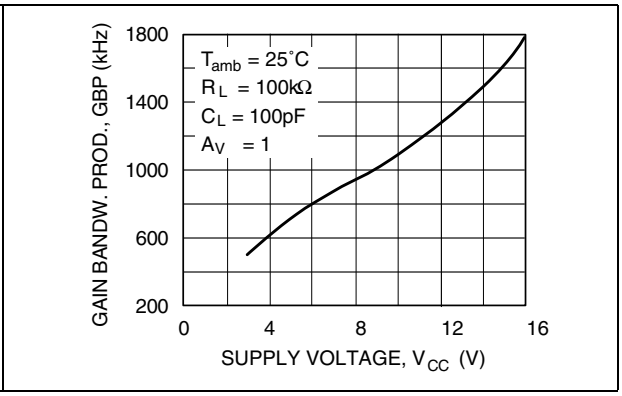


Figure 10. Phase margin versus supply voltage

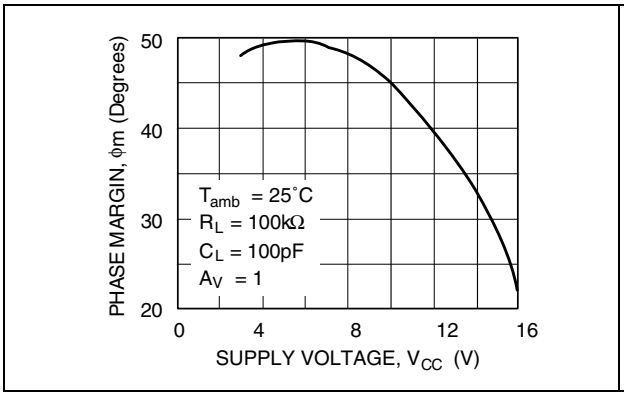


Figure 11. Phase margin versus capacitive load

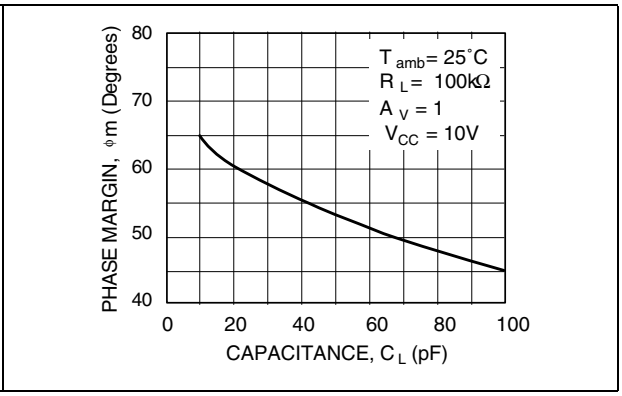


Figure 12. Slew rate versus supply voltage

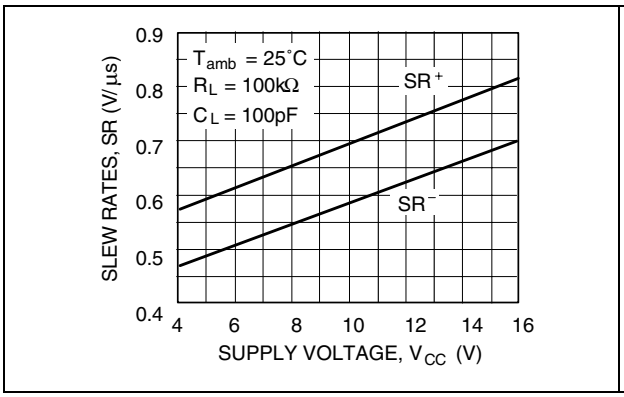
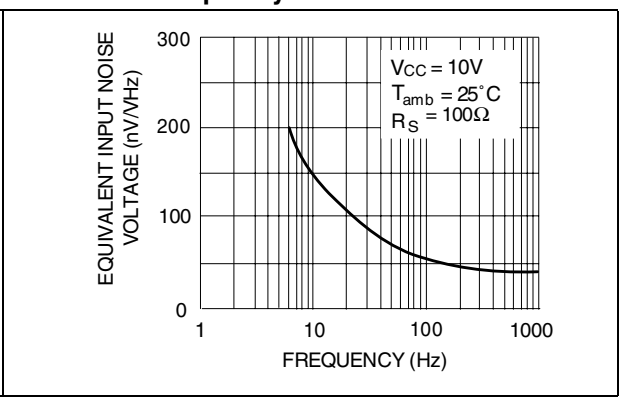


Figure 13. Input voltage noise versus frequency



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.
ECOPACK® is an ST trademark.

4.1 DIP8 package information

Figure 14. DIP8 package mechanical drawing

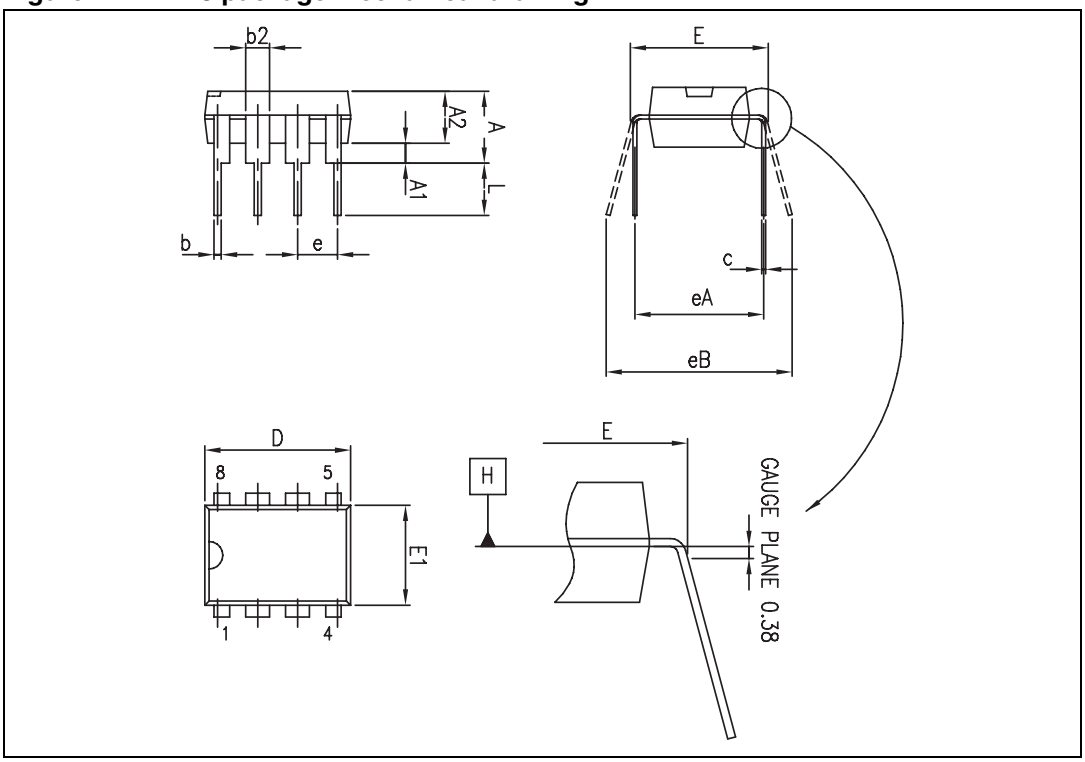


Table 4. DIP8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.33			0.210
A1	0.38			0.015		
A2	2.92	3.30	4.95	0.115	0.130	0.195
b	0.36	0.46	0.56	0.014	0.018	0.022
b2	1.14	1.52	1.78	0.045	0.060	0.070
c	0.20	0.25	0.36	0.008	0.010	0.014
D	9.02	9.27	10.16	0.355	0.365	0.400
E	7.62	7.87	8.26	0.300	0.310	0.325
E1	6.10	6.35	7.11	0.240	0.250	0.280
e		2.54			0.100	
eA		7.62			0.300	
eB			10.92			0.430
L	2.92	3.30	3.81	0.115	0.130	0.150

4.2 SO-8 package information

Figure 15. SO-8 package mechanical drawing

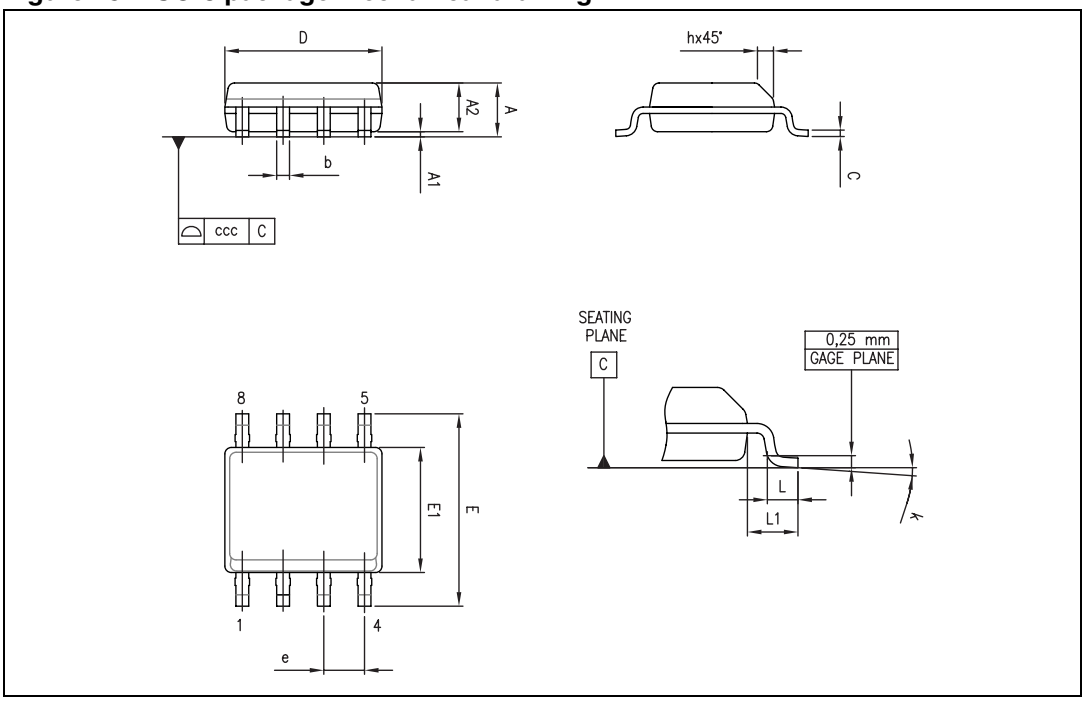


Table 5. SO-8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
L1		1.04			0.040	
k	1°		8°	1°		8°
ccc			0.10			0.004

4.3 TSSOP8 package information

Figure 16. TSSOP8 package mechanical drawing

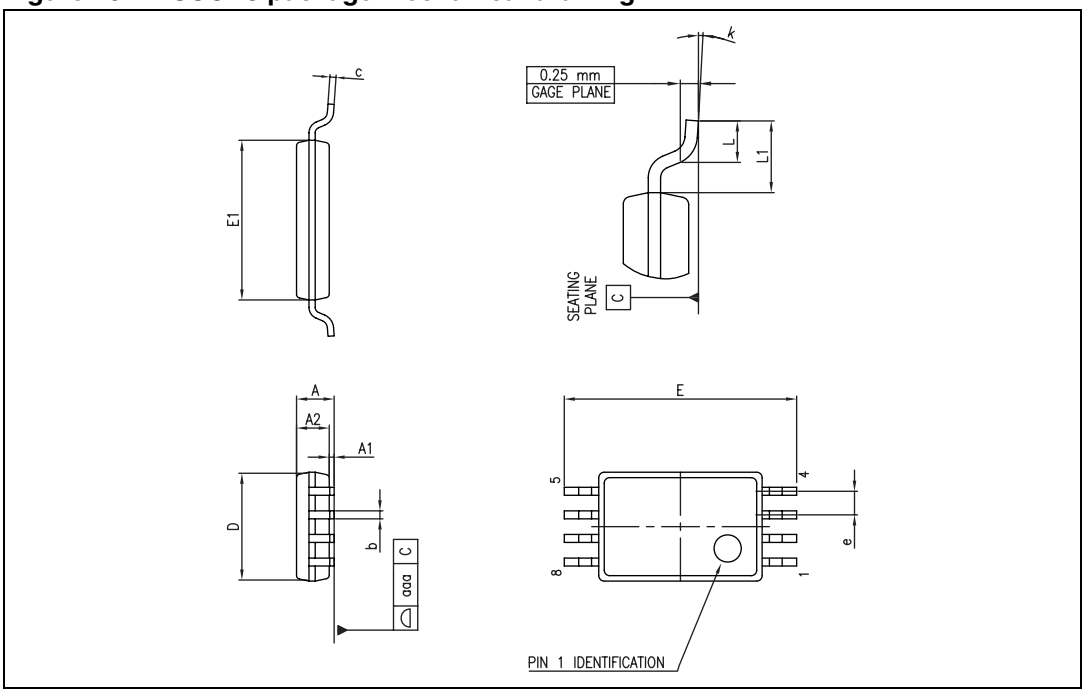


Table 6. TSSOP8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.20			0.047
A1	0.05		0.15	0.002		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
e		0.65			0.0256	
k	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1			0.039	
aaa			0.10			0.004

5 Ordering information

Table 7. Order codes

Part number	Temperature range	Package	Packing	Marking
TS27M2CD TS27M2CDT	0° C to +70° C	SO-8	Tube Tape & reel	27M2C
TS27M2CN		DIP8	Tube	TS27M2CN
TS27M2CPT		TSSOP8	Tube Tape & reel	27M2C
TS27M2ACD TS27M2ACDT		SO-8	Tube Tape & reel	27M2AC
TS27M2ACN		DIP8	Tube	S27M2ACN
TS27M2ACPT		TSSOP8	Tape & reel	2M2AC
TS27M2BCD TS27M2BCDT		SO-8	Tube Tape & reel	27M2BC
TS27M2BCN		DIP8	Tube	S27M2BCN
TS27M2BCPT		TSSOP8	Tape & reel	2M2BC
TS27M2ID TS27M2IDT	-40° C to +125° C	SO-8	Tube Tape & reel	27M2I
TS27M2IN		DIP8	Tube	TS27M2IN
TS27M2IPT		TSSOP8	Tape & reel	27M2I
TS27M2AID TS27M2AIDT		SO-8	Tube Tape & reel	27M2AI
TS27M2AIN		DIP8	Tube	S27M2AIN
TS27M2AIPT		TSSOP8	Tape & reel	2M2AI
TS27M2BID TS27M2BIDT		SO-8	Tube Tape & reel	27M2BI
TS27M2BIN		DIP8	Tube	S27M2BIN
TS27M2BIPT		TSSOP8	Tape & reel	2M2BI

6 Revision history

Table 8. Document revision history

Date	Revision	Changes
01-Nov-2001	1	Initial release.
18-Aug-2009	2	Updated document format. Added ESD and Rthja information in *Table 1: Absolute maximum ratings*. Removed block diagram. Added minimum values for Io, GBP and SR parameters in *Table 3*. Added order codes in *Table 7*.

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