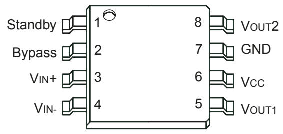
life.augmented

TS419, TS421

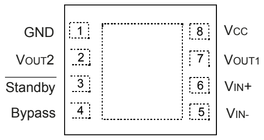
Datasheet

360 mW mono amplifier with standby mode

TS419IST : MiniSO8



TS421IQT : DFN8



Maturity status link
TS3431

Features

- Operating from V_{CC} = 2 V to 5.5 V
- Standby mode active high (TS419) or low (TS421)
- Output power into 16 Ω: 367 mW @ 5 V with 10% THD+N max or 295 mW @ 5 V and 110 mW @ 3.3 V with 1% THD+N max.
- Low current consumption: 2.5 mA max.
- High signal-to-noise ratio: 95 dB (A) at 5 V
- PSRR: 56 dB typ. at 1 kHz, 46 dB at 217 Hz
- Short-circuit limitation
- ON/OFF click reduction circuitry
- Available in MiniSO8 and DFN 3x3

Applications

- 16/32 Ω earpiece or receiver speaker driver
- Mobile and cordless phones (analog / digital)
- PDAs & computers
- Portable appliances

Description

The TS419/TS421 is a monaural audio power amplifier driving in BTL mode a 16 or 32 Ω earpiece or receiver speaker. The main advantage of this configuration is to get rid of bulky output capacitors.

Capable of descending to low voltages, it delivers up to 220 mW per channel (into 16 Ω loads) of continuous average power with 0.2% THD+N in the audio bandwidth from a 5 V power supply.

An externally controlled standby mode reduces the supply current to 10 nA (typ.). The TS419 / TS421 can be configured by external gain-setting resistors.

1 Maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage [(1)]	6	V
V_i	Input voltage	-0.3 V to V_{CC} +0.3 V	V
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
R_{thja}	Thermal resistance junction-to-ambient MiniSO8 DFN8	215 70	°C/W
P_d	Power dissipation [(2)] MiniSO8 DFN8	0.58 1.79	W
ESD	Human body model (pin to pin): TS419 [(3)], TS421	1.5	kV
ESD	Machine Model - 220 pF - 240 pF (pin to pin)	100	V
Latch-up	Latch-up Immunity (All pins)	200	mA
	Lead temperature (soldering, 10 s)	250	°C
	Output short-circuit to V_{CC} or GND	continuous [(4)]	

1. *All voltage values are measured with respect to the ground pin.*
2. *Pd has been calculated with Tamb = 25 °C, Tj = 150 °C.*
3. *TS419 stands 1.5 KV on all pins except standby pin which stands 1 KV*
4. *Attention must be paid to continous power dissipation (V_{DD} x 300 mA). Exposure of the IC to a short circuit for an extended time period is dramatically reducing product life expectancy.*

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2 to 5.5	V
R_L	Load resistor	≥ 16	Ω
T_{oper}	Operating free air temperature range	-40 to +85	°C
C_L	Load capacitor R_L = 16 to 100 Ω R_L > 100 Ω	400 100	pF
V_{ICM}	Common mode input voltage range	GND to V_{CC} - 1 V	V
V_{STB}	Standby voltage input TS421 ACTIVE / TS419 in STANDBY TS421 in STANDBY / TS419 ACTIVE	$1.5 \leq V_{STB} \leq V_{CC}$ $GND \leq V_{STB} \leq 0.4$ [(1)]	V
R_{thja}	Thermal resistance junction-to-ambient MiniSO8 DFN8 [(2)]	190 41	°C/W

Symbol	Parameter	Value	Unit
T_{wu}	Wake-up time from standby to active mode (Cb = 1 µF) (3)	≥ 0.12	s

1. *The minimum current consumption ($I_{STANDBY}$) is guaranteed at V_{CC} (TS419) or GND (TS421) for the whole temperature range.*
2. *When mounted on a 4-layer PCB.*
3. *For more details on T_{WU}, please refer to application note section on Wake-up time page 28.*

2 Typical application schematics

Figure 1. Application schematics

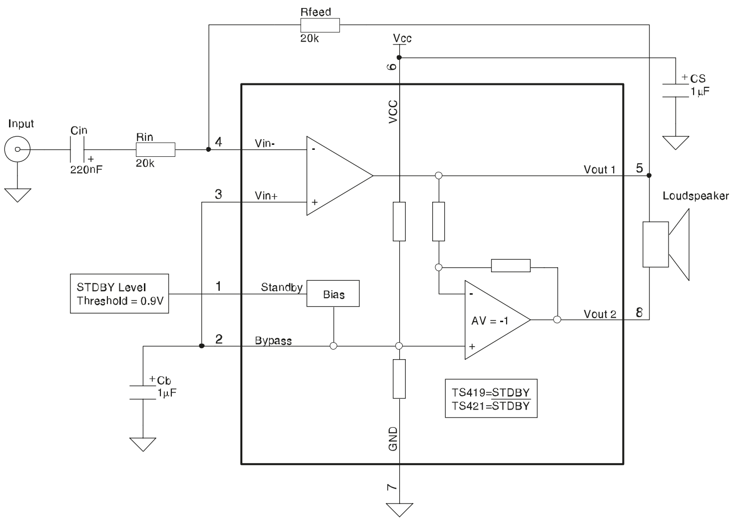


Table 3. Application components information

Components	Functional description
R_{IN}	Inverting input resistor which sets the closed loop gain in conjunction with R_{FEED}. This resistor also forms a high pass filter with C_{IN} (f_{cl} = 1 / (2 x P_i x R_{IN} x C_{IN})).
C_{IN}	Input coupling capacitor which blocks the DC voltage at the amplifier’s input terminal.
R_{FEED}	Feedback resistor which sets the closed loop gain in conjunction with R_{IN}. A_V = Closed Loop Gain= 2 x R_{FEED} / R_{IN}.
C_S	Supply bypass capacitor which provides power supply filtering.
C_B	Bypass capacitor which provides half supply filtering.

3 Electrical characteristics

Table 4. Electrical characteristics V_{CC} = +5 V, GND = 0 V, T_{amb} = 25 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current No input signal, no load		6	8	mA
$I_{STANDBY}$	Standby current No input signal, $V_{STANDBY}$ = GND for TS421 No input signal, $V_{STANDBY}$ = V_{CC} for TS419		10	1000	nA
V_{OO}	Output offset voltage No input signal, R_L = 16 Ω or 32 Ω, R_{feed} = 20 kΩ		5	25	mV
P_O	Output power THD+N = 0.1% Max, F = 1 kHz, R_L = 32 Ω		190		mW
	Output power THD+N = 1% Max, F = 1 kHz, R_L = 32 Ω	166	207		
	Output power THD+N = 10% Max, F = 1 kHz, R_L = 32 Ω		258		
	Output power THD+N = 0.1% Max, F = 1 kHz, R_L = 16 Ω		270		
	Output power THD+N = 1% Max, F = 1 kHz, R_L = 16 Ω	240	295		
	Output power THD+N = 10% Max, F = 1 kHz, R_L = 16 Ω		367		
THD + N	Total harmonic distortion + noise (Av = 2) R_L = 32 Ω, P_{out} = 150 mW, 20 Hz ≤ F ≤ 20 kHz R_L = 16 Ω, P_{out} = 220 mW, 20 Hz ≤ F ≤ 20 kHz		0.15 0.2		%
PSRR	Power supply rejection ratio (Av = 2) F = 1 kHz, V_{ripple} = 200 mVpp, input grounded, C_b = 1 µF	50	56		dB
SNR	Signal-to-Noise Ratio (Filter Type A, Av = 2) (1) (R_L = 32 Ω, THD +N < 0.5%, 20 Hz ≤ F ≤ 20 kHz)	85	98		dB
ϕ_M	Phase margin at unity gain R_L = 16 Ω, C_L = 400 pF		58		Degrees
GM	Gain margin R_L = 16 Ω, C_L = 400 pF		18		dB
GBP	Gain bandwidth product R_L = 16 Ω		1.1		MHz
SR	Slew rate R_L = 16 Ω		0.4		V/µS

1. *Guaranteed by design and evaluation.*

Table 5. Electrical characteristics V_{CC} = +3.3 V, GND = 0 V, T_{amb} = 25 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current No input signal, no load		1.8	2.5	mA
$I_{STANDBY}$	Standby current No input signal, $V_{STANDBY}$ = GND for TS421 No input signal, $V_{STANDBY}$ = V_{CC} for TS419		10	1000	nA
V_{OO}	Output offset voltage No input signal, R_L = 16 Ω or 32 Ω, R_{feed} = 20 kΩ		5	25	mV
P_O	Output power THD+N = 0.1% Max, F = 1 kHz, R_L = 32 Ω		75		mW
	Output power THD+N = 1% Max, F = 1 kHz, R_L = 32 Ω	65	81		
	Output power THD+N = 10% Max, F = 1 kHz, R_L = 32 Ω		102		
	Output power THD+N = 0.1% Max, F = 1 kHz, R_L = 16 Ω		104		
	Output power THD+N = 1% Max, F = 1 kHz, R_L = 16 Ω	91	113		
	Output power THD+N = 10% Max, F = 1 kHz, R_L = 16 Ω		143		
THD + N	Total harmonic distortion + noise (Av = 2) R_L = 32 Ω, P_{out} = 150 mW, 20 Hz ≤ F ≤ 20 kHz R_L = 16 Ω, P_{out} = 220 mW, 20 Hz ≤ F ≤ 20 kHz		0.15 0.2		%
PSRR	Power supply rejection ratio (Av = 2) F = 1 kHz, V_{ripple} = 200 mVpp, input grounded, C_b = 1 µF	50	56		dB
SNR	Signal-to-Noise Ratio (Weighted A, Av = 2) (R_L = 32 Ω, THD +N < 0.5%, 20 Hz ≤ F ≤ 20 kHz)	82	94		dB
ϕ_M	Phase margin at unity gain R_L = 16 Ω, C_L = 400 pF		58		Degrees
GM	Gain margin R_L = 16 Ω, C_L = 400 pF		18		dB
GBP	Gain bandwidth product R_L = 16 Ω		1.1		MHz
SR	Slew rate R_L = 16 Ω		0.4		V/µS

Note: All electrical values are guaranted with correlation measurements at 2 V and 5 V.

Table 6. Electrical characteristics V_{CC} = +2.5 V, GND = 0 V, T_{amb} = 25 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current No input signal, no load		1.7	2.5	mA
$I_{STANDBY}$	Standby current No input signal, $V_{STANDBY}$ = GND for TS421 No input signal, $V_{STANDBY}$ = V_{CC} for TS419		10	1000	nA
V_{OO}	Output offset voltage No input signal, R_L = 16 Ω or 32 Ω, R_{feed} = 20 kΩ		5	25	mV
P_O	Output power THD+N = 0.1% Max, F = 1 kHz, R_L = 32 Ω		37		mW
	Output power THD+N = 1% Max, F = 1 kHz, R_L = 32 Ω	32	41		
	Output power THD+N = 10% Max, F = 1 kHz, R_L = 32 Ω		52		
	Output power THD+N = 0.1% Max, F = 1 kHz, R_L = 16 Ω		50		
	Output power THD+N = 1% Max, F = 1 kHz, R_L = 16 Ω	44	55		
	Output power THD+N = 10% Max, F = 1 kHz, R_L = 16 Ω		70		
THD + N	Total harmonic distortion + noise (Av = 2) R_L = 32 Ω, P_{out} = 150 mW, 20 Hz ≤ F ≤ 20 kHz R_L = 16 Ω, P_{out} = 220 mW, 20 Hz ≤ F ≤ 20 kHz		0.15 0.2		%
PSRR	Power supply rejection ratio (Av = 2) F = 1 kHz, V_{ripple} = 200 mVpp, input grounded, C_b = 1 µF	50	56		dB
SNR	Signal-to-Noise Ratio (Weighted A, Av = 2) (R_L = 32 Ω, THD +N < 0.5%, 20 Hz ≤ F ≤ 20 kHz)	80	91		dB
ϕ_M	Phase margin at unity gain R_L = 16 Ω, C_L = 400 pF		58		Degrees
GM	Gain margin R_L = 16 Ω, C_L = 400 pF		18		dB
GBP	Gain bandwidth product R_L = 16 Ω		1.1		MHz
SR	Slew rate R_L = 16 Ω		0.4		V/µS

Note: All electrical values are guaranted with correlation measurements at 2 V and 5 V.

Table 7. Electrical characteristics V_{CC} = +2 V, GND = 0 V, T_{amb} = 25 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current No input signal, no load		1.7	2.5	mA
$I_{STANDBY}$	Standby current No input signal, $V_{STANDBY}$ = GND for TS421 No input signal, $V_{STANDBY}$ = V_{CC} for TS419		10	1000	nA
V_{OO}	Output offset voltage No input signal, R_L = 16 Ω or 32 Ω, R_{feed} = 20 kΩ		5	25	mV
P_O	Output power THD+N = 0.1% Max, F = 1 kHz, R_L = 32 Ω		20		mW
	Output power THD+N = 1% Max, F = 1 kHz, R_L = 32 Ω	19	23		
	Output power THD+N = 10% Max, F = 1 kHz, R_L = 32 Ω		30		
	Output power THD+N = 0.1% Max, F = 1 kHz, R_L = 16 Ω		26		
	Output power THD+N = 1% Max, F = 1 kHz, R_L = 16 Ω	24	30		
	Output power THD+N = 10% Max, F = 1 kHz, R_L = 16 Ω		40		
THD + N	Total harmonic distortion + noise (Av = 2) R_L = 32 Ω, P_{out} = 150 mW, 20 Hz ≤ F ≤ 20 kHz R_L = 16 Ω, P_{out} = 220 mW, 20 Hz ≤ F ≤ 20 kHz		0.1 0.15		%
PSRR	Power supply rejection ratio (Av = 2) (1) F = 1 kHz, V_{ripple} = 200 mVpp, input grounded, C_b = 1 µF	49	54		dB
SNR	Signal-to-Noise Ratio (Weighted A, Av = 2) (1) (R_L = 32 Ω, THD +N < 0.5%, 20 Hz ≤ F ≤ 20 kHz)	80	89		dB
ϕ_M	Phase margin at unity gain R_L = 16 Ω, C_L = 400 pF		58		Degrees
GM	Gain margin R_L = 16 Ω, C_L = 400 pF		20		dB
GBP	Gain bandwidth product R_L = 16 Ω		1.1		MHz
SR	Slew rate R_L = 16 Ω		0.4		V/µS

1. *Guaranteed by design and evaluation.*

4 Electrical characteristics curves

Figure 2. Open loop gain and phase vs. frequency

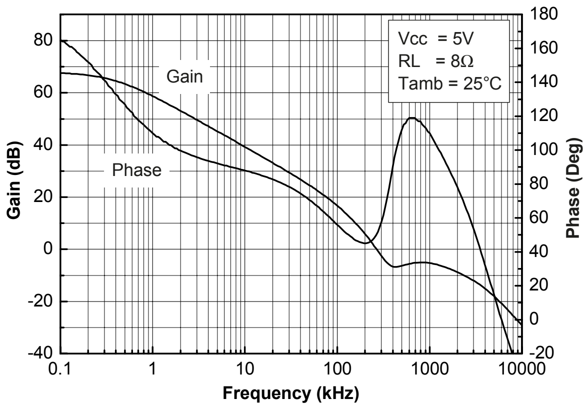


Figure 3. Open loop gain and phase vs. frequency Vcc = 2 V

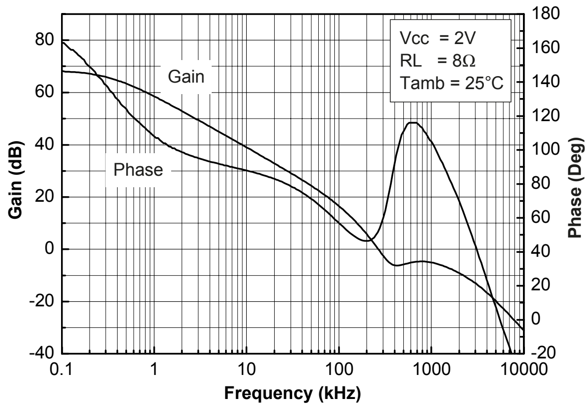


Figure 4. Open loop gain and phase vs. frequency Vcc = 5 V

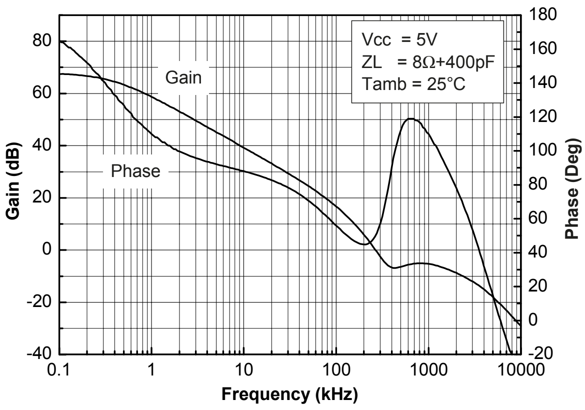


Figure 5. Open loop gain and phase vs. frequency ZL = 8 Ω

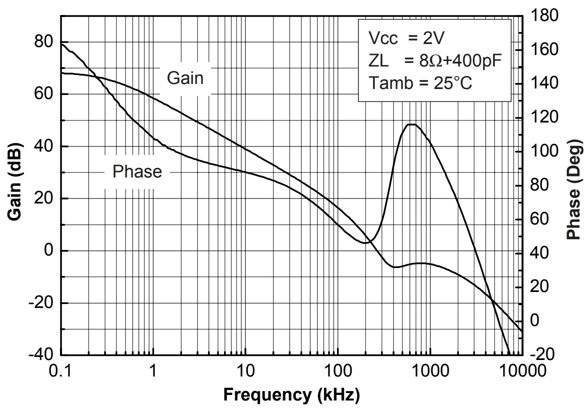


Figure 6. **Open loop gain and phase vs. frequency RL = 16 Ω**

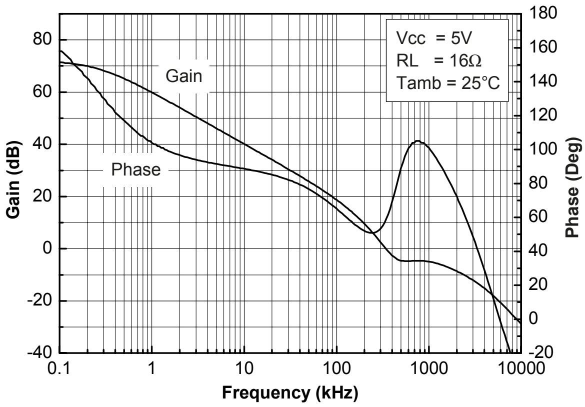


Figure 7. **Open loop gain and phase vs. frequency RL = 16 Ω, Vcc = 2 V**

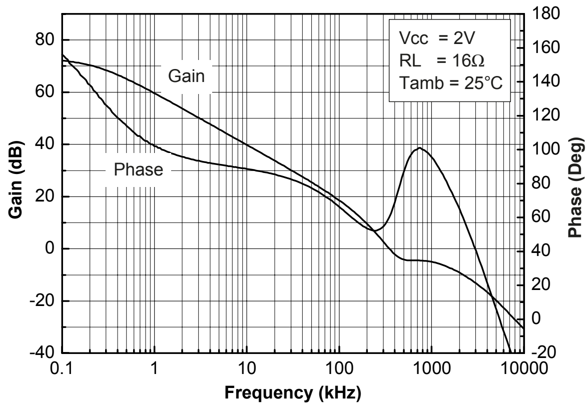


Figure 8. **Open loop gain and phase vs. frequency ZL = 16 Ω, Vcc = 5 V**

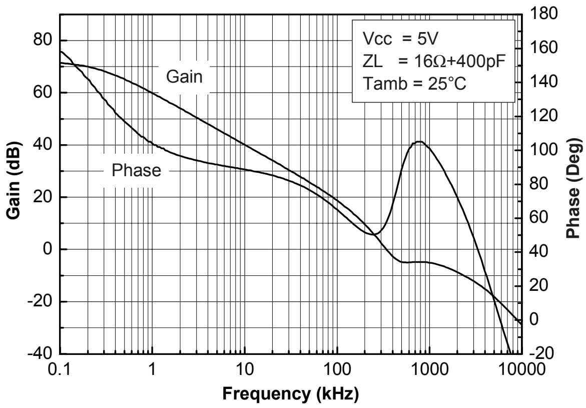


Figure 9. **Open loop gain and phase vs. frequency ZL = 16 Ω, Vcc = 2 V**

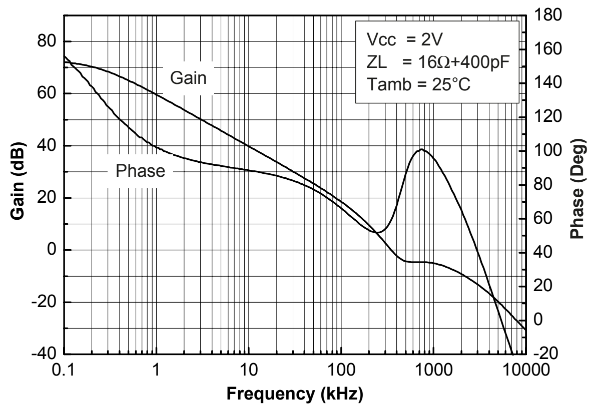


Figure 10. Open loop gain and phase vs. frequency RL = 32 Ω

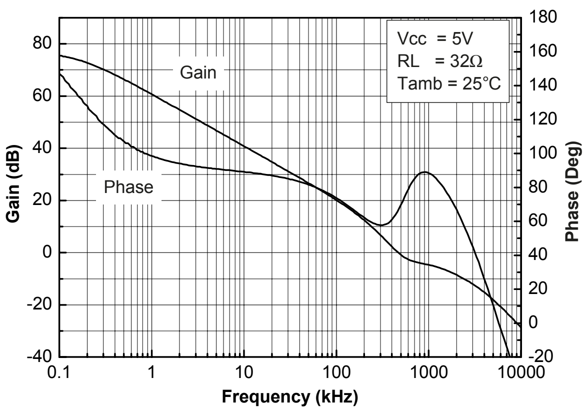


Figure 11. Open loop gain and phase vs. frequency RL = 32 Ω, Vcc = 2 V

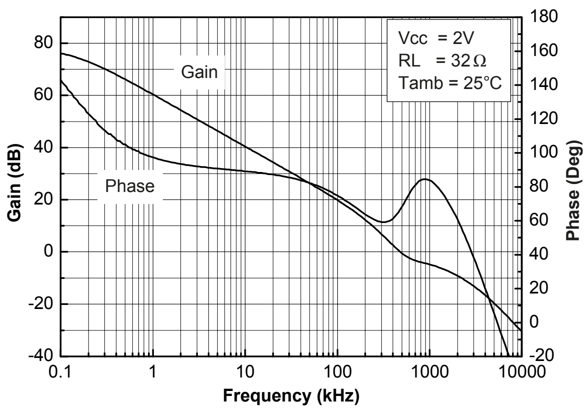


Figure 12. Open loop gain and phase vs. frequency ZL = 32 Ω

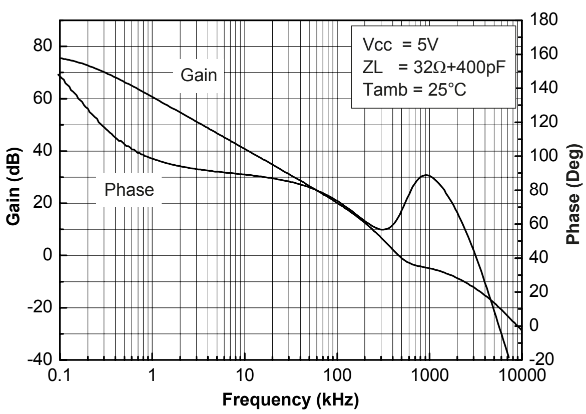


Figure 13. Open loop gain and phase vs. frequency ZL = 32 Ω, Vcc = 2 V

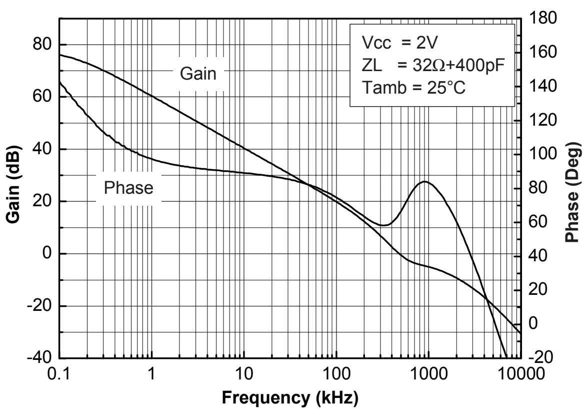


Figure 14. Current consumption vs. power supply voltage

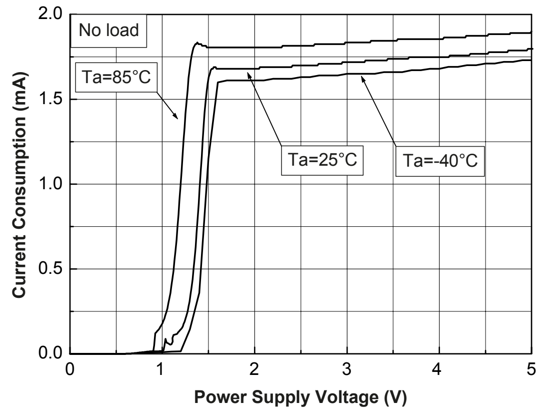


Figure 15. Current consumption vs. standby voltage Vcc = 5 V

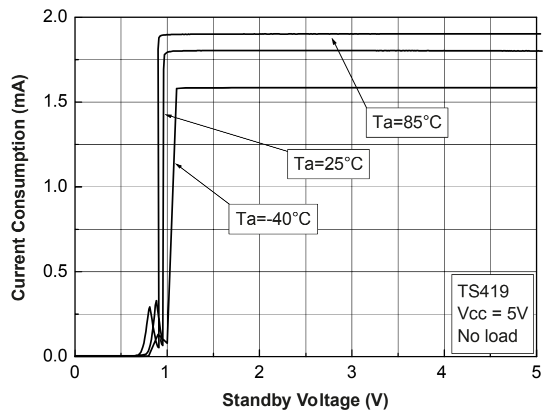


Figure 16. Current consumption vs. standby voltage Vcc = 3.3 V

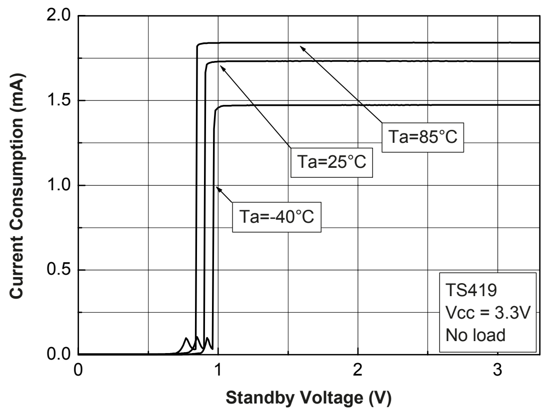


Figure 17. Current consumption vs. standby voltage Vcc = 2 V

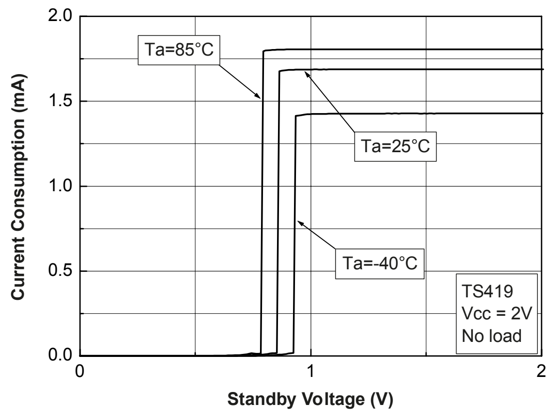


Figure 18. Current consumption vs. standby voltage Vcc = 5 V (TS421)

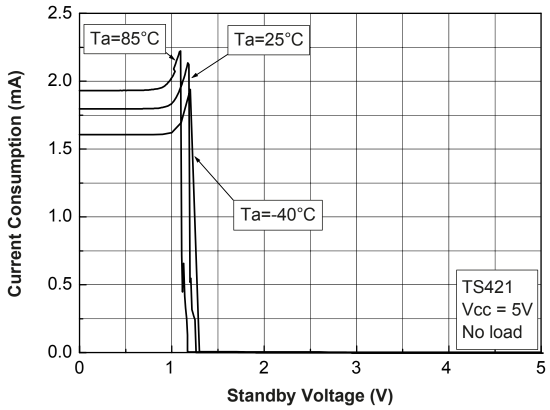


Figure 19. Current consumption vs. standby voltage Vcc = 3.3 V (TS421)

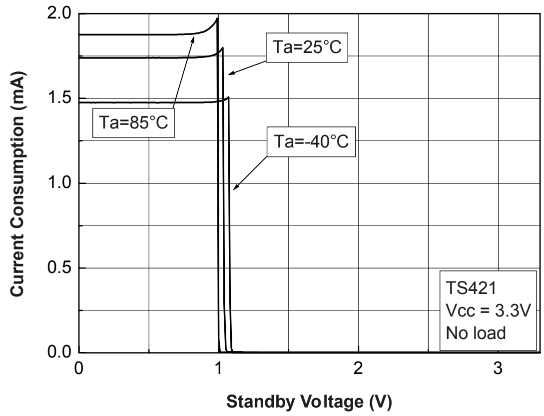


Figure 20. Current consumption vs. standby voltage Vcc = 2 V (TS421)

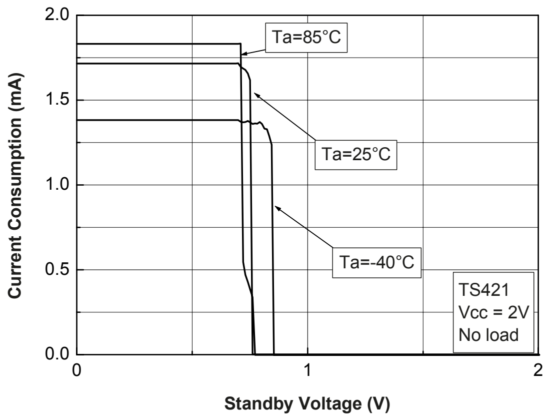


Figure 21. Output power vs. power supply voltage RL = 8 Ω

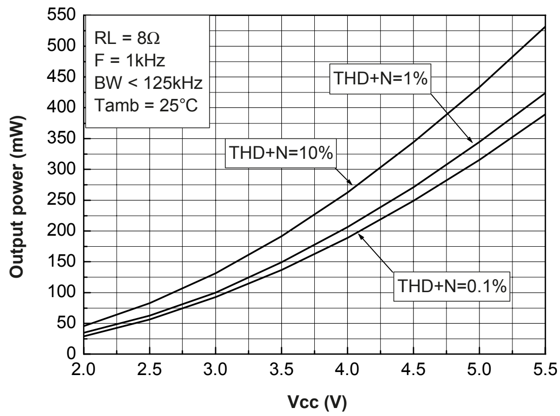


Figure 22. Output power vs. power supply voltage RL = 16 Ω

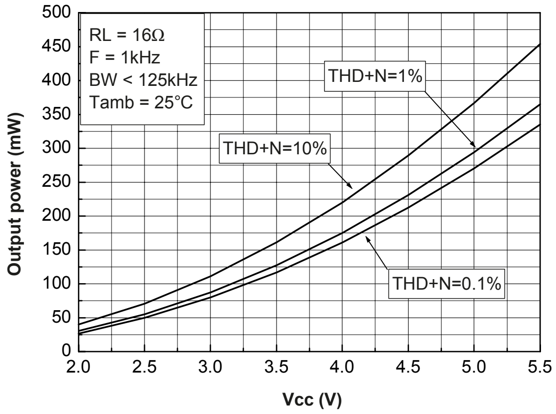


Figure 23. Output power vs. power supply voltage RL = 32 Ω

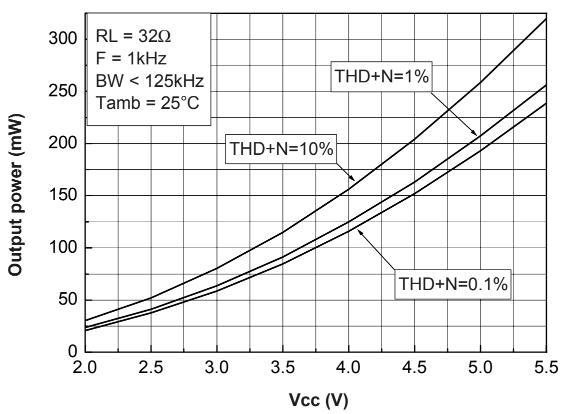


Figure 24. Output power vs. power supply voltage RL = 64 Ω

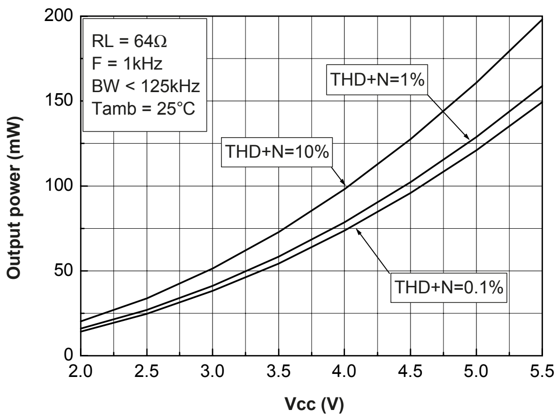


Figure 25. Output power vs. load resistor Vcc = 5 V

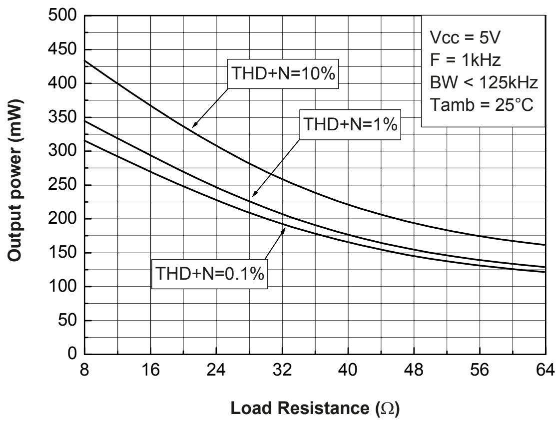


Figure 26. Output power vs. load resistor Vcc = 3.3 V

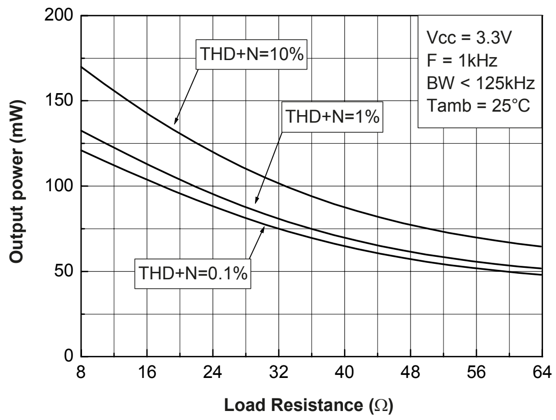


Figure 27. Output power vs. load resistor Vcc = 2.5 V

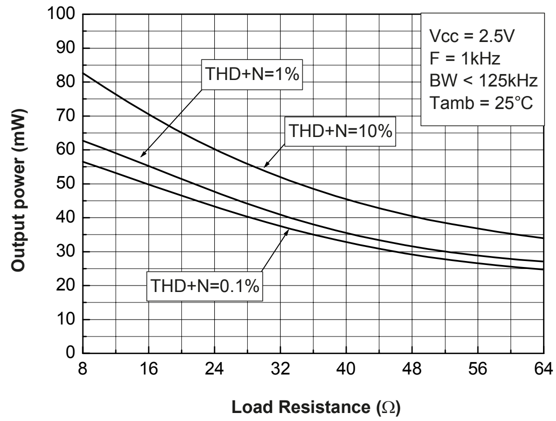


Figure 28. Output power vs. load resistor Vcc = 2 V

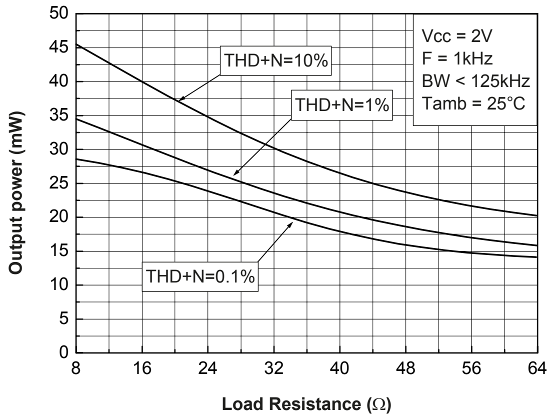


Figure 29. Power dissipation vs. output power Vcc = 5 V

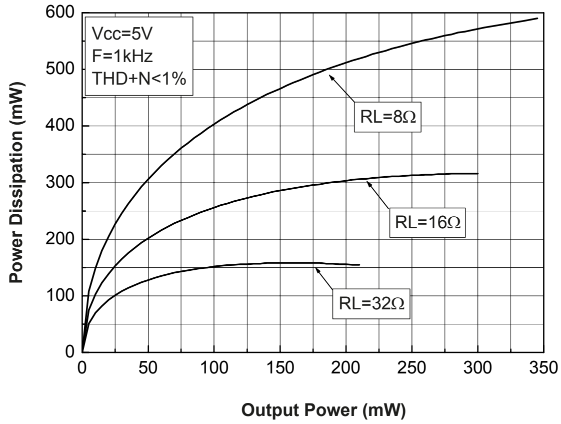


Figure 30. Power dissipation vs. output power Vcc = 3.3 V

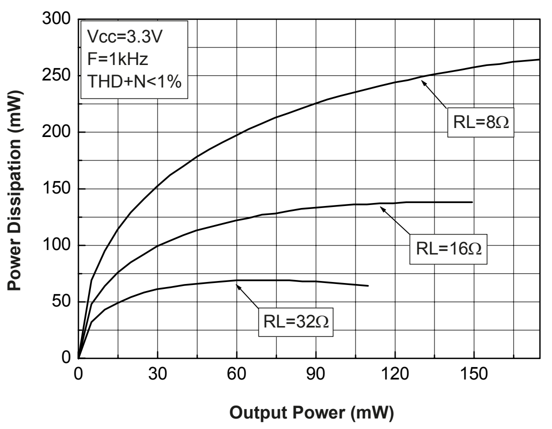


Figure 31. Power dissipation vs. output power Vcc = 2.5 V

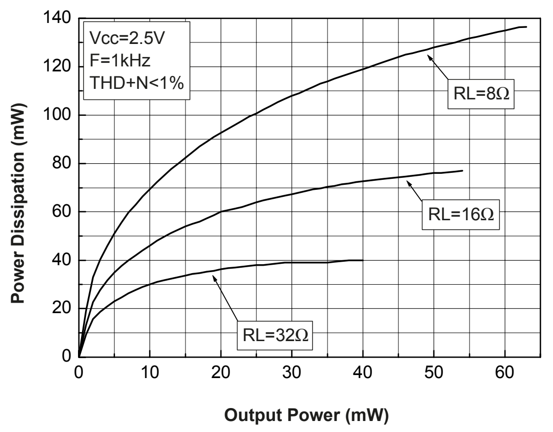


Figure 32. Power dissipation vs. output power Vcc = 2 V

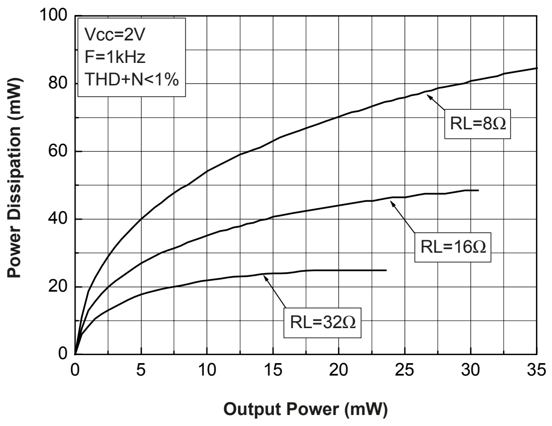


Figure 33. Power derating curves

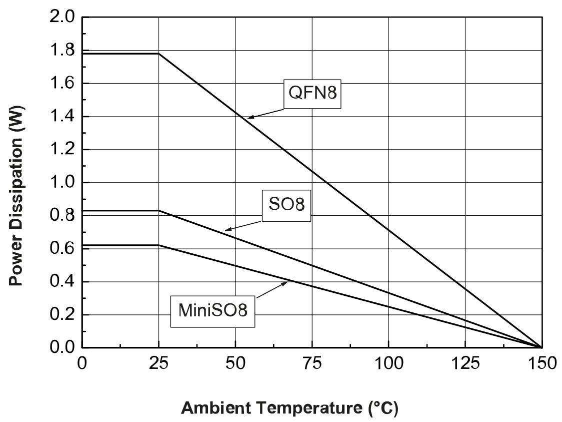


Figure 34. Output voltage swing for one Amp. vs. power supply voltage

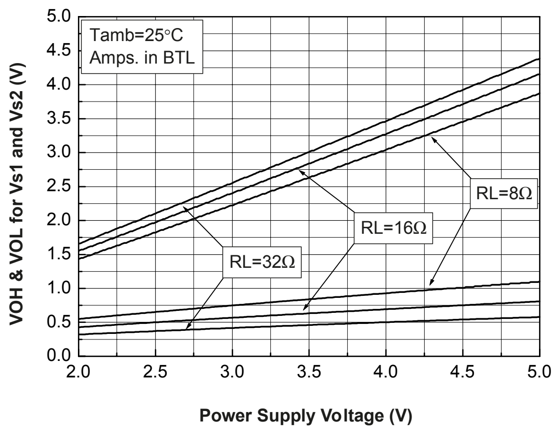


Figure 35. THD + N vs. output power RL = 8 Ω

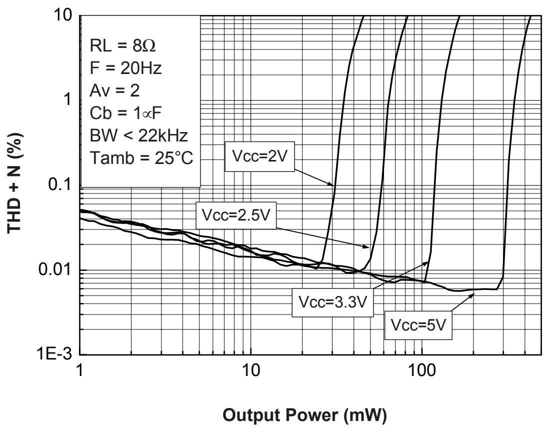


Figure 36. THD + N vs. output power RL = 16 Ω

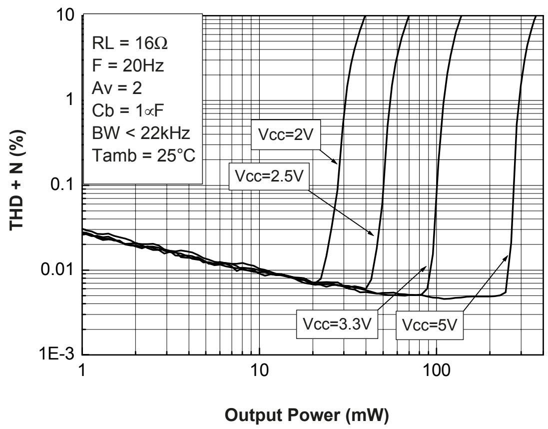


Figure 37. THD + N vs. output power RL = 32 Ω

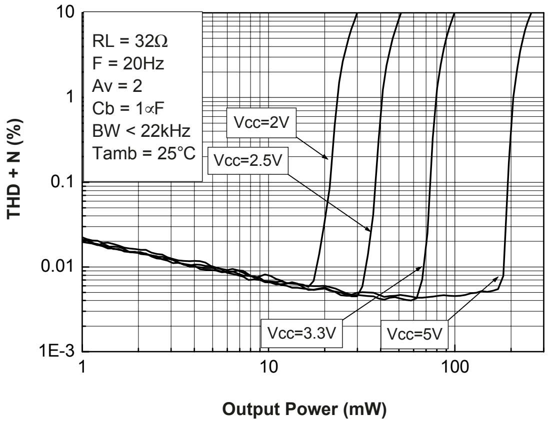


Figure 38. THD + N vs. output power RL = 8 Ω, Av = 2

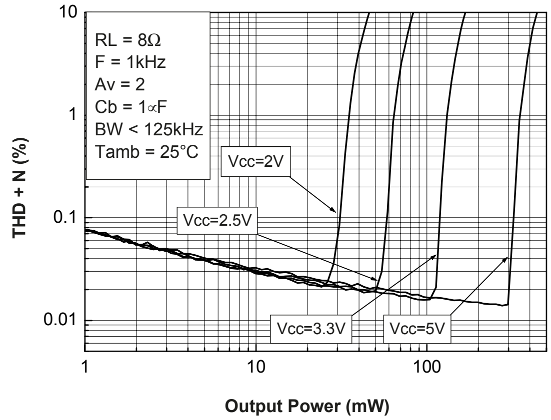


Figure 39. THD + N vs. output power RL = 16 Ω, Av = 2

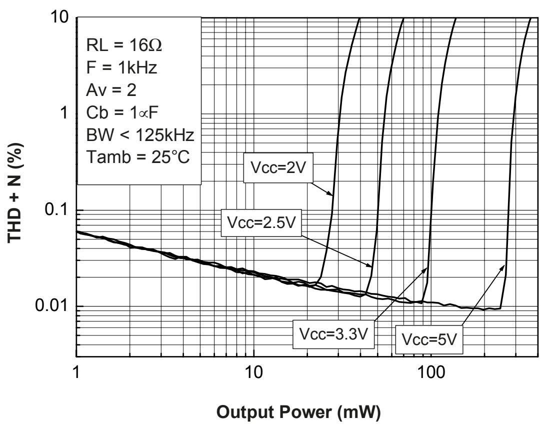


Figure 40. THD + N vs. output power RL = 32 Ω, Av = 2

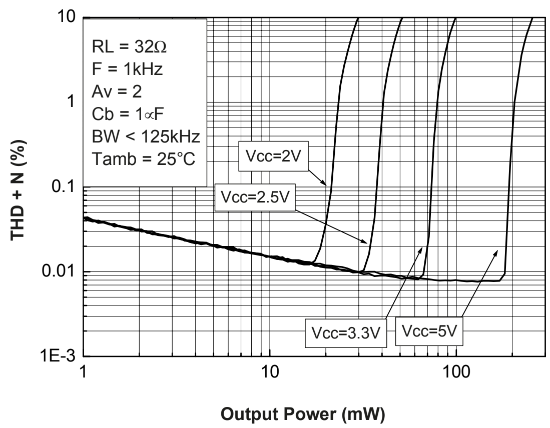


Figure 41. THD + N vs. output power RL = 8 Ω, Cb = 1 µF

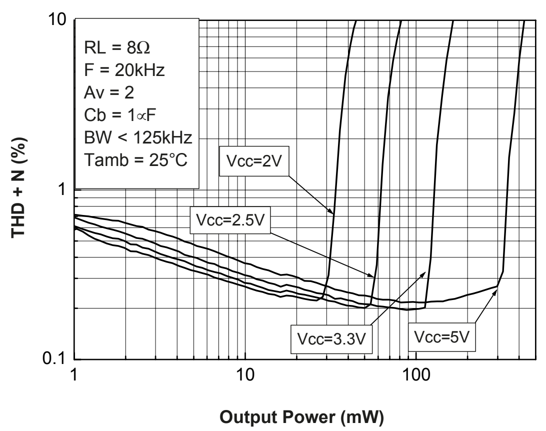


Figure 42. THD + N vs. output power RL = 16 Ω, Cb = 1 µF

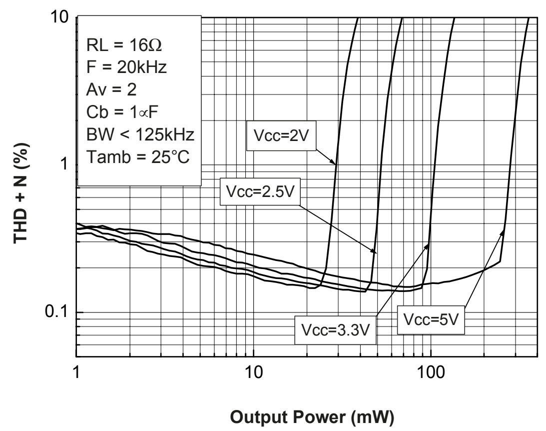


Figure 43. THD + N vs. output power RL = 32 Ω, Cb = 1 µF

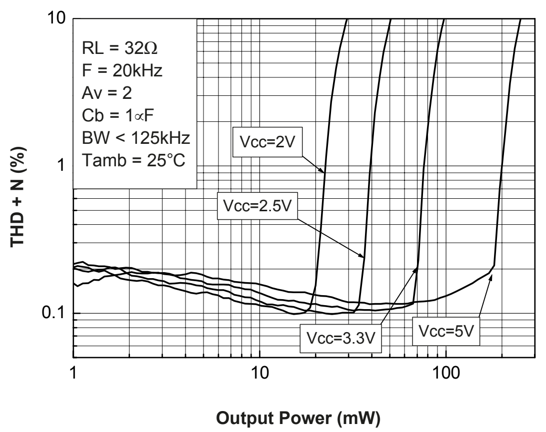


Figure 44. THD + N vs. frequency RL = 8 Ω

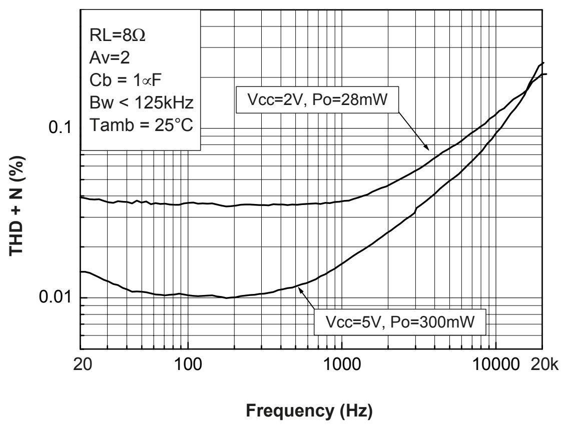


Figure 45. THD + N vs. frequency RL = 16 Ω

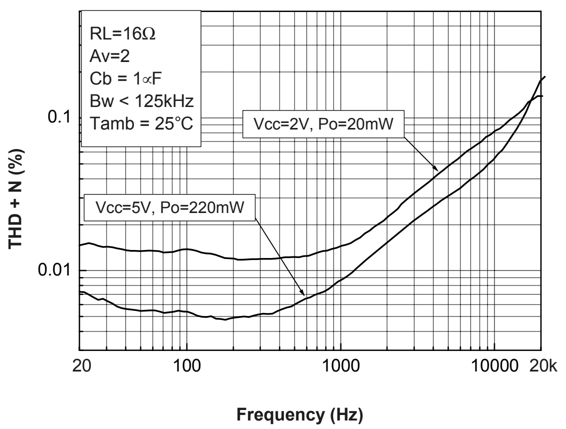


Figure 46. THD + N vs. frequency RL = 32 Ω

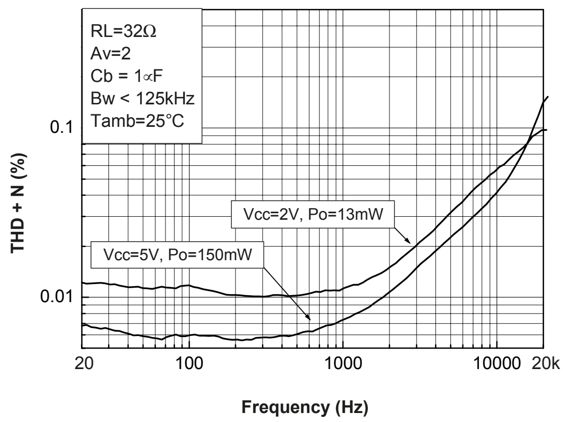


Figure 47. Signal to noise ratio vs. power supply voltage with unweighted filter (20 Hz to 20 kHz)

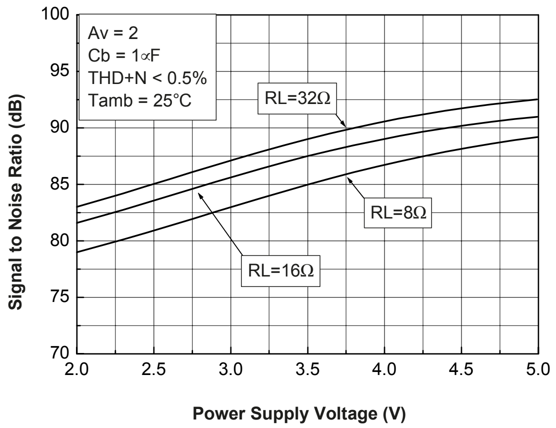


Figure 48. Signal to noise ratio vs. power supply voltage with weighted filter Type A

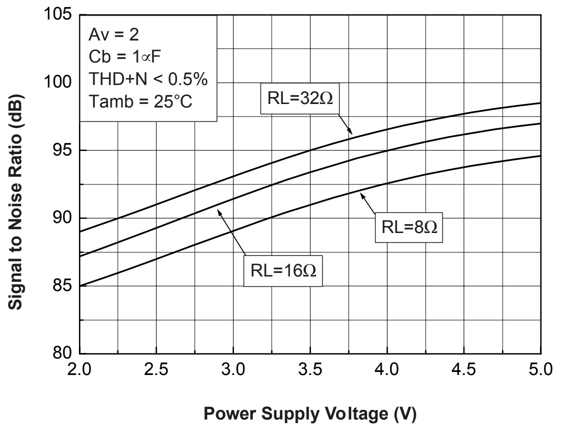


Figure 49. Noise floor Vcc = 5 V

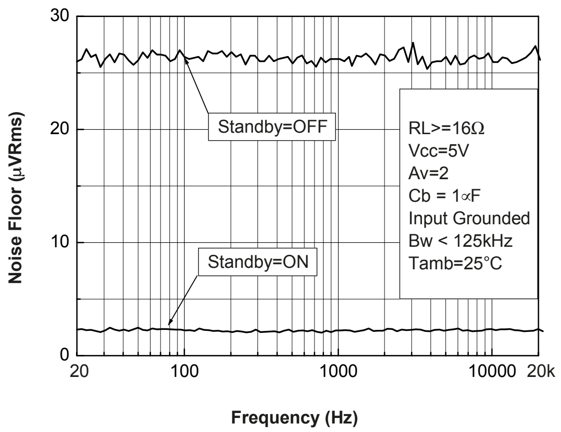


Figure 50. Noise floor Vcc = 2 V

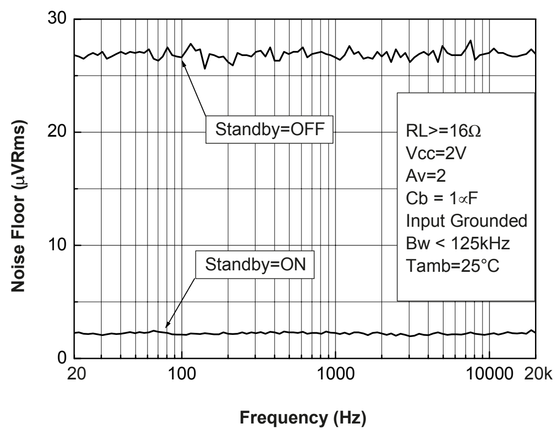


Figure 51. PSRR vs. input capacitor

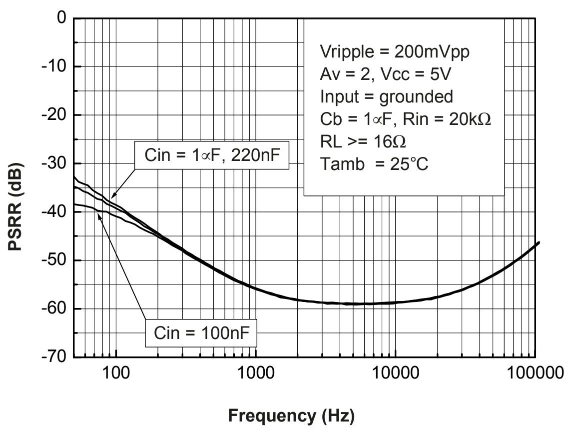


Figure 52. PSRR vs. power supply voltage

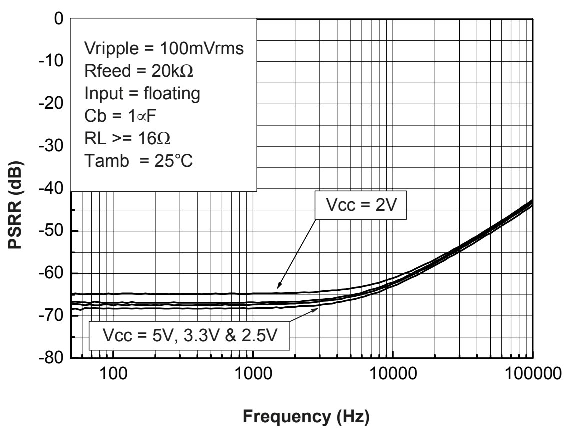


Figure 53. PSRR vs. bypass capacitor Cb = Cin = 1 µF

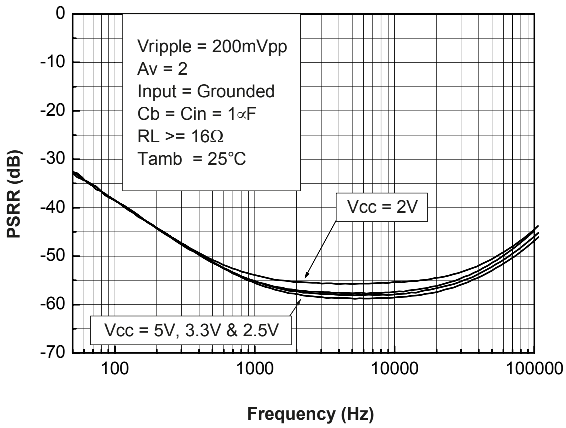


Figure 54. PSRR vs. bypass capacitor Cb = 4.7 µF

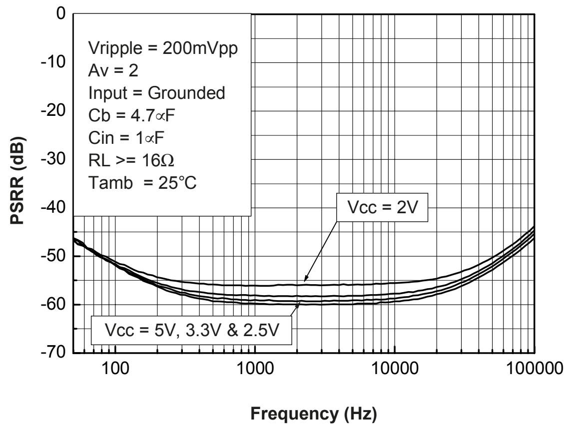


Figure 55. PSRR vs. bypass capacitor Cb = 10 µF

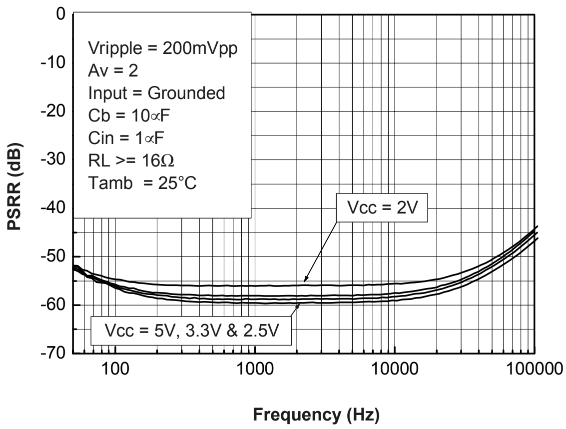


Figure 56. THD + N vs. output power RL = 8 Ω

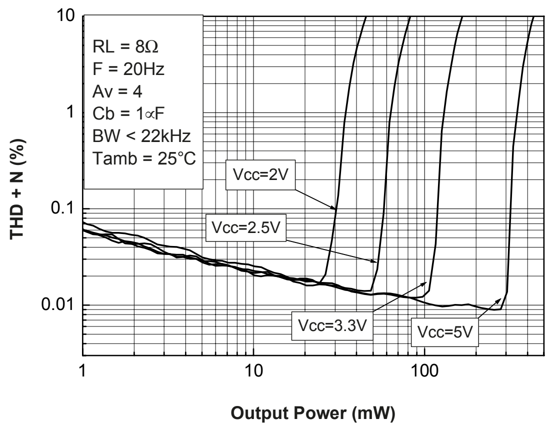


Figure 57. THD + N vs. output power RL = 16 Ω

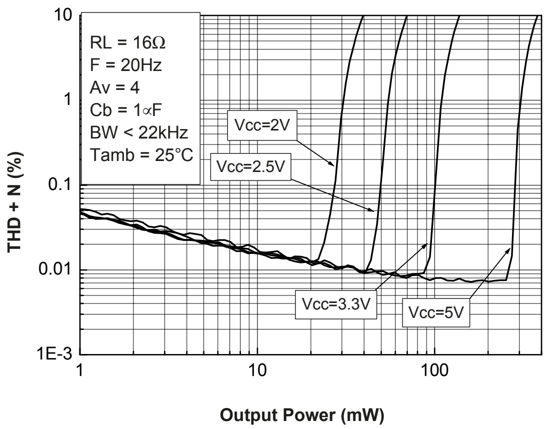


Figure 58. THD + N vs. output power RL = 32 Ω

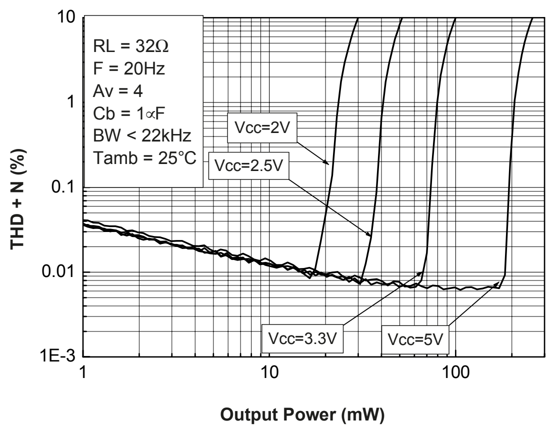


Figure 59. THD + N vs. output power RL = 8 Ω, Av = 4

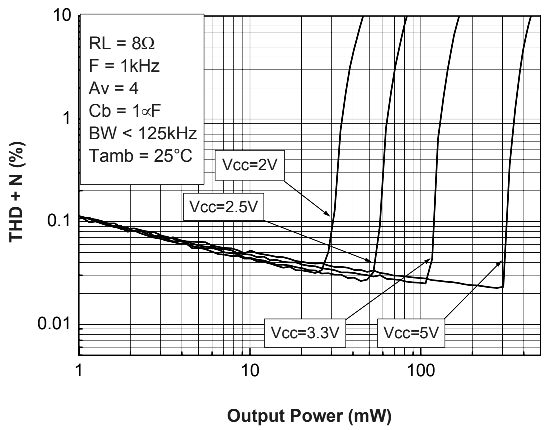


Figure 60. THD + N vs. output power RL = 16 Ω, Av = 4

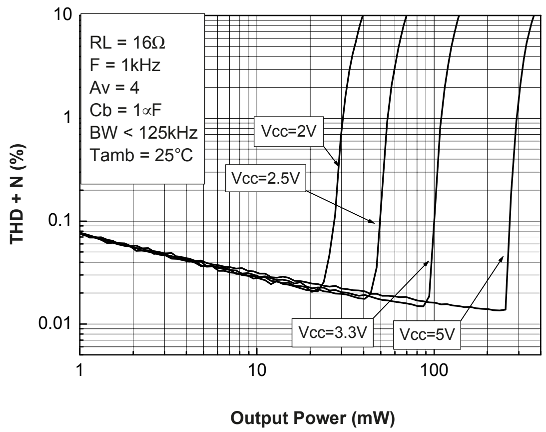


Figure 61. THD + N vs. output power RL = 32 Ω, Av = 4

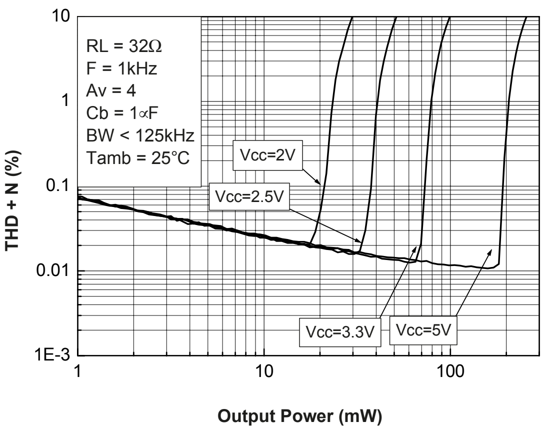


Figure 62. THD + N vs. output power RL = 8 Ω

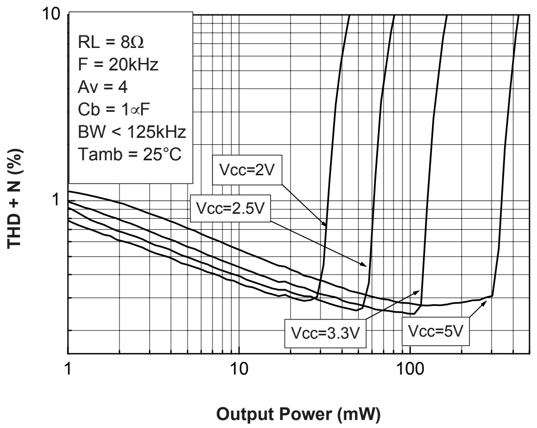


Figure 63. THD + N vs. output power RL = 16 Ω

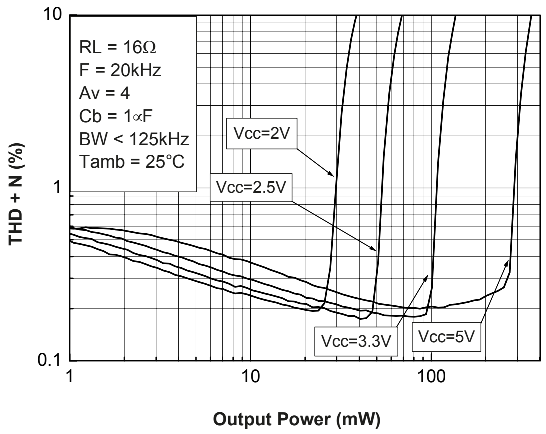


Figure 64. THD + N vs. output power RL = 32 Ω

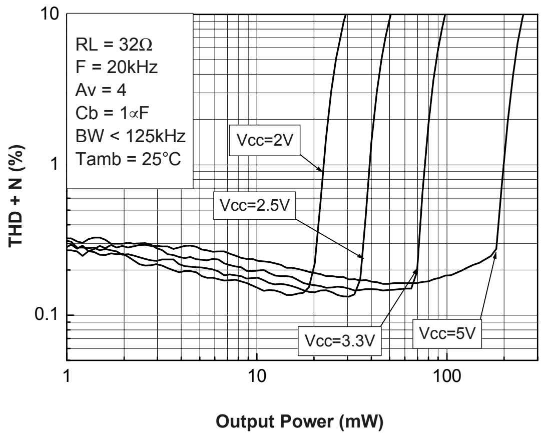


Figure 65. THD + N vs. frequency RL = 8 Ω

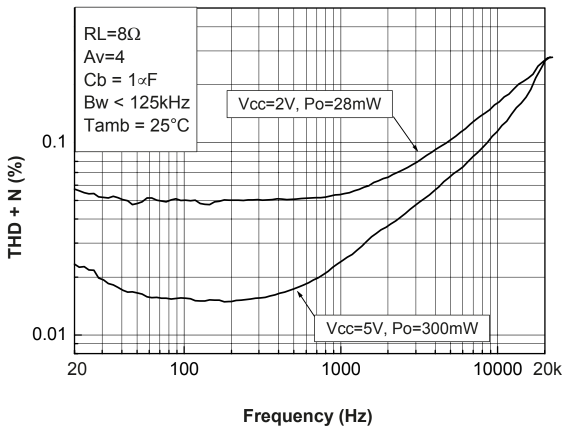


Figure 66. THD + N vs. frequency RL = 16 Ω

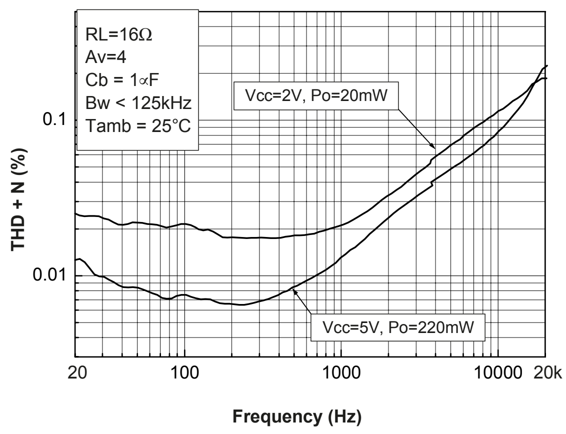


Figure 67. THD + N vs. frequency RL = 32 Ω

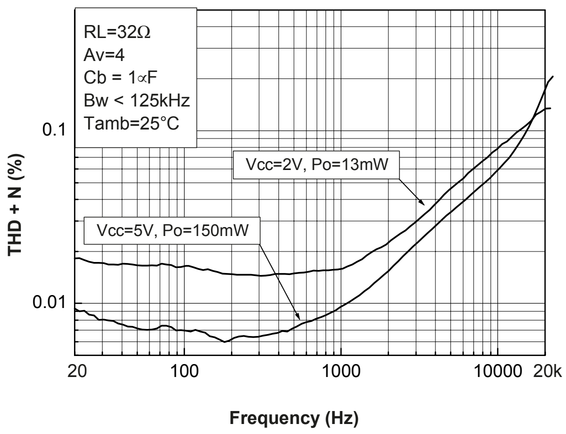


Figure 68. Signal-to-noise ratio vs. power supply voltage with unweighted filter (20 Hz to 20 kHz)

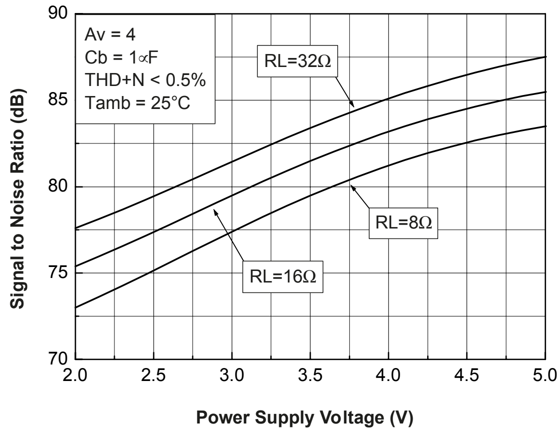


Figure 69. Signal-to-noise ratio vs power supply voltage with weighted filter Type A

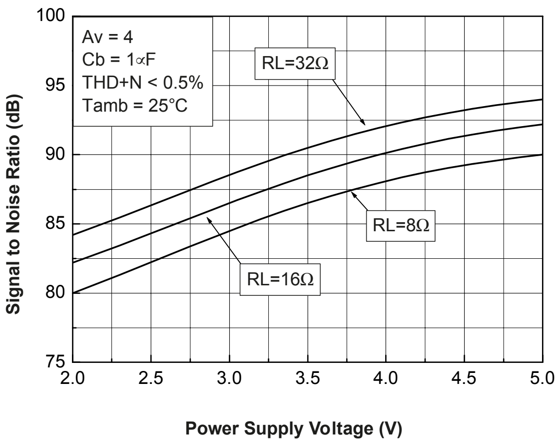


Figure 70. Noise floor Vcc = 5 V

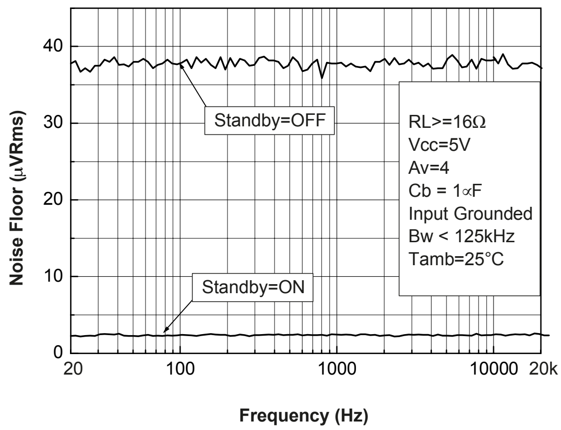


Figure 71. Noise floor Vcc = 2 V

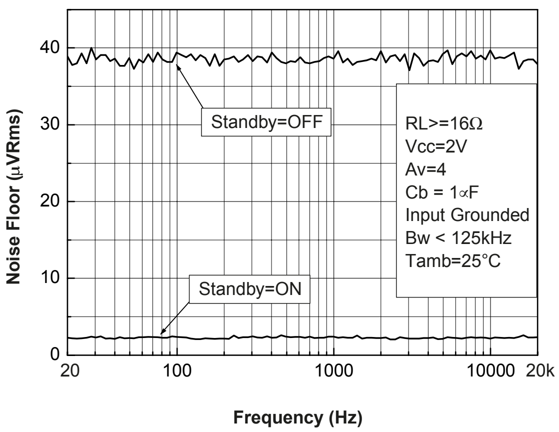


Figure 72. PSRR vs. power supply voltage

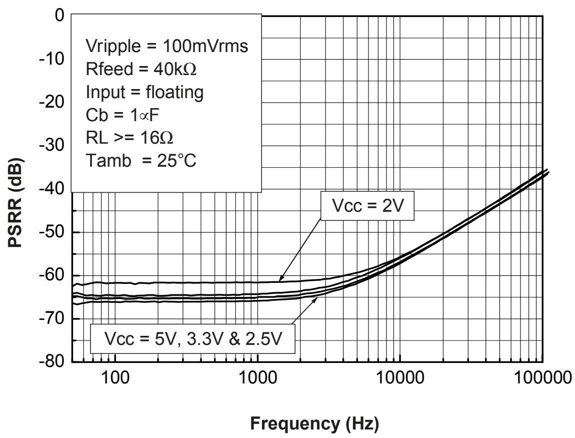


Figure 73. PSRR vs. input capacitor

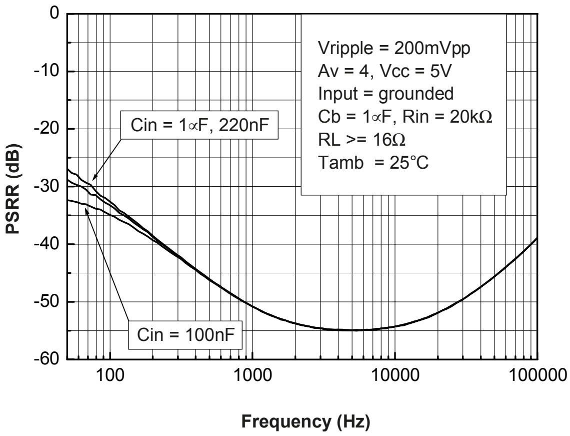


Figure 74. PSRR vs. bypass capacitor Cb = Cin = 1 µF

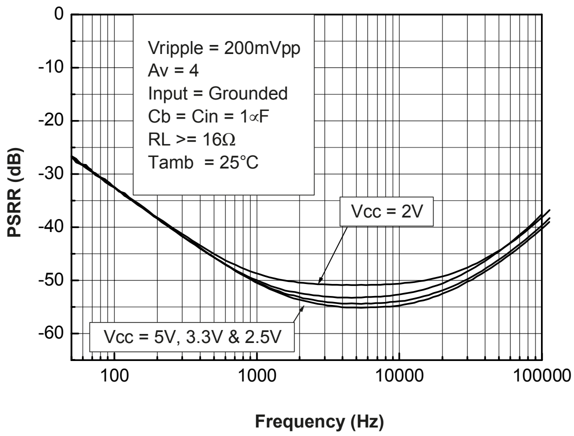


Figure 75. PSRR vs. bypass capacitor Cb = Cin = 4.7 µF

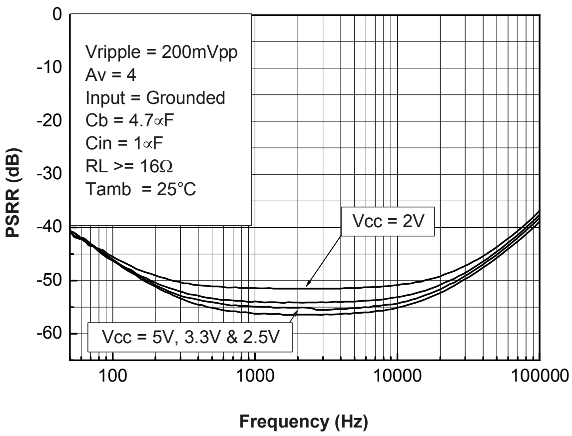


Figure 76. PSRR vs. bypass capacitor Cb = Cin = 10 µF

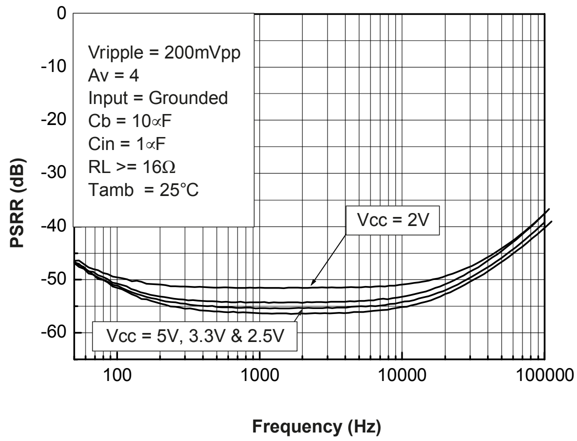


Figure 77. THD + N vs. output power RL = 8 Ω

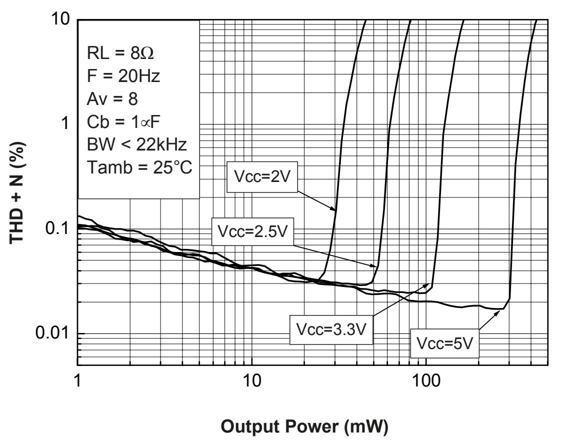


Figure 78. THD + N vs. output power RL = 16 Ω

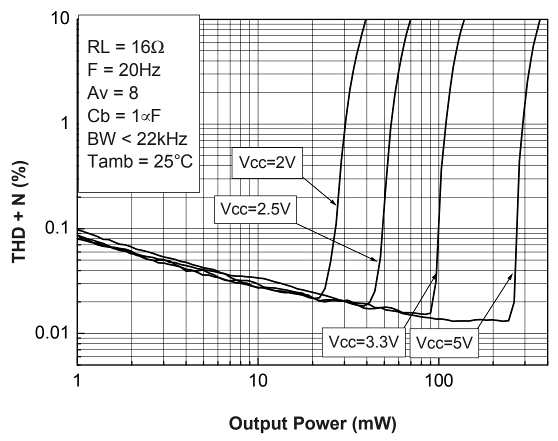


Figure 79. THD + N vs. output power RL = 32 Ω

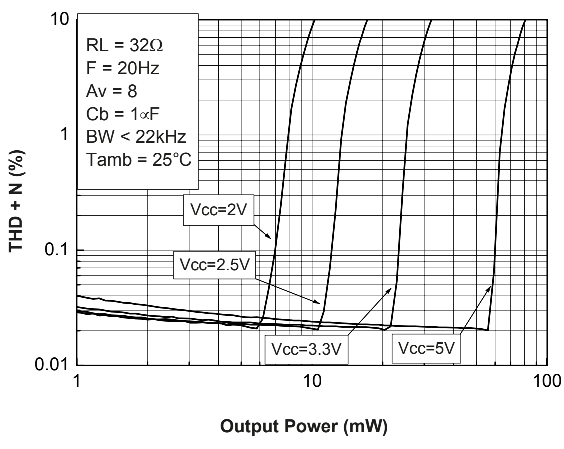


Figure 80. THD + N vs. output power RL = 8 Ω, Av = 8

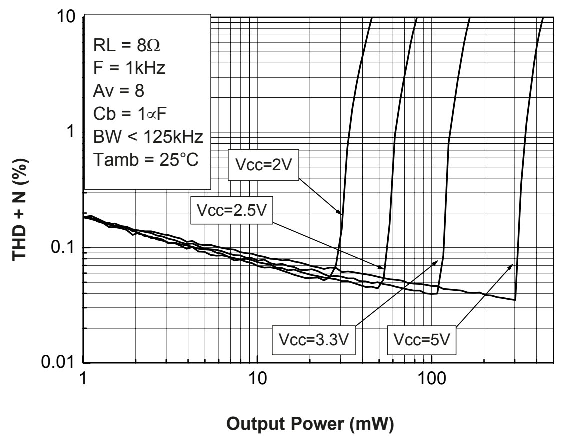


Figure 81. THD + N vs. output power RL = 16 Ω, Av = 8

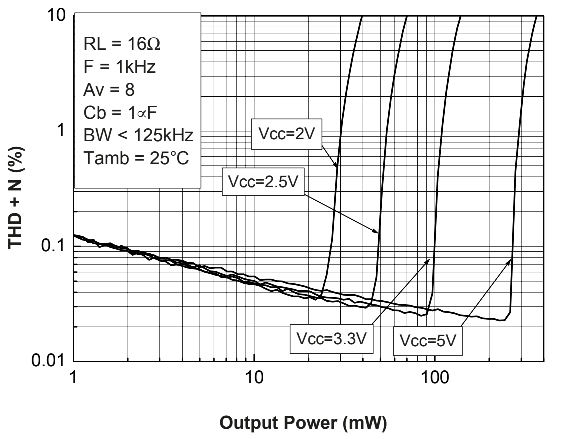


Figure 82. THD + N vs. output power RL = 32 Ω, Av = 8

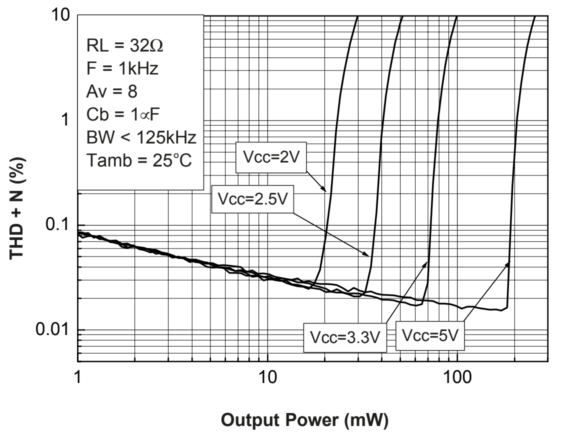


Figure 83. THD + N vs. output power RL = 8 Ω, Cb = 1 µF

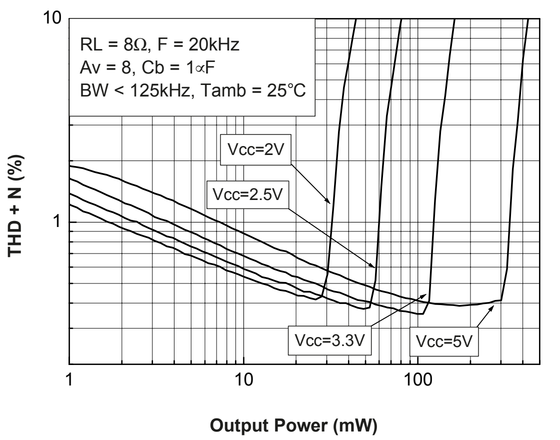


Figure 84. THD + N vs. output power RL = 16 Ω, Cb = 1 µF

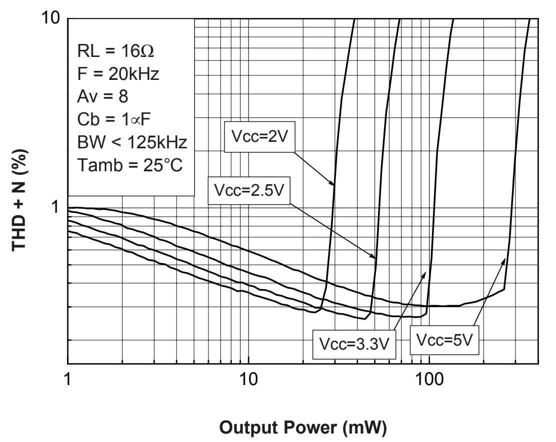


Figure 85. THD + N vs. output power RL = 32 Ω, Cb = 1 µF

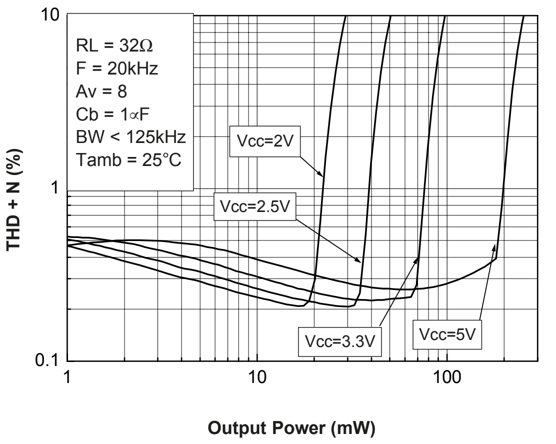


Figure 86. THD + N vs. frequency RL = 8 Ω

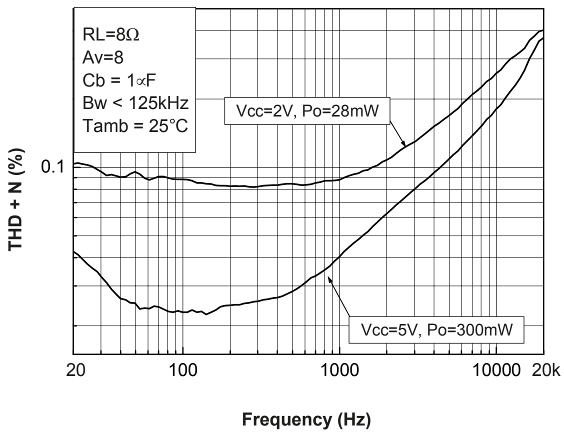


Figure 87. THD + N vs. frequency RL = 16 Ω

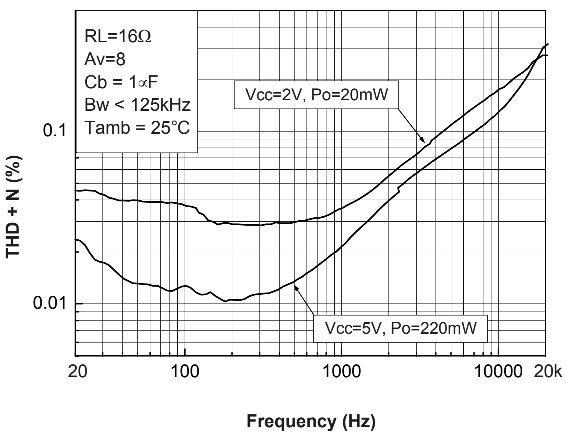


Figure 88. THD + N vs. frequency RL = 32 Ω

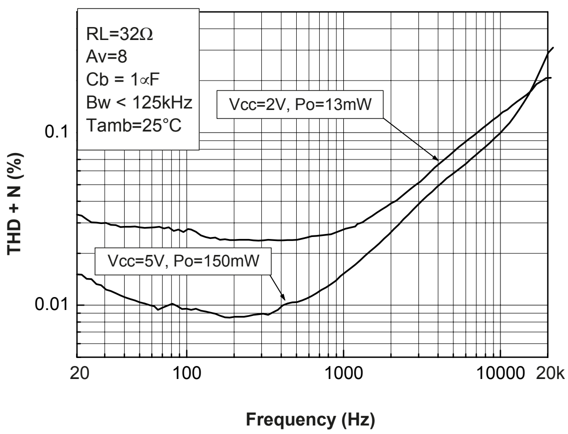


Figure 89. Signal to noise ratio vs. power supply voltage with unweighted filter (20 Hz to 20 kHz)

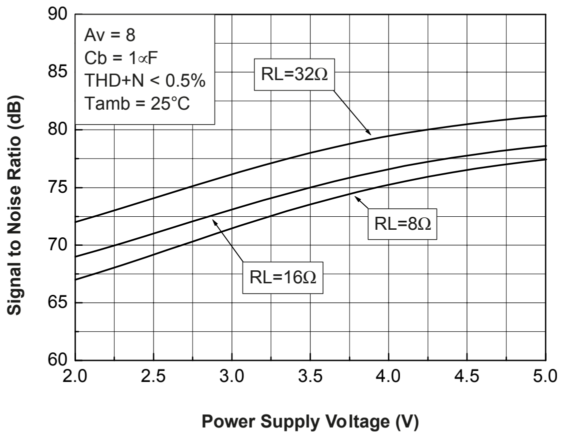


Figure 90. Signal to noise ratio vs. power supply voltage with weighted filter Type A

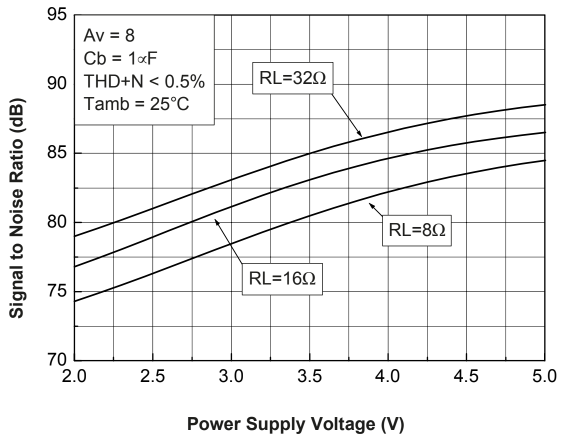


Figure 91. Noise floor Vcc = 5 V

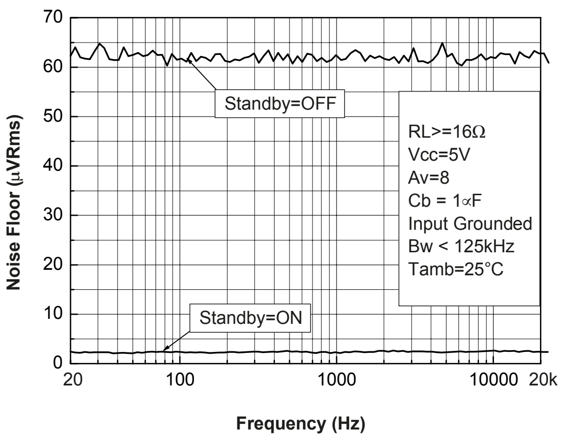


Figure 92. Noise floor Vcc = 2 V

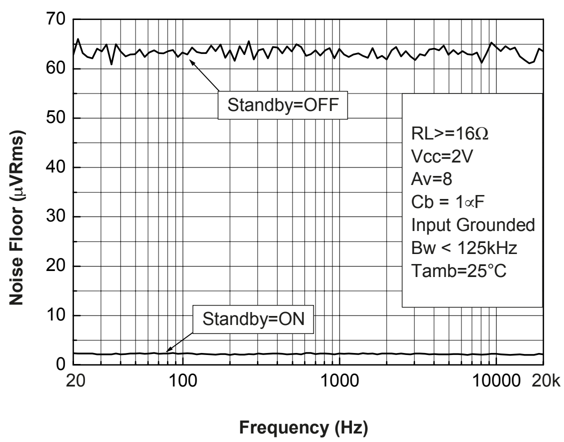


Figure 93. **PSRR vs. power supply voltage**

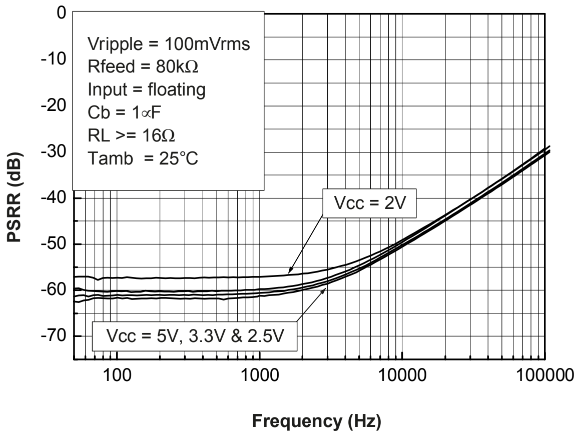


Figure 94. **PSRR vs. input capacitor**

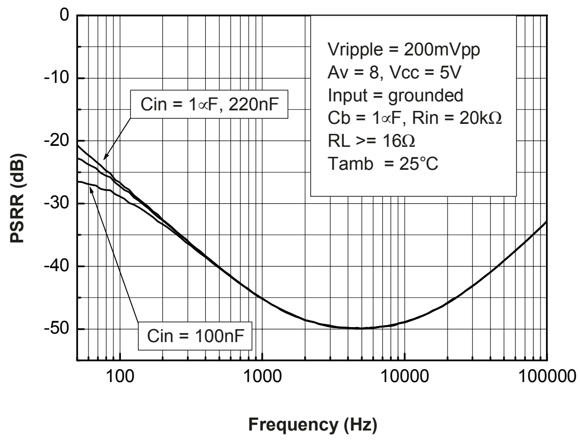


Figure 95. **PSRR vs. bypass capacitor Cb = Cin = 1 µF**

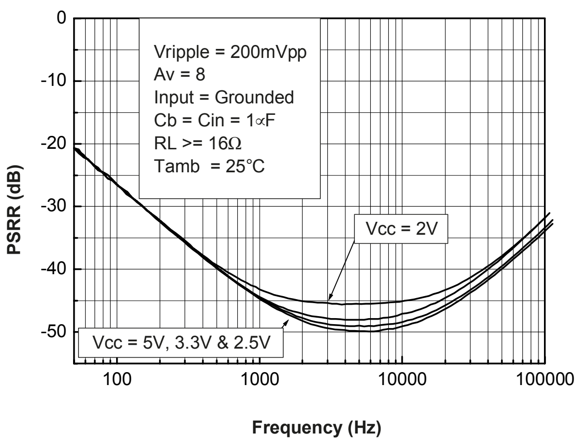


Figure 96. **PSRR vs. bypass capacitor Cb = 4.7 µF**

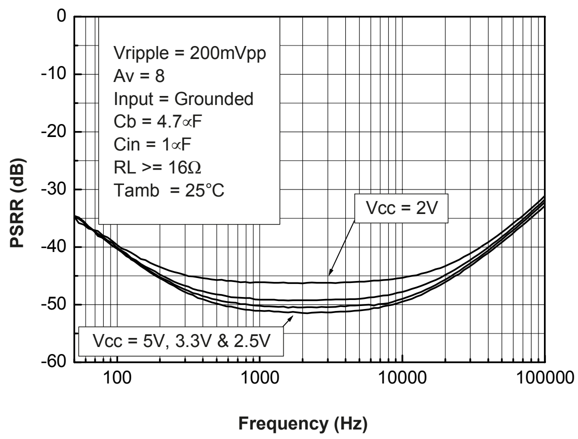
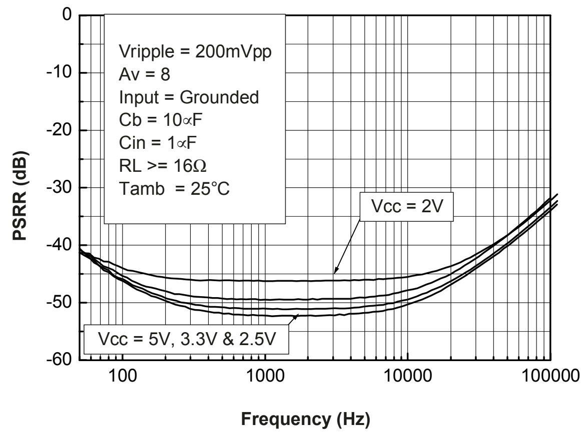


Figure 97. **PSRR vs. bypass capacitor Cb = 1 µF**



5 Application information

5.1 BTL configuration principle

The TS419 and TS421 are monolithic power amplifiers with a BTL output type. BTL (Bridge Tied Load) means that each end of the load is connected to two single-ended output amplifiers. Thus, we have:

Single ended output 1 = Vout1 = Vout (V)

Single ended output 2 = Vout2 = -Vout (V)

And Vout1 - Vout2 = 2Vout (V)

The output power is:

Pout $(2Vout_{RMS})^2 / R_L$ (W)

For the same power supply voltage, the output power in BTL configuration is four times higher than the output power in single ended configuration.

5.2 Gain in typical application schematic

In flat region (no effect of Cin), the output voltage of the first stage is:

$$Vout = -Vin\frac{Rfeed}{Rin}(V) \tag{1}$$

For the second stage : Vout2 = -Vout1 (V)

The differential output voltage is:

$$Vout2 - Vout1 = 2Vin\frac{Rfeed}{Rin}(V) \tag{2}$$

The differential gain named gain (Gv) for more convenient usage is:

$$Gv = \frac{Vout2 - Vout1}{Vin} = 2\frac{Rfeed}{Rin} \tag{3}$$

Remark : Vout2 is in phase with Vin and Vout1 is 180° phased with Vin. It means that the positive terminal of the loud speaker should be connected to Vout2 and the negative to Vout1.

5.3 Low and high frequency response

In low frequency region, the effect of Cin starts. Cin with Rin forms a high pass filter with a -3 dB cut-off frequency

$$F_{CL} = \frac{1}{2\pi RinCin}(Hz)$$

In high frequency region, you can limit the bandwidth by adding a capacitor (Cfeed) in parallel on Rfeed. Its form a low pass filter with a -3 dB cut-off frequency.

$$F_{CH} = \frac{1}{2\pi RfeedCfeed}(Hz)$$

5.4 Power dissipation and efficiency

Hypothesis:

- Voltage and current in the load are sinusoidal (Vout and Iout)
- Supply voltage is a pure DC source (Vcc)

Regarding the load we have:

$$V_{OUT} = V_{PEAK}\sin\omega t(t) \tag{4}$$

and

$$I_{OUT} = \frac{V_{OUT}}{R_L}(A) \tag{5}$$

$$P_{OUT} = \frac{V_{PEAK}{}^2}{2R_L}\left(W\right) \quad (6)$$

Then, the average current delivered by the supply voltage is:

$$Icc_{AVG} = 2\frac{V_{PEAK}}{\pi R_L}\left(A\right) \quad (7)$$

The power delivered by the supply voltage is Psupply = Vcc Icc_{AVG} (W)

Then, the power dissipated by the amplifier is Pdiss = Psupply - Pout (W)

$$Pdiss = \frac{2\sqrt{2Vcc}}{\pi\sqrt{R_L}}\sqrt{P_{OUT}} - P_{OUT}\left(W\right) \quad (8)$$

and the maximum value is obtained when:

$$\frac{\partial Pdiss}{\partial P_{OUT}} = 0 \quad (9)$$

and its value is:

$$Pdissmax = \frac{2V_{CC}{}^2}{\pi^2 R_L}\left(W\right) \quad (10)$$

Remark : This maximum value is only depending on power supply voltage and load values.

The efficiency is the ratio between the output power and the power supply

$$\eta = \frac{P_{OUT}}{P_{supply}} = \frac{\pi V_{PEAK}}{4V_{CC}} \quad (11)$$

The maximum theoretical value is reached when

Vpeak = Vcc, so

$$\frac{\pi}{4} = 78.5\,\% \quad (12)$$

5.5 Decoupling of the circuit

Two capacitors are needed to bypass properly the TS419/TS421. A power supply bypass capacitor C_S and a bias voltage bypass capacitor C_B.

C_S has particular influence on the THD+N in the high frequency region (above 7 kHz) and an indirect influence on power supply disturbances.

With 1 µF, you can expect similar THD+N performances to those shown in the datasheet.

In the high frequency region, if C_S is lower than 1 µF, it increases THD+N and disturbances on the power supply rail are less filtered.

On the other hand, if C_S is higher than 1 µF, those disturbances on the power supply rail are more filtered.

C_B has an influence on THD+N at lower frequencies, but its function is critical to the final result of PSRR (with input grounded and in the lower frequency region).

If C_B is lower than 1 µF, THD+N increases at lower frequencies and PSRR worsens.

If C_B is higher than 1 µF, the benefit on THD+N at lower frequencies is small, but the benefit to PSRR is substantial.

Note: that C_{IN} has a non-negligible effect on PSRR at lower frequencies. The lower the value of C_{IN}, the higher the PSRR.

5.6 Wake-up time: T_{WU}

When standby is released to put the device ON, the bypass capacitor C_B will not be charged immediatly. As C_B is directly linked to the bias of the amplifier, the bias will not work properly until the C_B voltage is correct. The time to reach this voltage is called wake-up time or T_{WU} and typically equal to:

T_{WU} = 0.15xC_B (s) with C_B in µF.

Due to process tolerances, the range of the wake-up time is:

$0.12xCb < T_{WU} < 0.18xC_B$ (s) with C_B in µF

Note: When the standby command is set, the time to put the device in shutdown mode is a few microseconds.

5.7 Pop performance

Pop performance is intimately linked with the size of the input capacitor Cin and the bias voltage bypass capacitor C_B.

The size of C_{IN} is dependent on the lower cut-off frequency and PSRR values requested. The size of C_B is dependent on THD+N and PSRR values requested at lower frequencies.

Moreover, C_B determines the speed with which the amplifier turns ON. The slower the speed is, the softer the turn ON noise is.

The charge time of C_B is directly proportional to the internal generator resistance 150 kΩ.

Then, the charge time constant for C_B is

$\tau_B = 150\ k\Omega \times C_B$ (s)

As C_B is directly connected to the non-inverting input (pin 2 & 3) and if we want to minimize, in amplitude and duration, the output spike on Vout1 (pin 5), C_{IN} must be charged faster than C_B. The equivalent charge time constant of C_{IN} is:

$\tau_{IN} = (Rin + Rfeed) \times C_{IN}$ (s)

Thus we have the relation:

$\tau_{IN} < \tau_B$ (s)

Proper respect of this relation allows to minimize the pop noise.

Remark : Minimizing C_{IN} and C_B benefits both the pop phenomena, and the cost and size of the application.

5.8 Application : Differential inputs BTL power amplifier

The schematic on figure 98, shows how to design the TS419/21 to work in a differential input mode.

The gain of the amplifier is:

$$G_{VDIFF} = 2\frac{R_2}{R_1} \tag{13}$$

In order to reach optimal performances of the differential function, R_1 and R_2 should be matched at 1% max.

Figure 98. Differential input amplifier configuration

Input capacitance C can be calculated by the following formula using the -3 dB lower frequency required. (F_L is the lower frequency required).

$$C \approx \frac{1}{2\pi R_1 F_L}(F) \tag{14}$$

Note : This formula is true only if:

$$F_{CB} = \frac{1}{942000 \times C_B}(Hz) \tag{15}$$

is ten times lower than F_L.

The following bill of material is an example of a differential amplifier with a gain of 2 and a -3 dB lower cuttoff frequency of about 80 Hz.

Table 8. Components

Designator	Part type
R1	20 k / 1%
R2	20 k / 1%
C	100 nF
$C_B = C_S$	1 µF
U1	TS419/21

6 Package information

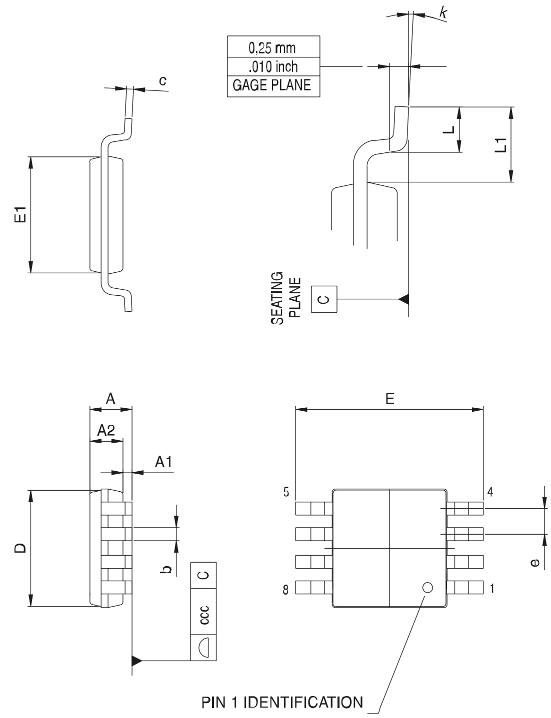
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 MiniSO-8 mechanical data

Table 9. MiniSO-8 mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0.05	0.10	0.15	0.002	0.004	0.005
A2	0.78	0.86	0.94	0.031	0.031	0.037
b	0.25	0.33	0.4Q	0.010	0.13	0.013
c	0.13	0.16	0.23	0.005	0.007	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.75	4.90	5.05	0.187	0.193	0.199
E1	2.90	3.00	3.10	0.114	0.118	0.122
e		0.65			0.026	
K	0°		6°	0°		6°
L	0.40	0.55	0.70	0.016	0.022	0.028
L1			0.10			0.004

Figure 99. MiniSO-8 drawing

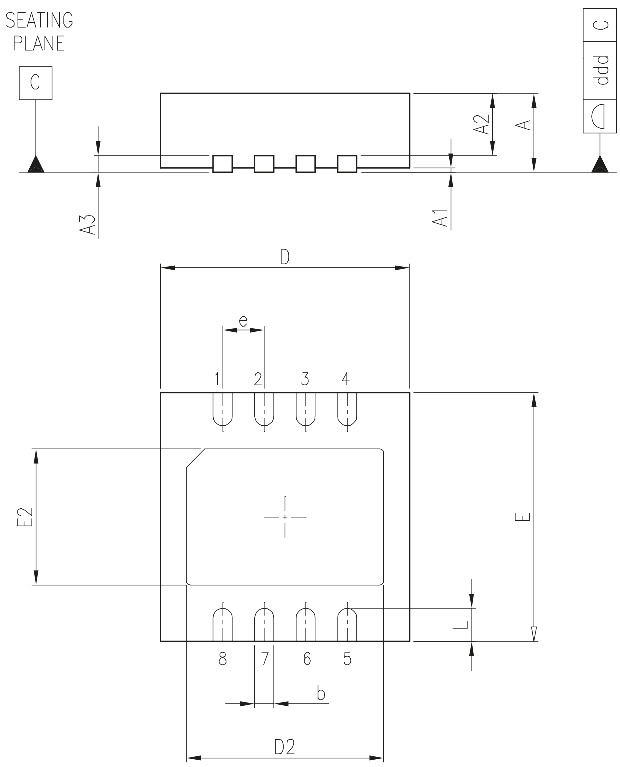


6.2 DFN8 (3x3) mechanical data

Table 10. DFN8 (3x3) mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80	0.90	1.00	31.5	35.4	39.4
A1		0.02	0.05		0.8	2.0
A2		0.70			27.6	
A3		0.20			7.9	
b	0.18	0.23	0.30	7.1	9.1	11.8
D		3.00			118.1	
D2	2.23	2.38	2.48	87.8	93.7	97.7
E		3.00			118.1	
E2	1.49	1.64	1.74	58.7	64.6	68.5
e		0.50			19.7	
L	0.30	0.40	0.50	11.8	15.7	19.7

Figure 100. DFN8 (3x3) drawing



7 Ordering information

Table 11. Order codes

Order code	Temperature range	Package	Packing	Marking
TS419IST	-40°C to 85°C	miniSO8	Tape and reel	K19A
TS421IQT		DFN8		K21A

Revision history

Table 12. **Document revision history**

Date	Revision	Changes
06-Feb-2013	4	No history because of migration.
29-May-2019	5	Removed the part numbers TS419IDT, TS421IDT and all its reference throughout the document.

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