TS912, TS912A, TS912B

Rail-to-rail CMOS dual operational amplifier

Datasheet — production data

Features

- Rail-to-rail input and output voltage ranges
- Single (or dual) supply operation from 2.7 to 16 V
- Extremely low input bias current: 1 pA typ.
- Low input offset voltage: 2 mV max.
- Specified for 600 Ω and 100 Ω loads
- Low supply current: 200 µA/amplifier (V_{CC} = 3 V)
- Latch-up immunity
- ESD tolerance: 3 kV
- Spice macromodel included in this specification

Related products

- See TS56x series for better accuracy and smaller packages

Description

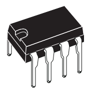
The TS912 device is a rail-to-rail CMOS dual operational amplifier designed to operate with a single or dual supply voltage.

The input voltage range V_{icm} includes the two supply rails V_{CC}^+ and V_{CC}^-.

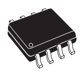
The output reaches V_{CC}^- +30 mV, V_{CC}^+ -40 mV, with R_L = 10 kΩ and V_{CC}^- +300 mV, V_{CC}^+ -400 mV, with R_L = 600 Ω.

This product offers a broad supply voltage operating range from 2.7 to 16 V and a supply current of only 200 µA/amp. (V_{CC} = 3 V).

Source and sink output current capability is typically 40 mA (at V_{CC} = 3 V), fixed by an internal limitation circuit.

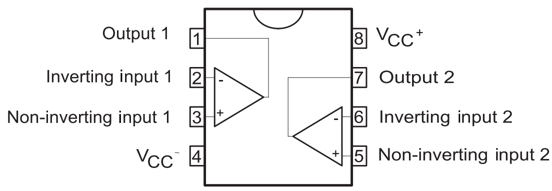


N
DIP8
(plastic package)



D
SO-8
(plastic micropackage)

Pin connections (top view)



Contents

1 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage(1)	18	V
V_{id}	Differential input voltage(2)	±18	V
V_i	Input voltage(3)	-0.3 to 18	V
I_{in}	Current on inputs	±50	mA
I_o	Current on outputs	±130	mA
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
R_{thja}	Thermal resistance junction-to-ambient(4) DIP8 SO-8	 85 125	°C/W
R_{thjc}	Thermal resistance junction to case(4) DIP8 SO-8	 41 40	°C/W
ESD	HBM: human body model(5)	3	kV
	MM: machine model(6)	200	V
	CDM: charged device model(7)	1500	V

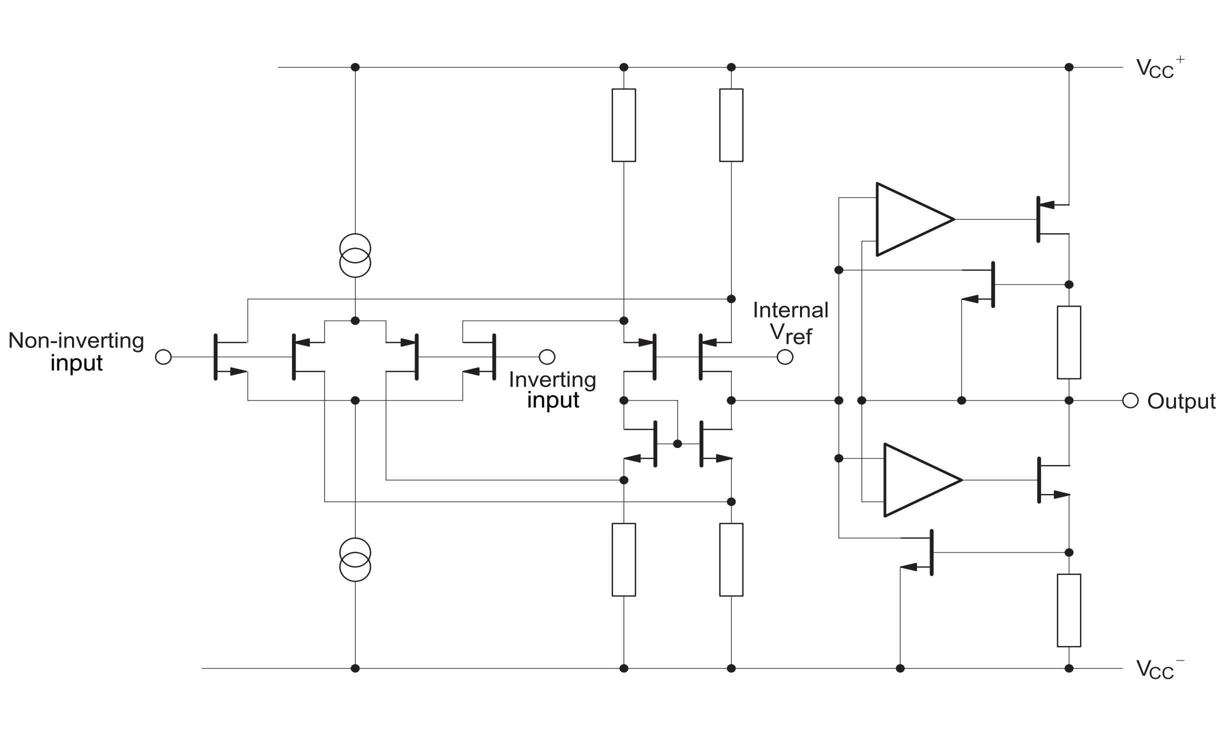
1. All voltage values, except differential voltage are with respect to network ground terminal.
2. Differential voltages are non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of input and output voltages must never exceed V_{CC}^+ +0.3 V.
4. Short-circuits can cause excessive heating. Destructive dissipation can result from simultaneous short-circuits on all amplifiers. These values are typical.
5. Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
6. Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.
7. Charged device model: all pins and the package are charged together to the specified voltage and then discharged directly to ground through only one pin. This is done for all pins.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.7 to 16	V
V_{icm}	Common mode input voltage range	V_{CC-}-0.2 to V_{CC+}+0.2	V
T_{oper}	Operating free air temperature range	-40 to + 125	°C

2 Schematic diagram

Figure 1. Schematic diagram (1/2 TS912)



3 Electrical characteristics

Table 3. V_{CC+} = 3 V, V_{CC-} = 0 V, R_L, C_L connected to $V_{CC}/2$, T_{amb} = 25 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage ($V_{ic} = V_o = V_{CC}/2$) TS912 TS912A TS912B $T_{min} \leq T_{amb} \leq T_{max}$ TS912 TS912A TS912B			 10 5 2 12 7 3	mV
ΔV_{io}	Input offset voltage drift		5		µV/°C
I_{io}	Input offset current(1) $T_{min} \leq T_{amb} \leq T_{max}$		1	100 200	pA
I_{ib}	Input bias current(1) $T_{min} \leq T_{amb} \leq T_{max}$		1	150 300	pA
I_{CC}	Supply current (per amplifier, A_{VCL} = 1, no load) $T_{min} \leq T_{amb} \leq T_{max}$		200	300 400	µA
CMR	Common mode rejection ratio V_{ic} = 0 to 3 V, V_o = 1.5 V		70		dB
SVR	Supply voltage rejection ratio (V_{CC}^+ = 2.7 to 3.3 V, $V_o = V_{CC}/2$)	50	80		dB
A_{vd}	Large signal voltage gain (R_L = 10 kΩ, V_o = 1.2 V to 1.8 V) $T_{min} \leq T_{amb} \leq T_{max}$	3 2	10		V/mV
V_{OH}	High level output voltage (V_{id} = 1 V) R_L = 100 kΩ R_L = 10 kΩ R_L = 600 Ω R_L = 100 Ω $T_{min} \leq T_{amb} \leq T_{max}$ R_L = 10 kΩ R_L = 600 Ω	 2.95 2.9 2.3 2.8 2.1	 2.96 2.6 2		V
V_{OL}	Low level output voltage (V_{id} = -1 V) R_L = 100 kΩ R_L = 10 kΩ R_L = 600 Ω R_L = 100 Ω $T_{min} \leq T_{amb} \leq T_{max}$ R_L = 10 kΩ R_L = 600 Ω		 30 300 900	 50 70 400 100 600	mV
I_o	Output short-circuit current (V_{id} = ±1 V) Source ($V_o = V_{CC-}$) Sink ($V_o = V_{CC+}$)	 20 20	 40 40		mA
GBP	Gain bandwidth product (A_{VCL} = 100, R_L = 10 kΩ, C_L = 100 pF, f = 100 kHz)		0.8		MHz

Table 3. V_{CC+} = 3 V, V_{CC-} = 0 V, R_L, C_L connected to $V_{CC}/2$, T_{amb} = 25 °C (unless otherwise specified) (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SR^+	Slew rate (A_{VCL} = 1, R_L = 10 kΩ, C_L = 100 pF, V_i = 1.3 V to 1.7 V)		0.4		V/µs
SR^-	Slew rate (A_{VCL} = 1, R_L = 10 kΩ, C_L = 100 pF, V_i = 1.3 V to 1.7 V)		0.3		V/µs
ϕm	Phase margin		30		Degrees
en	Equivalent input noise voltage (R_s = 100 Ω, f = 1 kHz)		30		nV/√Hz

1. Maximum values include unavoidable inaccuracies of the industrial tests.

Table 4. V_{CC+} = 5 V, V_{CC-} = 0 V, R_L, C_L connected to $V_{CC}/2$, T_{amb} = 25 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage ($V_{ic} = V_o = V_{CC}/2$) TS912 TS912A TS912B $T_{min} \leq T_{amb} \leq T_{max}$ TS912 TS912A TS912B			 10 5 2 12 7 3	mV
ΔV_{io}	Input offset voltage drift		5		µV/°C
I_{io}	Input offset current(1) $T_{min} \leq T_{amb} \leq T_{max}$		1	100 200	pA
I_{ib}	Input bias current(1) $T_{min} \leq T_{amb} \leq T_{max}$		1	150 300	pA
I_{CC}	Supply current (per amplifier, A_{VCL} = 1, no load) $T_{min} \leq T_{amb} \leq T_{max}$		230	350 450	µA
CMR	Common mode rejection ratio V_{ic} = 1.5 to 3.5 V, V_o = 2.5 V	60	85		dB
SVR	Supply voltage rejection ratio (V_{CC+} = 3 to 5 V, $V_o = V_{CC}/2$)	55	80		dB
A_{vd}	Large signal voltage gain (R_L = 10 kΩ, V_o = 1.5 V to 3.5 V) $T_{min} \leq T_{amb} \leq T_{max}$	10 7	40		V/mV
V_{OH}	High level output voltage (V_{id} = 1 V) R_L = 100 kΩ R_L = 10 kΩ R_L = 600 Ω R_L = 100 Ω $T_{min} \leq T_{amb} \leq T_{max}$ R_L = 10 kΩ R_L = 600 Ω	 4.95 4.9 4.25 4.8 4.1	 4.95 4.55 3.7		V
V_{OL}	Low level output voltage (V_{id} = -1 V) R_L = 100 kΩ R_L = 10 kΩ R_L = 600 Ω R_L = 100 Ω $T_{min} \leq T_{amb} \leq T_{max}$ R_L = 10 kΩ R_L = 600 Ω		 40 350 1400	 50 100 500 150 750	mV
I_o	Output short-circuit current (V_{id} = ±1 V) Source ($V_o = V_{CC-}$) Sink ($V_o = V_{CC+}$)	 45 45	 65 65		mA
GBP	Gain bandwidth product (A_{VCL} = 100, R_L = 10 kΩ, C_L = 100 pF, f = 100 kHz)		1		MHz
SR^+	Slew rate (A_{VCL} = 1, R_L = 10 kΩ, C_L = 100 pF, V_i = 1 V to 4 V)		0.8		V/µs
SR^-	Slew rate (A_{VCL} = 1, R_L = 10 kΩ, C_L = 100 pF, V_i = 1 V to 4 V)		0.6		V/µs

Table 4. V_{CC+} = 5 V, V_{CC-} = 0 V, R_L, C_L connected to $V_{CC}/2$, T_{amb} = 25 °C (unless otherwise specified) (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
en	Equivalent input noise voltage (R_s = 100 Ω, f = 1 kHz)		30		nV/√Hz
V_{O1}/V_{O2}	Channel separation (f = 1 kHz)		120		dB
ϕm	Phase margin		30		Degrees

1. Maximum values include unavoidable inaccuracies of the industrial tests.

Table 5. V_{CC+} = 10 V, V_{CC-} = 0 V, R_L, C_L connected to $V_{CC}/2$, T_{amb} = 25 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage ($V_{ic} = V_o = V_{CC}/2$) TS912 TS912A TS912B $T_{min} \leq T_{amb} \leq T_{max}$ TS912 TS912A TS912B			 10 5 2 12 7 3	mV
ΔV_{io}	Input offset voltage drift		5		µV/°C
I_{io}	Input offset current(1) $T_{min} \leq T_{amb} \leq T_{max}$		1	100 200	pA
I_{ib}	Input bias current(1) $T_{min} \leq T_{amb} \leq T_{max}$		1	150 300	pA
I_{CC}	Supply current (per amplifier, A_{VCL} = 1, no load) $T_{min} \leq T_{amb} \leq T_{max}$		400	600 700	µA
CMR	Common mode rejection ratio V_{ic} = 3 to 7 V, V_o = 5 V V_{ic} = 0 to 10 V, V_o = 5 V	 60 50	 90 75		dB
SVR	Supply voltage rejection ratio (V_{CC+} = 5 to 10 V, $V_o = V_{CC}/2$)	60	90		dB
A_{vd}	Large signal voltage gain (R_L = 10 kΩ, V_o = 2.5 V to 7.5 V) $T_{min} \leq T_{amb} \leq T_{max}$	15 10	50		V/mV
V_{OH}	High level output voltage (V_{id} = 1V) R_L = 100 kΩ R_L = 10 kΩ R_L = 600 Ω R_L = 100 Ω $T_{min} \leq T_{amb} \leq T_{max}$ R_L = 10 kΩ R_L = 600 Ω	 9.95 9.85 9 9.8 8.8	 9.95 9.35 7.8		V
V_{OL}	Low level output voltage (V_{id} = -1 V) R_L = 100 kΩ R_L = 10 kΩ R_L = 600 Ω R_L = 100 Ω $T_{min} \leq T_{amb} \leq T_{max}$ R_L = 10 kΩ R_L = 600 Ω		 50 650 2300	 50 150 800 150 900	mV
I_o	Output short-circuit current (V_{id} = ±1 V) Source ($V_o = V_{CC-}$) Sink ($V_o = V_{CC+}$)	 45 50	 65 75		mA
GBP	Gain bandwidth product (A_{VCL} = 100, R_L = 10 kΩ, C_L = 100 pF, f = 100 kHz)		1.4		MHz

Table 5. V_{CC+} = 10 V, V_{CC-} = 0 V, R_L, C_L connected to $V_{CC}/2$, T_{amb} = 25 °C (unless otherwise specified) (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SR^+	Slew rate (A_{VCL} = 1, R_L = 10 kΩ, C_L = 100 pF, V_i = 2.5 V to 7.5 V)		1.3		V/μs
SR^-	Slew rate (A_{VCL} = 1, R_L = 10 kΩ, C_L = 100 pF, V_i = 2.5 V to 7.5 V)		0.8		V/μs
φm	Phase margin		40		Degrees
en	Equivalent input noise voltage (R_s = 100 Ω, f = 1 kHz)		30		nV/√Hz
THD	Total harmonic distortion (A_{VCL} = 1, R_L = 10 kΩ, C_L = 100 pF, V_o = 4.75 V to 5.25 V, f = 1 kHz)		0.02		%
C_{in}	Input capacitance		1.5		pF

1. Maximum values include unavoidable inaccuracies of the industrial tests.

Figure 2. Supply current (each amplifier) vs. supply voltage

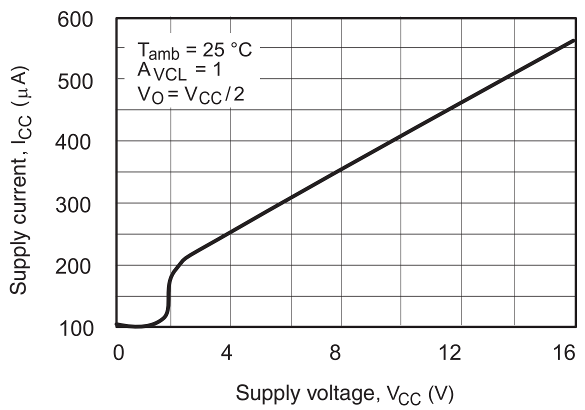


Figure 3. High level output voltage vs. high level output current (V_{CC} = +5 V, V_{CC} = +3 V)

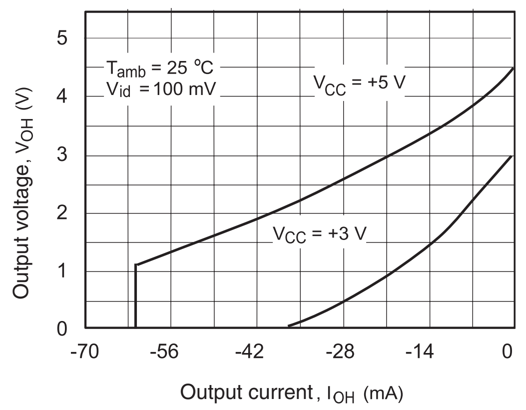


Figure 4. Low level output voltage vs. low level output current (V_{CC} = +3 V, V_{CC} = +5 V)

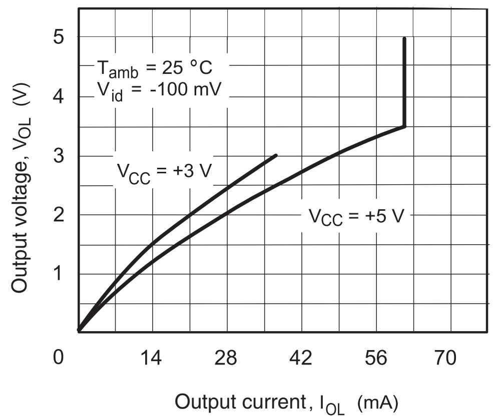


Figure 5. Input bias current vs. temperature

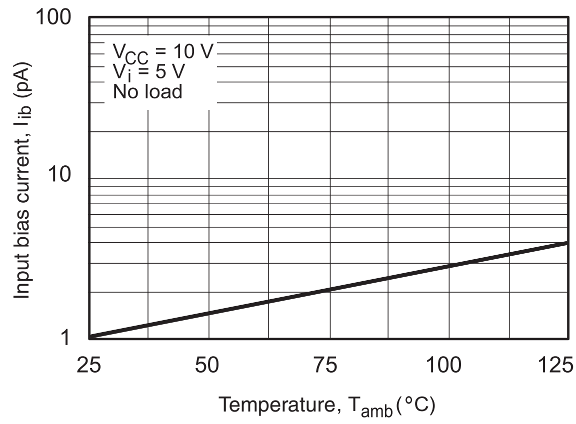


Figure 6. High level output voltage vs. high level output current (V_{CC} = +16 V, V_{CC} = +10 V)

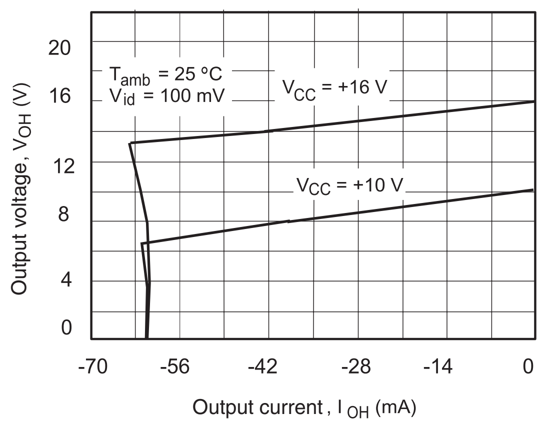


Figure 7. Low level output voltage vs. low level output current (V_{CC} = 16 V, V_{CC} = 10 V)

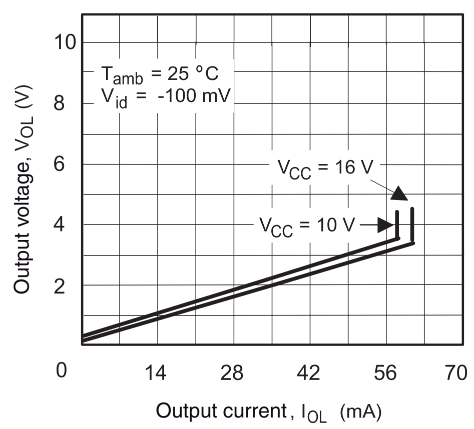


Figure 8. Gain and phase vs. frequency (R_L = 10 kΩ)

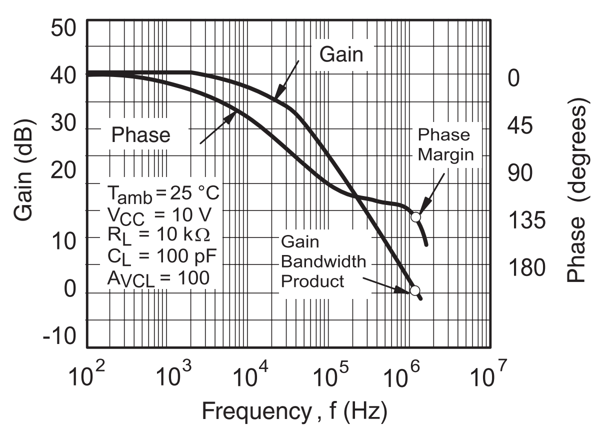


Figure 9. Gain bandwidth product vs. supply voltage (R_L = 10 kΩ)

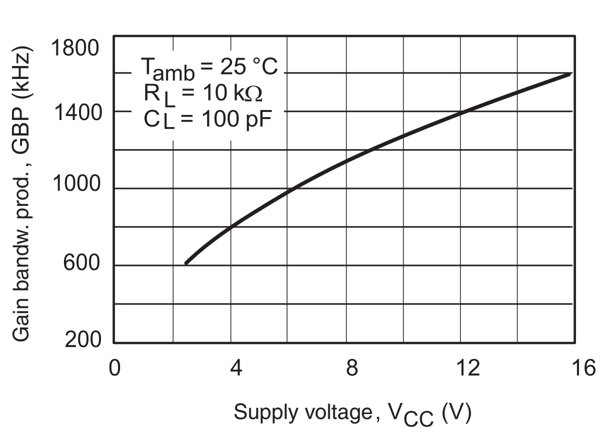


Figure 10. Phase margin vs. supply voltage (R_L = 10 kΩ)

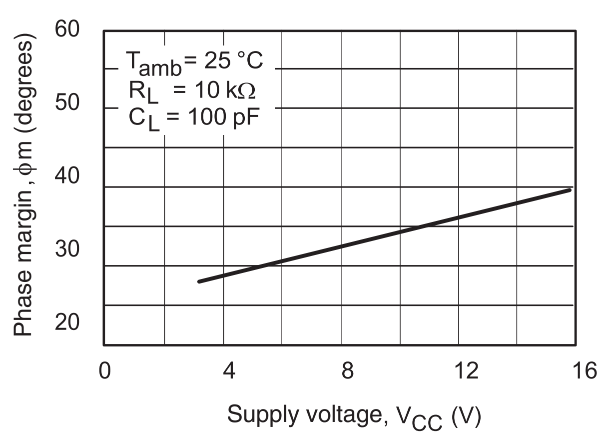


Figure 11. Gain and phase vs. frequency (R_L = 600 Ω)

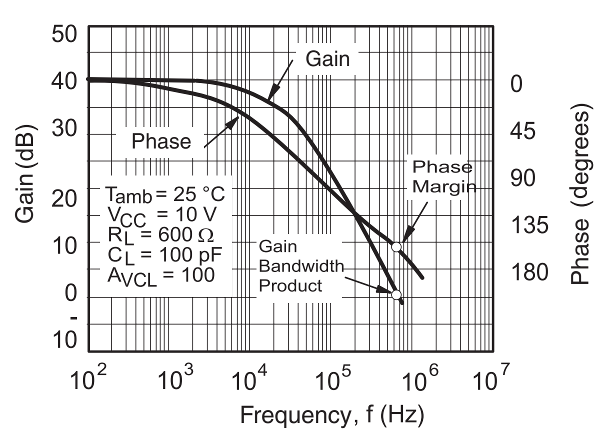


Figure 12. Gain bandwidth product vs. supply voltage (R_L = 600 Ω)

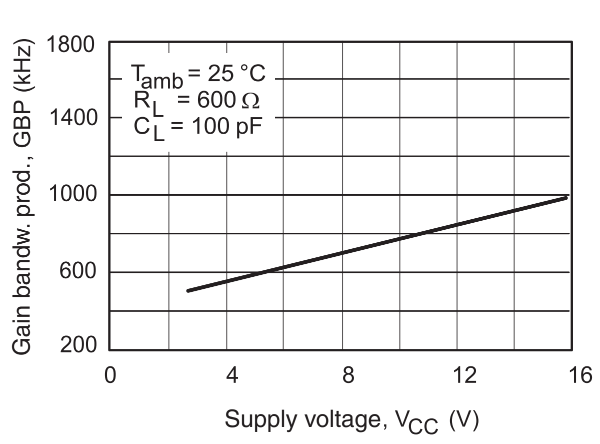


Figure 13. Phase margin vs. supply voltage (R_L = 600 Ω)

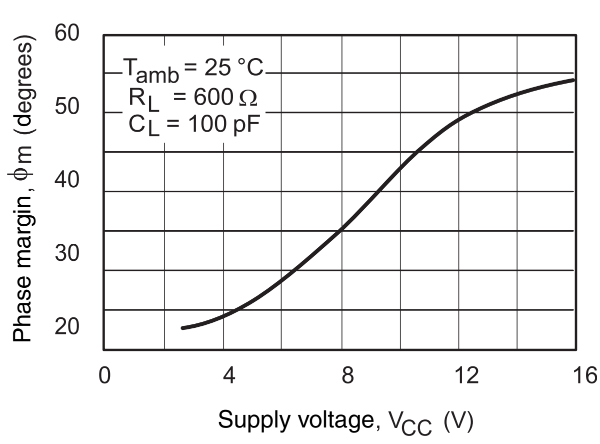
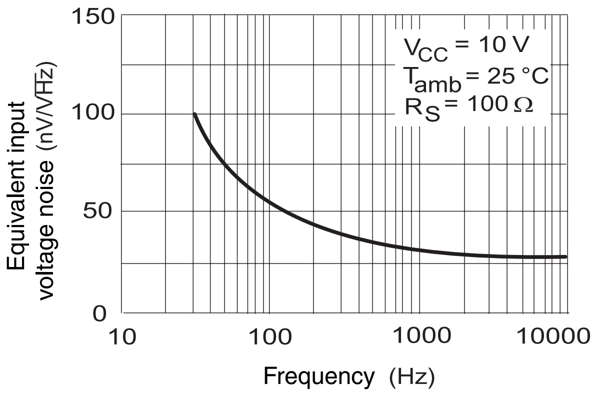


Figure 14. Input voltage noise vs. frequency



4 Macromodel

4.1 Important note concerning this macromodel

- All models are a trade-off between accuracy and complexity (i.e. simulation time).
- Macromodels are not a substitute to breadboarding; rather, they confirm the validity of a design approach and help to select surrounding component values.
- A macromodel emulates the **nominal** performance of a **typical** device within **specified operating conditions** (temperature, supply voltage, for example). Thus the macromodel is often not as exhaustive as the datasheet, its purpose is to illustrate the main parameters of the product.

Data derived from macromodels used outside of the specified conditions (V_{CC}, temperature, for example) or even worse, outside of the device operating conditions (V_{CC}, V_{icm}, for example), is not reliable in any way.

4.2 Macromodel code

```
** Standard Linear Ics Macromodels, 1993.
** CONNECTIONS :
* 1 INVERTING INPUT
* 2 NON-INVERTING INPUT
* 3 OUTPUT
* 4 POSITIVE POWER SUPPLY
* 5 NEGATIVE POWER SUPPLY
.SUBCKT TS912 1 2 3 4 5
**********************************************************
.MODEL MDTH D IS=1E-8 KF=6.563355E-14 CJO=10F
* INPUT STAGE
CIP 2 5 1.500000E-12
CIN 1 5 1.500000E-12
EIP 10 5 2 5 1
EIN 16 5 1 5 1
RIP 10 11 6.500000E+00
RIN 15 16 6.500000E+00
RIS 11 15 7.655100E+00
DIP 11 12 MDTH 400E-12
DIN 15 14 MDTH 400E-12
VOFP 12 13 DC 0.000000E+00
VOFN 13 14 DC 0
IPOL 13 5 4.000000E-05
CPS 11 15 3.82E-08
DINN 17 13 MDTH 400E-12
VIN 17 5 -0.5000000e+00
DINR 15 18 MDTH 400E-12
VIP 4 18 -0.5000000E+00
FCP 4 5 VOFP 7.750000E+00
FCN 5 4 VOFN 7.750000E+00
* AMPLIFYING STAGE
FIP 5 19 VOFP 5.500000E+02
FIN 5 19 VOFN 5.500000E+02
RG1 19 5 5.087344E+05
RG2 19 4 5.087344E+05
CC 19 29 2.200000E-08
HZTP 30 29 VOFP 12.33E+02
HZTN  5 30 VOFN 12.33E+02
DOPM 19 22 MDTH 400E-12
DONM 21 19 MDTH 400E-12
HOPM 22 28 VOUT 3135
VIPM 28 4 150
HONM 21 27 VOUT 3135
VINM 5 27 150
EOUT 26 23 19 5 1
VOUT 23 5 0
ROUT 26 3 65
COUT 3 5 1.000000E-12
DOP 19 68 MDTH 400E-12
VOP 4 25 1.924
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HSCP 68 25 VSCP1 1E8
DON 69 19 MDTH 400E-12
VON 24 5 2.4419107
HSCN 24 69 VSCN1 1.5E8
VSCTHP 60 61 0.1375
DSCP1 61 63 MDTH 400E-12
VSCP1 63 64 0
ISCP 64 0 1.000000E-8
DSCP2 0 64 MDTH 400E-12
DSCN2 0 74 MDTH 400E-12
ISCN 74 0 1.000000E-8
VSCN1 73 74 0
DSCN1 71 73 MDTH 400E-12
VSCTHN 71 70 -0.75
ESCP 60 0 2 1 500
ESCN 70 0 2 1 -2000
.ENDS
```

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

5.1 DIP8 package information

Figure 15. DIP8 package outline

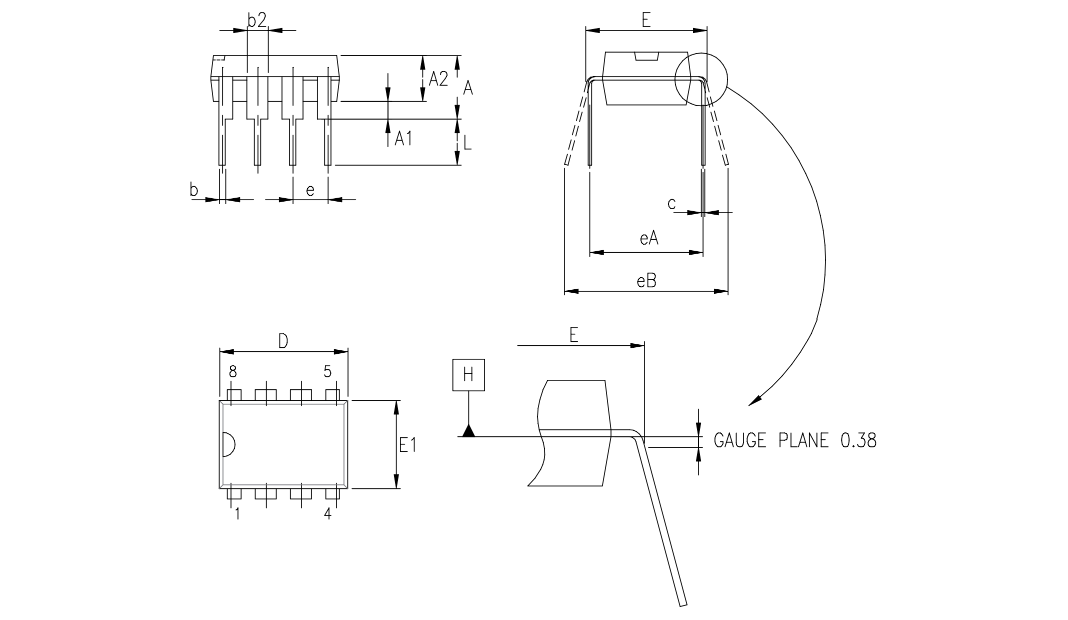

Table 6. DIP8 package mechanical data

Symbol	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.33			0.210
A1	0.38			0.015		
A2	2.92	3.30	4.95	0.115	0.130	0.195
b	0.36	0.46	0.56	0.014	0.018	0.022
b2	1.14	1.52	1.78	0.045	0.060	0.070
c	0.20	0.25	0.36	0.008	0.010	0.014
D	9.02	9.27	10.16	0.355	0.365	0.400
E	7.62	7.87	8.26	0.300	0.310	0.325
E1	6.10	6.35	7.11	0.240	0.250	0.280
e		2.54			0.100	
eA		7.62			0.300	
eB			10.92			0.430
L	2.92	3.30	3.81	0.115	0.130	0.150

5.2 SO-8 package information

Figure 16. SO-8 package outline

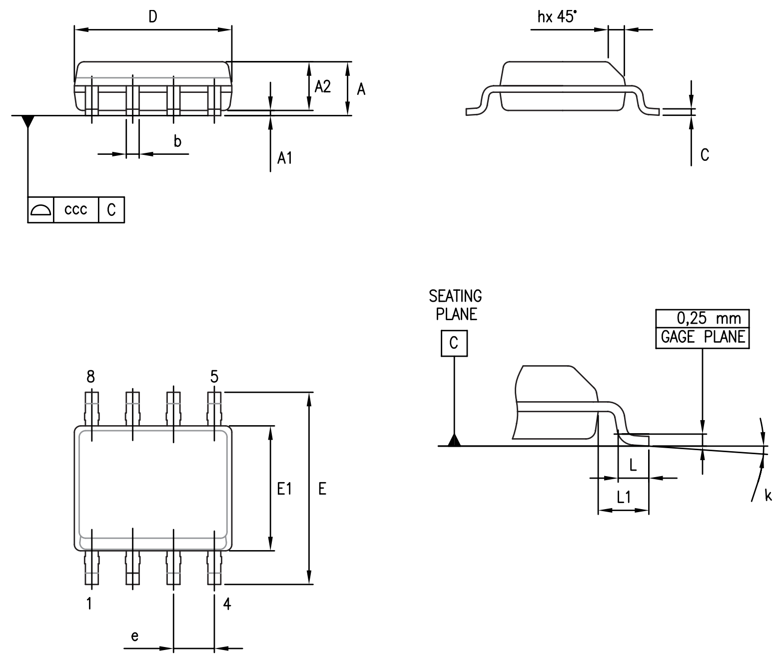

Table 7. SO-8 package mechanical data

Symbol	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
L1		1.04			0.040	
k	0		8°	1°		8°
ccc			0.10			0.004

6 Ordering information

Table 8. Order codes

Part number	Temperature range	Package	Packing	Marking
TS912IN	-40 °C, +125 °C	DIP8	Tube	TS912IN
TS912AIN				TS912AIN
TS912ID TS912IDT		SO-8	Tube or tape and reel	912I
TS912AID TS912AIDT				912AI
TS912BID TS912BIDT				912BI
TS912IYDT(1)		SO-8 (automotive grade level)		912IY
TS912AIYDT(1)				912AIY
TS912BIYDT(1)				912BY

1. Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q 002 or equivalent.

7 Revision history

Table 9. Document revision history

Date	Revision	Changes
04-Dec-2001	1	First release.
31-Jul-2005	2	PPAP references inserted in the datasheet, see order codes table. ESD protection inserted in AMR table.
03-Oct-2005	3	Some errors in the Order Codes table were corrected. Reorganization of *Section 4: Macromodel*.
13-Feb- 2006	4	Parameters added in AMR table (T_j, ESD, R_{thja}, R_{thjc}).
16-Oct-2007	5	Corrected units and ESD footnotes in *Table 1: Absolute maximum ratings*. Corrected misalignments in electrical characteristics table. Updated *Section 4: Macromodel*. Added missing automotive grade order codes and footnote in *Table 8: Order codes*. Format update.
01-Feb-2010	6	Added TS912A and TS912B part numbers on cover page.
06-Nov-2012	7	Updated *Features* (added *Related products*). Updated *Figure 3*, *Figure 4*, *Figure 6* to *Figure 13* (added conditions to differentiate them). Removed TS912IYD, TS912AIYD, and TS912BIYD device from *Table 8*. Minor corrections throughout document.