TS914, TS914A

Rail-to-rail CMOS quad operational amplifier

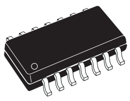
Datasheet − production data

Features

- Rail-to-rail input and output voltage ranges
- Single (or dual) supply operation from 2.7 to 16 V
- Extremely low input bias current: 1 pA typical
- Low input offset voltage: 5 mV max. (A grade)
- Specified for 600 Ω and 100 Ω loads
- Low supply current: 200 µA/ampli. (V_{CC} = 3 V)
- Latch-up immunity
- Spice macromodel included in this specification

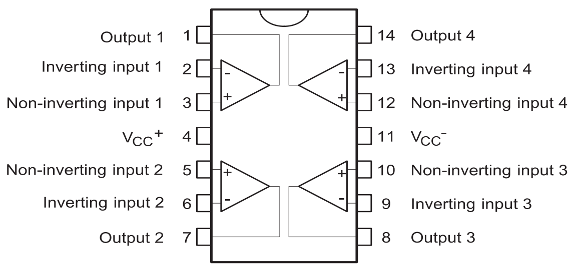
Related products

- See TS56x series for better accuracy and smaller packages



D
SO-14
(plastic micropackage)

Pin connections (top view)



Description

The TS914 device is a rail-to-rail CMOS quad operational amplifier designed to operate with a single or dual supply voltage.

The input voltage range V_{icm} includes the two supply rails V_{CC+} and V_{CC-}.

The output reaches V_{CC-} +50 mV, V_{CC+} -50 mV, with R_L = 10 kΩ, and V_{CC-} +350 mV, V_{CC+} - 350 mV, with R_L = 600 Ω

This product offers a broad supply voltage operating range from 2.7 to 16 V and a supply current of only 200 µA/amp. (V_{CC} = 3 V).

The source and sink output current capability is typically 40 mA (at V_{CC} = 3 V), fixed by an internal limitation circuit.

1 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage(1)	18	V
V_{id}	Differential input voltage(2)	±18	V
V_{in}	Input voltage(3)	-0.3 to 18	V
I_{in}	Current on inputs	±50	mA
I_o	Current on outputs	±130	mA
T_j	Maximum junction temperature	150	°C
T_{stg}	Storage temperature	-65 to +150	°C
R_{thja}	Thermal resistance junction to ambient(4)	103	°C/W
R_{thjc}	Thermal resistance junction to case	31	°C/W
ESD	HBM: human body model(5)	1	kV
	MM: machine model(6)	50	V
	CDM: charged device model(7)	1.5	kV

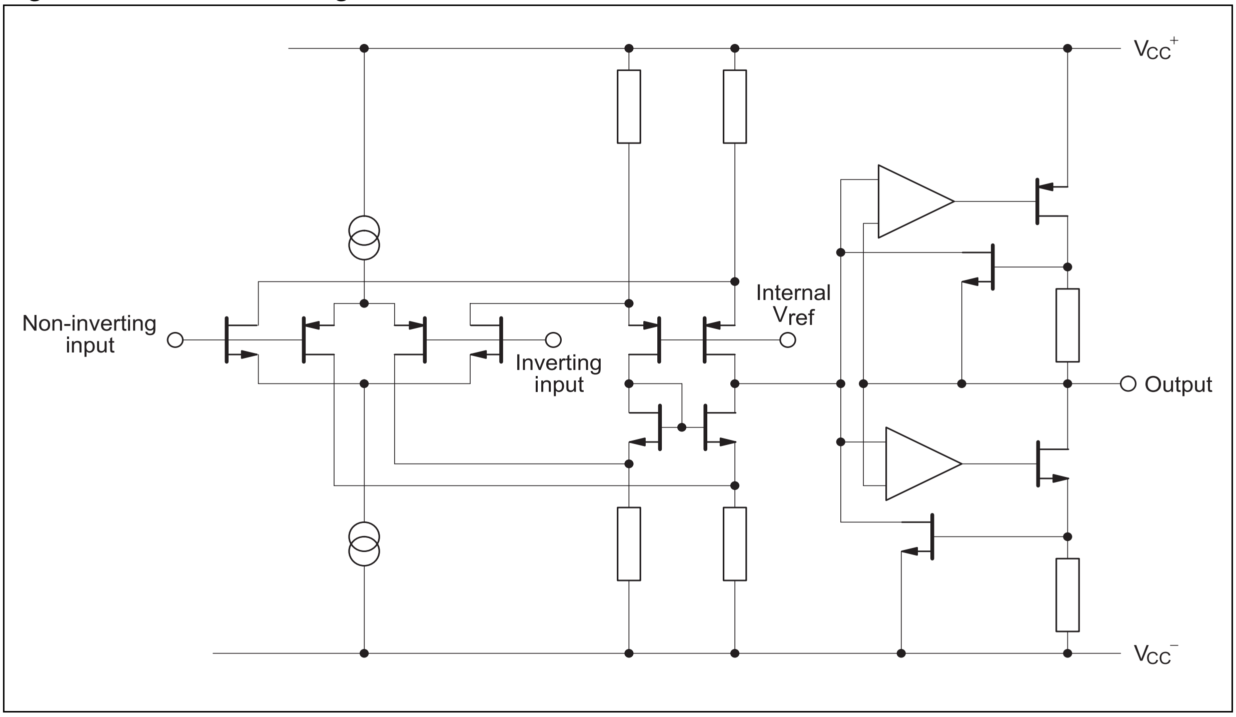
1. All voltage values, except differential voltage are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of input and output voltages must never exceed V_{CC}^+ +0.3 V.
4. Short-circuits can cause excessive heating. Destructive dissipation can result from simultaneous short-circuit on all amplifiers. These are typical values.
5. Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
6. Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.
7. Charged device model: all pins and the package are charged together to the specified voltage and then discharged directly to ground through only one pin. This is done for all pins.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.7 to 16	V
V_{icm}	Common mode input voltage range	V_{CC-} -0.2 to V_{CC+} +0.2	V
T_{oper}	Operating free air temperature range	-40 to + 125	°C

2 Schematic diagram

Figure 1. Schematic diagram



3 Electrical characteristics

Table 3. $V_{CC+} = 3$ V, $V_{CC-} = 0$ V, R_L, C_L connected to $V_{CC}/2$, $T_{amb} = 25$ °C (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage ($V_{icm} = V_o = V_{CC}/2$)	TS914 TS914A $T_{min} \leq T_{amb} \leq T_{max}$, TS914 $T_{min} \leq T_{amb} \leq T_{max}$, TS914A			10 5 12 7	mV
ΔV_{io}	Input offset voltage drift			5		µV/°C
I_{io}	Input offset current(1)	 $T_{min} \leq T_{amb} \leq T_{max}$		1	100 200	pA
I_{ib}	Input bias current(1)	 $T_{min.} \leq T_{amb} \leq T_{max}$		1	150 300	pA
I_{CC}	Supply current	per amplifier, $A_{VCL} = 1$, no load $T_{min} \leq T_{amb} \leq T_{max}$		200	300 400	µA
CMR	Common mode rejection ratio	$V_{icm} = 0$ to 3 V, $V_o = 1.5$ V		70		dB
SVR	Supply voltage rejection ratio	$V_{CC+} = 2.7$ to 3.3 V, $V_o = V_{CC}/2$		80		dB
A_{vd}	Large signal voltage gain	$R_L = 10$ kΩ, $V_o = 1.2$ V to 1.8 V $T_{min} \leq T_{amb} \leq T_{max}$	3 2	10		V/mV
V_{OH}	High level output voltage	$V_{id} = 1$ V, $R_L = 10$ kΩ $R_L = 600$ Ω $R_L = 100$ Ω $V_{id} = 1$V, $T_{min} \leq T_{amb} \leq T_{max}$ $R_L = 10$ kΩ $R_L = 600$ Ω	 2.9 2.2 2.8 2.1	 2.97 2.7 2		V
V_{OL}	Low level output voltage	$V_{id} = -1$ V, $R_L = 10$ kΩ $R_L = 600$ Ω $R_L = 100$ Ω $V_{id} = -1$ V, $T_{min} \leq T_{amb} \leq T_{max}$ $R_L = 10$ kΩ $R_L = 600$ Ω		 50 300 900	 100 600 150 900	mV
I_o	Output short-circuit current	$V_{id} = \pm 1$ V Source ($V_o = V_{CC-}$) Sink ($V_o = V_{CC+}$)		 40 40		mA
GBP	Gain bandwidth product	$A_{VCL} = 100$, $R_L = 10$ kΩ, $C_L = 100$ pF, f = 100 kHz		0.8		MHz
SR	Slew rate	$A_{VCL} = 1$, $R_L = 10$ kΩ, $C_L = 100$ pF, $V_{in} = 1.3$ V to 1.7 V		0.5		V/µs
ϕ_m	Phase margin			30		°
e_n	Equivalent input noise voltage	$R_s = 100$ Ω, f = 1 kHz		30		nV/√Hz
V_{O1}/V_{O2}	Channel separation	f = 1 kHz		120		dB

1. Maximum values include unavoidable inaccuracies of the industrial tests.

Table 4. V_{CC}^+ = 5 V, V_{CC}^- = 0 V, R_L, C_L connected to $V_{CC}/2$, T_{amb} = 25 °C (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage ($V_{icm} = V_o = V_{CC}/2$)	TS914 TS914A $T_{min} \le T_{amb} \le T_{max}$, TS914 $T_{min} \le T_{amb} \le T_{max}$, TS914A			10 5 12 7	mV
ΔV_{io}	Input offset voltage drift			5		µV/°C
I_{io}	Input offset current (1)	 $T_{min} \le T_{amb} \le T_{max}$		1	100 200	pA
I_{ib}	Input bias current (1)	 $T_{min} \le T_{amb} \le T_{max}$		1	150 300	pA
I_{CC}	Supply current	per amplifier, A_{VCL} = 1, no load $T_{min} \le T_{amb} \le T_{max}$		230	350 450	µA
CMR	Common mode rejection ratio	V_{icm} = 1.5 to 3 V, V_o = 2.5 V		85		dB
SVR	Supply voltage rejection ratio	V_{CC+} = 3 to 5 V, $V_o = V_{CC}/2$		80		dB
A_{vd}	Large signal voltage gain	R_L = 10 kΩ, V_o = 1.5 V to 3.5 V $T_{min} \le T_{amb} \le T_{max}$	10 7	40		V/mV
V_{OH}	High level output voltage	V_{id} = 1 V, R_L = 10 kΩ R_L = 600 Ω R_L = 100 Ω V_{id} = 1 V, $T_{min} \le T_{amb} \le T_{max}$ R_L = 10 kΩ R_L = 600 Ω	 4.85 4.20 4.8 4.1	 4.95 4.65 3.7		V
V_{OL}	Low level output voltage	V_{id} = -1 V, R_L = 10 kΩ R_L = 600 Ω R_L = 100 Ω V_{id} = -1 V, $T_{min} \le T_{amb} \le T_{max}$ R_L = 10 kΩ R_L = 600 Ω		 50 350 1400	 100 680 150 900	mV
I_o	Output short-circuit current	V_{id} = ±1 V Source ($V_o = V_{CC-}$) Sink ($V_o = V_{CC+}$)		 60 60		mA
GBP	Gain bandwidth product	A_{VCL} = 100, R_L = 10 kΩ, C_L = 100 pF, f = 100 kHz		1		MHz
SR	Slew rate	A_{VCL} = 1, R_L = 10 kΩ, C_L = 100 pF, V_{in} = 1 V to 4 V		0.8		V/µs
ϕ_m	Phase margin			30		°
e_n	Equivalent input noise voltage	R_s = 100 Ω, f = 1 kHz		30		nV/√Hz
V_{O1}/V_{O2}	Channel separation	f = 1 kHz		120		dB

1. Maximum values include unavoidable inaccuracies of the industrial tests.

Table 5. V_{CC}^+ = 10 V, V_{DD} = 0 V, R_L, C_L connected to $V_{CC}/2$, T_{amb} = 25 °C (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage (V_{icm} = V_o = $V_{CC}/2$)	TS914 TS914A $T_{min} \le T_{amb} \le T_{max}$, TS914 $T_{min} \le T_{amb} \le T_{max}$, TS914A			10 5 12 7	mV
ΔV_{io}	Input offset voltage drift			5		µV/°C
I_{io}	Input offset current(1)	 $T_{min} \le T_{amb} \le T_{max}$		1	100 200	pA
I_{ib}	Input bias current(1)	 $T_{min} \le T_{amb} \le T_{max}$		1	150 300	pA
CMR	Common mode rejection ratio	V_{icm} = 3 to 7 V, V_o = 5 V V_{icm} = 0 to 10 V, V_o = 5 V		90 75		dB
SVR	Supply voltage rejection ratio	V_{CC+}= 5 to 10 V, V_o = $V_{CC}/2$		90		dB
A_{vd}	Large signal voltage gain	R_L = 10 kΩ, V_o = 2.5 V to 7.5 V $T_{min} \le T_{amb} \le T_{max}$	15 10	60		V/mV
V_{OH}	High level output voltage	V_{id} = 1 V, R_L = 10 kΩ R_L = 600 Ω R_L = 100 Ω V_{id} = 1 V, $T_{min} \le T_{amb} \le T_{max}$ R_L = 10 kΩ R_L = 600 Ω	 9.85 9 9.8 9	 9.95 9.35 7.8		V
V_{OL}	Low level output voltage	V_{id} = -1 V, R_L = 10 kΩ R_L = 600 Ω R_L = 100 Ω V_{id} = -1 V, $T_{min} \le T_{amb} \le T_{max}$ R_L = 10 kΩ R_L = 600 Ω		 50 650 2300	 180 800 150 900	mV
I_o	Output short-circuit current	V_{id} = ±1 V		60		mA
I_{CC}	Supply current / operator	A_{VCL} = 1, no load, $T_{min} \le T_{amb} \le T_{max}$		400	600 700	µA
GBP	Gain bandwidth product	A_{VCL} = 100, R_L = 10 kΩ, C_L = 100 pF, f = 100 kHz		1.4		MHz
SR	Slew rate	A_{VCL} = 1, R_L = 10 kΩ, C_L = 100 pF, V_i = 2.5 V to 7.5 V		1		V/µs
ϕ_m	Phase margin	R_s = 100 Ω, f = 1 kHz		40		°
e_n	Equivalent input noise voltage	R_s = 100 Ω, f = 1 kHz		30		nV/√Hz
THD	Total harmonic distortion	A_{VCL} = 1, R_L = 10 kΩ, C_L = 100 pF, V_o = 4.75 to 5.25 V, f = 1 kHz		0.02		%
C_{in}	Input capacitance			1.5		pF

Table 5. V_{CC}^{+} = 10 V, V_{DD} = 0 V, R_L, C_L connected to $V_{CC}/2$, T_{amb} = 25 °C (unless otherwise specified) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
R_{in}	Input resistance			>10		Tera Ω
V_{O1}/V_{O2}	Channel separation	f = 1 kHz		120		dB

1. Maximum values include unavoidable inaccuracies of the industrial tests.

Figure 2. Supply current (each amplifier) vs. supply voltage

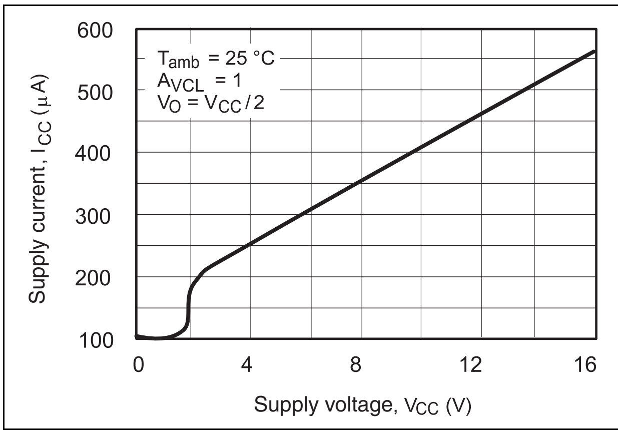


Figure 3. High level output voltage vs. high level output current (V_{CC} = +5 V, V_{CC} = +3 V)

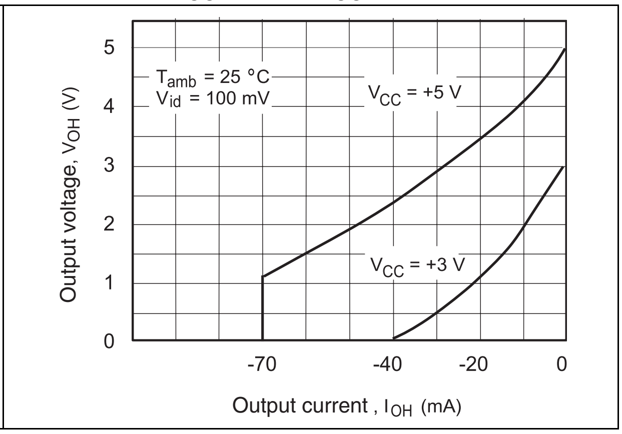


Figure 4. Low level output voltage vs. low level output current (V_{CC} = +5 V, V_{CC} = +3 V)

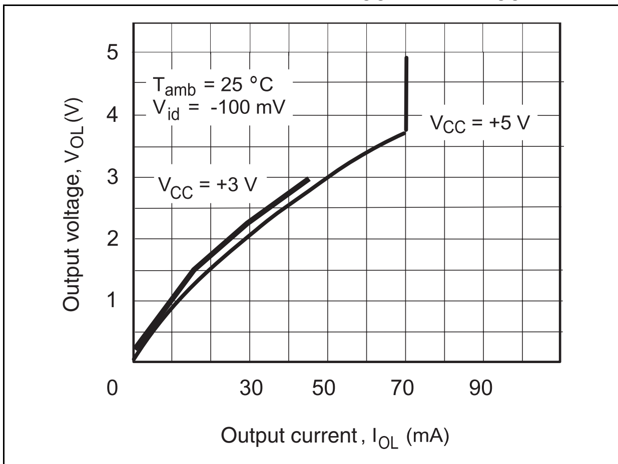


Figure 5. Input bias current vs. temperature

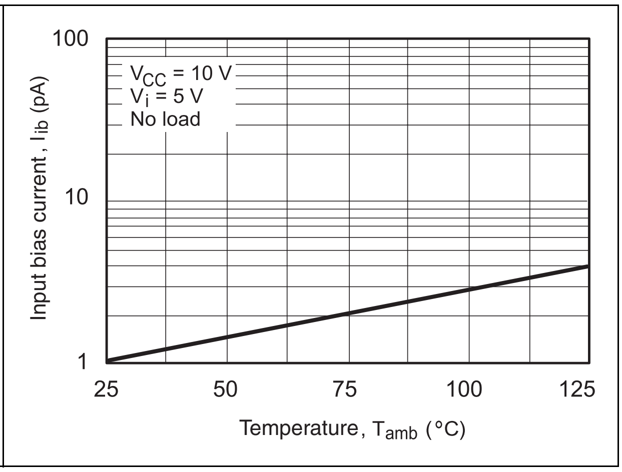


Figure 6. High level output voltage vs. high level output current (V_{CC} = +16 V, V_{CC} = +10 V)

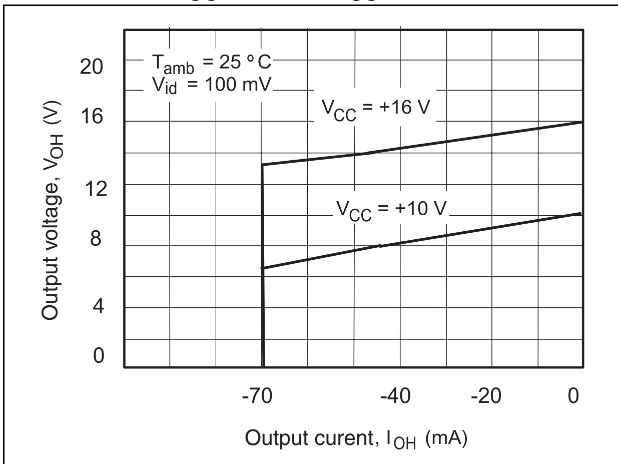


Figure 7. Low level output voltage vs. low level output current (V_{CC} = 16 V, V_{CC} = 10 V)

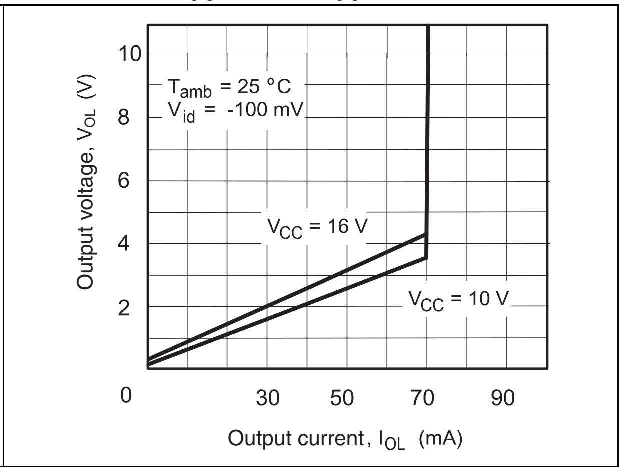


Figure 8. Gain and phase vs. frequency (R_L = 10 kΩ)

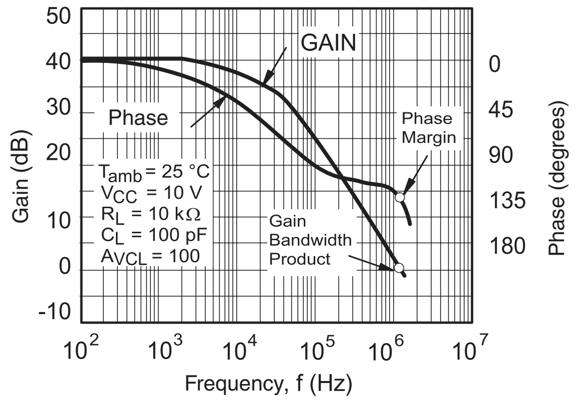


Figure 9. Gain bandwidth product vs. supply voltage (R_L = 10 kΩ)

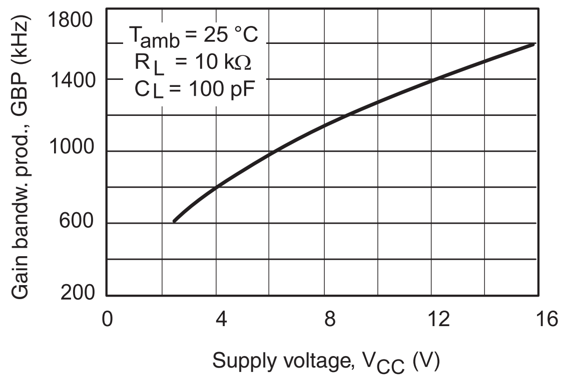


Figure 10. Phase margin vs. supply voltage (R_L = 10 kΩ)

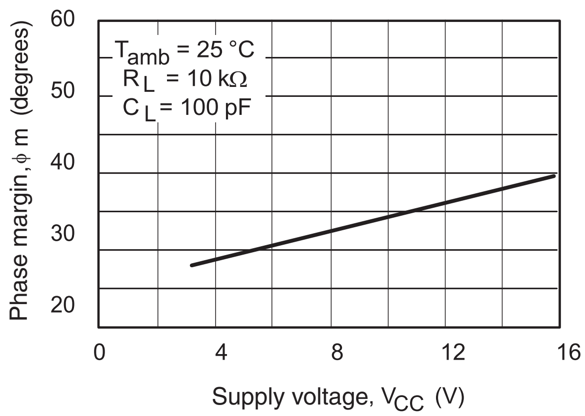


Figure 11. Gain and phase vs. frequency (R_L = 600 Ω)

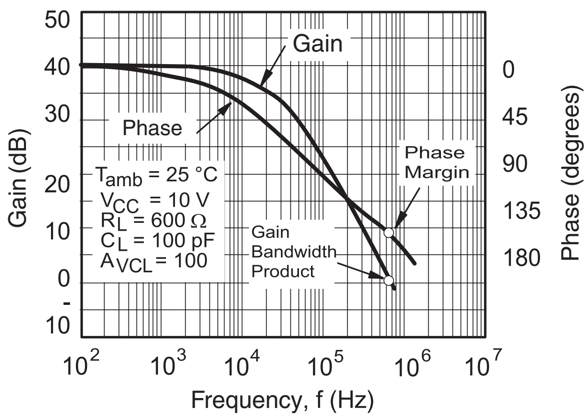


Figure 12. Gain bandwidth product vs. supply voltage (R_L = 600 Ω)

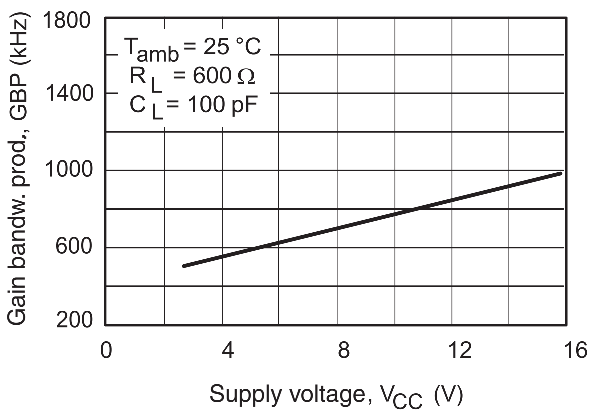


Figure 13. Phase margin vs. supply voltage (R_L = 600 Ω)

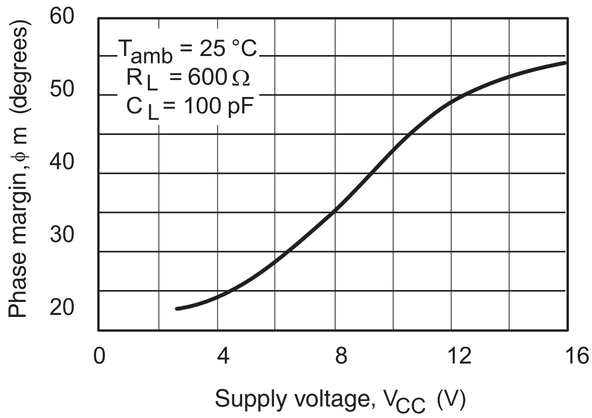
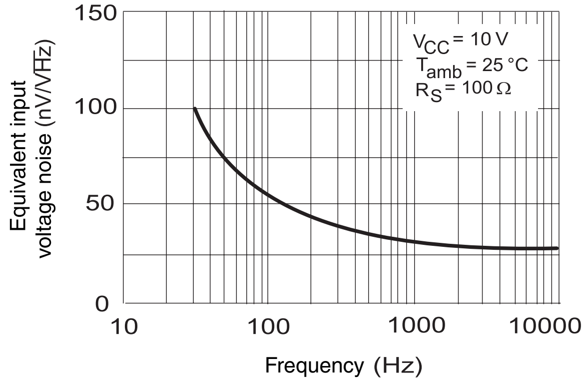


Figure 14. Input voltage noise vs. frequency



4 Macromodels

4.1 Important note concerning this macromodel

- All models are a trade-off between accuracy and complexity (that is, simulation time). Macromodels are not a substitute for breadboarding; rather, they confirm the validity of a design approach and help to select surrounding component values.
- A macromodel emulates the nominal performance of a typical device within specified operating conditions (such as temperature or supply voltage, etc.). Thus, the macromodel is often not as exhaustive as the datasheet, its purpose is to illustrate the main parameters of the product.
- Data derived from macromodels used outside of the specified conditions (such as V_{CC}, or temperature) or even worse, outside of the device's operating conditions (such as V_{CC} or V_{icm}) is not reliable in any way.

The values provided in *Table 6* are derived from this macromodel.

Table 6. V_{CC}^+ = 3 V, V_{CC}- = 0 V, R_L, C_L connected to $V_{CC/2}$, T_{amb} = 25 °C (unless otherwise specified)

Symbol	Conditions	Value	Unit
V_{io}		0	mV
A_{vd}	R_L = 10 kΩ	10	V/mV
I_{CC}	No load, per operator	100	µA
V_{icm}		-0.2 to 3.2	V
V_{OH}	R_L = 600 Ω	2.96	V
V_{OL}	R_L = 60 Ω	300	mV
I_{sink}	V_O = 3 V	40	mA
I_{source}	V_O = 0 V	40	mA
GBP	R_L = 10 kΩ, C_L = 100 pF	0.8	MHz
SR	R_L = 10 kΩ, C_L = 100 pF	0.3	V/µs
ϕ_m	Phase margin	30	Degrees

4.2 Macromodel code

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* Standard Linear Ics Macromodels, 1993.
** CONNECTIONS :
* 1 INVERTING INPUT
* 2 NON-INVERTING INPUT
* 3 OUTPUT
* 4 POSITIVE POWER SUPPLY
* 5 NEGATIVE POWER SUPPLY
*
.SUBCKT TS914 1 2 3 4 5
**************************************************
.MODEL MDTH D IS=1E-8 KF=6.564344E-14 CJO=10F
CIP 2 5 1.000000E-12
CIN 1 5 1.000000E-12
EIP 10 5 2 5 1
EIN 16 5 1 5 1
RIP 10 11 6.500000E+00
RIN 15 16 6.500000E+00
RIS 11 15 7.322092E+00
DIP 11 12 MDTH 400E-12
DIN 15 14 MDTH 400E-12
VOFP 12 13 DC 0.000000E+00
VOFN 13 14 DC 0
IPOL 13 5 4.000000E-05
CPS 11 15 2.498970E-08
DINN 17 13 MDTH 400E-12
VIN 17 5 0.000000e+00
DINR 15 18 MDTH 400E-12
VIP 4 18 0.000000E+00
FCP 4 5 VOFP 5.750000E+00
FCN 5 4 VOFN 5.750000E+00
* AMPLIFYING STAGE
FIP 5 19 VOFP 4.400000E+02
FIN 5 19 VOFN 4.400000E+02
RG1 19 5 4.904961E+05
RG2 19 4 4.904961E+05
CC 19 29 2.200000E-08
HZTP 30 29 VOFP 1.8E+03
HZTN 5 30 VOFN 1.8E+03
DOPM 19 22 MDTH 400E-12
DONM 21 19 MDTH 400E-12
HOPM 22 28 VOUT 3800
VIPM 28 4 230
HONM 21 27 VOUT 3800
VINM 5 27 230
EOUT 26 23 19 5 1
VOUT 23 5 0
ROUT 26 3 82
COUT 3 5 1.000000E-12
DOP 19 68 MDTH 400E-12
VOP 4 25 1.724
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HSCP 68 25 VSCP1 0.8E+8
DON 69 19 MDTH 400E-12
VON 24 5 1.7419107
HSCN 24 69 VSCN1 0.8E+8
VSCTHP 60 61 0.0875
DSCP1 61 63 MDTH 400E-12
VSCP1 63 64 0
ISCP 64 0 1.000000E-8
DSCP2 0 64 MDTH 400E-12
DSCN2 0 74 MDTH 400E-12
ISCN 74 0 1.000000E-8
VSCN1 73 74 0
DSCN1 71 73 MDTH 400E-12
VSCTHN 71 70 -0.55
ESCP 60 0 2 1 500
ESCN 70 0 2 1 -2000
.ENDS
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5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Figure 15. SO-14 package outline

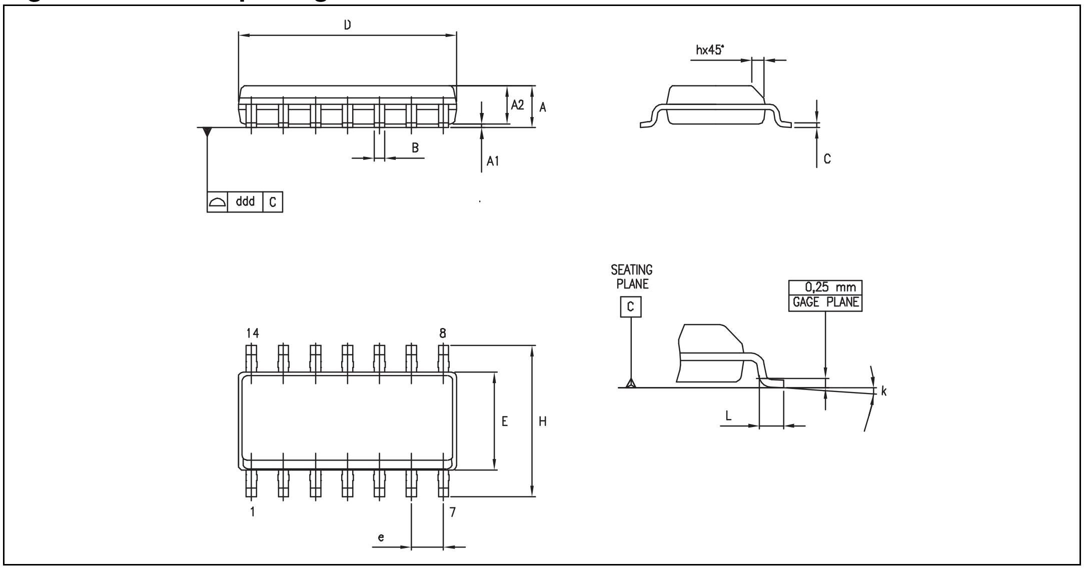

Table 7. SO-14 package mechanical data

Symbol	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.35		1.75	0.05		0.068
A1	0.10		0.25	0.004		0.009
A2	1.10		1.65	0.04		0.06
B	0.33		0.51	0.01		0.02
C	0.19		0.25	0.007		0.009
D	8.55		8.75	0.33		0.34
E	3.80		4.0	0.15		0.15
e		1.27			0.05	
H	5.80		6.20	0.22		0.24
h	0.25		0.50	0.009		0.02
L	0.40		1.27	0.015		0.05
k	8° (max.)					
ddd			0.10			0.004

6 Ordering information

Table 8. Order codes

Order code	Temperature range	Package	Packing	Marking
TS914ID TS914IDT	-40, +125 °C	SO-14	Tube and tape and reel	914I
TS914AID TS914AIDT		SO-14	Tube and tape and reel	914AI
TS914IYDT(1)		SO-14 (automotive grade level)	Tube and tape and reel	914IY
TS914AIYDT(1)		SO-14 (automotive grade level)	Tape and reel	914AIY

1. Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q 002 or equivalent.

7 Revision history

Table 9. Document revision history

Date	Revision	Changes
01-Dec-2001	1	Initial release.
01-Nov-2004	2	Changed V_{io} max. on cover page from 2 mV to 5 mV.
01-Jun-2005	3	Inserted PIPAP references (see order code table on cover page).
01-Feb-2006	4	Added parameters in *Table 1: Absolute maximum ratings on page 2* (T_j, ESD, R_{thja}, R_{thjc}).
08-Jan-2007	5	Corrected package names in order codes table on cover page. Corrected macromodel.
02-Apr-2009	6	Minor text edits. Removed table of contents. Updated package information in *Chapter 5*. Moved *Table 8: Order codes* from cover page to end of datasheet. Added footnote to *Table 8: Order codes*.
04-Feb-2010	7	Added parameters for TS914A. Removed DIP14 package information. Removed TS914AIYD order code from *Table 8*.
06-Nov-2012	8	Updated *Features* (added *Related products*). Updated titles of *Figure 3*, *Figure 4*, *Figure 6* to *Figure 13* (added conditions to differentiate them). Removed TS914IYD device from *Table 8*. Minor corrections throughout document.