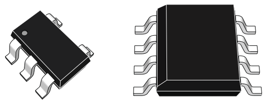
TSV91x, TSV91xA

Datasheet

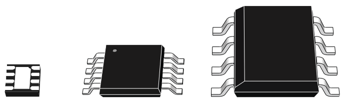
Single, dual, and quad rail-to-rail input/output 8 MHz operational amplifiers

TSV911



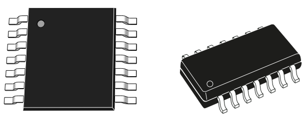
SOT23-5 SO8

TSV912



DFN8 2x2 MiniSO8 SO8

TSV914



TSSOP14 SO14

Product status link
TSV911, TSV911A, TSV912, TSV912A, TSV914, TSV914A

Related products	
See TSV991, TSV992, TSV994 and TSV991A, TSV992A, TSV994A	for higher speed

Features

- Rail-to-rail input and output
- Wide bandwidth
- Low power consumption: 820 μA typ.
- Unity gain stability
- High output current: 35 mA
- Operating from 2.5 V to 5.5 V
- Low input bias current, 1 pA typ.
- Low input offset voltage: 1.5 mV max. (A grade)
- ESD internal protection ≥ 5 kV
- Latch-up immunity

Applications

- Battery-powered applications
- Portable devices
- Signal conditioning
- Active filtering
- Medical instrumentation
- Automotive applications

Description

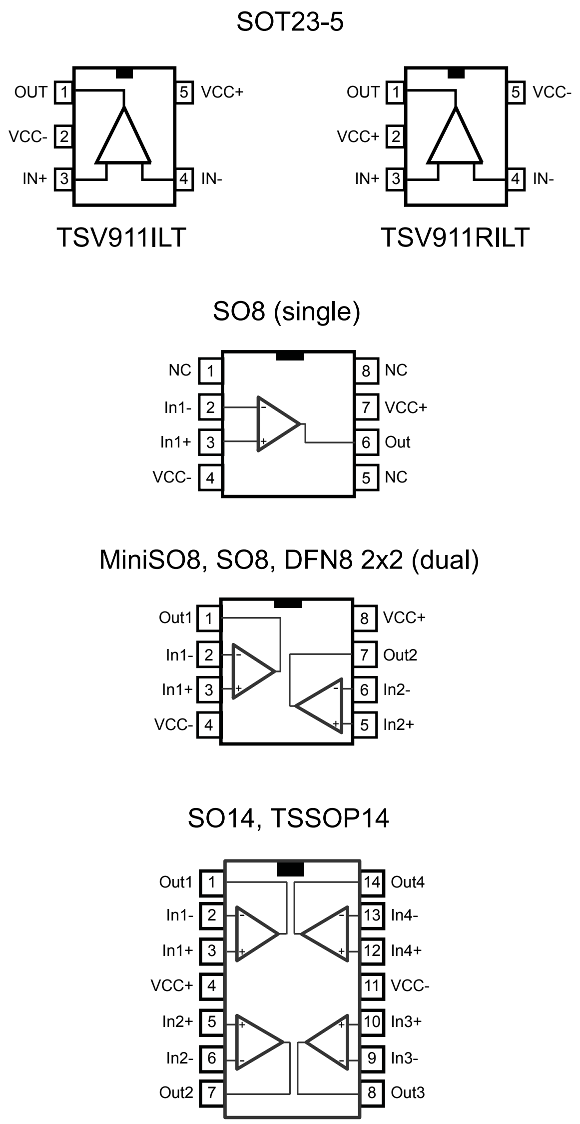
The TSV91x and TSV91xA operational amplifiers (op amps) offer low voltage operation and rail-to-rail input and output, as well as an excellent speed/power consumption ratio, providing an 8 MHz gain-bandwidth product while consuming only 1.1 mA maximum at 5 V. The op amps are unity gain stable and feature an ultra-low input bias current.

The devices are ideal for sensor interfaces, battery-supplied and portable applications, as well as active filtering.

DS4899 - Rev 12 - November 2019

1 Package pin connections

Figure 1. **Pin connections for each package (top view)**



1. The exposed pad of the DFN8 2x2 package is not internally connected and can be set to V_{CC}^{-} or left floating.

2 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings (AMR)

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage [1]		6	V
V_{id}	Differential input voltage [2]		$\pm V_{CC}$	
V_{in}	Input voltage [3]		$(V_{CC-}) - 0.2$ to $(V_{CC+}) + 0.2$	
I_{in}	Input current [4]		10	mA
T_{stg}	Storage temperature		-65 to 150	°C
T_j	Maximum junction temperature		150	
R_{thja}	Thermal resistance junction to ambient [5] [6]	SOT23-5	250	°C/W
		DFN8 2x2	57	
		SO8	125	
		MiniSO8	190	
		SO14	103	
		TSSOP14	100	
R_{thjc}	Thermal resistance junction to case [5] [6]	SOT23-5	81	
		SO8	40	
		MiniSO8	39	
		SO14	31	
		TSSOP14	32	
ESD	HBM: human body model [7]		5	kV
	MM: machine model [8]		400	V
	CDM: charged device model [9]	SOT23-5, SO8, MiniSO8	1500	
		TSSOP14	750	
		SO14	500	
	Latch-up immunity		200	mA

1. *All voltage values, except the differential voltage, are with respect to network ground terminal.*
2. *Differential voltages are the non-inverting input terminal with respect to the inverting input terminal*
3. V_{CC} - V_{IN} *must not exceed 6 V*
4. *Input current must be limited by a resistor in series with the inputs*
5. *Short-circuits can cause excessive heating and destructive dissipation.*
6. R_{th} *are typical values*
7. *Human body model: 100 pF discharged through a 1.5 kΩ resistor between two pins of the device, done for all couples of pin combinations with other pins floating.*
8. *Machine model: 200 pF charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω), done for all couples of pin combinations with other pins floating*
9. *Charged device model: all pins plus packages are charged together to the specified voltage and then discharged directly to the ground.*

Table 2. Operating conditions

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage	-40 °C < T_{op} < 125 °C	2.5 to 5.5	V
		0 °C < T_{op} < 125 °C	2.3 to 5.5	
V_{icm}	Common mode input voltage range		(V_{CC-}) - 0.1 to (V_{CC+}) + 0.1	
T_{op}	Operating free air temperature range		-40 to 125	°C

3 Electrical characteristics

Table 3. Electrical characteristics at V_{CC+} = 2.5 V, V_{CC-} = 0 V, V_{icm} = $V_{CC}/2$, with R_L connected to $V_{CC}/2$, T = 25 °C (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage, TSV91x	T_{op} = 25 °C		0.1	4.5	mV
		$T_{min} < T_{op} < T_{max}$			7.5	
	Offset voltage, TSV91xA	T_{op} = 25 °C			1.5	
		$T_{min} < T_{op} < T_{max}$			3	
$\Delta V_{io}/\Delta T$	Input offset voltage drift			5		µV/°C
I_{io}	Input offset current [1]	T_{op} = 25 °C		1	10	pA
		$T_{min} < T_{op} < T_{max}$			100	
I_{ib}	Input bias current [1]	T_{op} = 25 °C		1	10	
		$T_{min} < T_{op} < T_{max}$			100	
CMR	Common mode rejection ratio,20 log ($\Delta V_{ic}/\Delta V_{io}$)	0 V to 2.5 V, V_{out} = 1.25 V, T_{op} = 25 °C	58	75		dB
		$T_{min} < T_{op} < T_{max}$	53			
A_{vd}	Large signal voltage gain	R_L = 10 kΩ, V_{out} = 0.5 V to 2 V, T_{op} = 25 °C	80	89		
		$T_{min} < T_{op} < T_{max}$	75			
V_{CC} - V_{OH}	High-level output voltage	R_L = 10 kΩ		15	40	mV
		$T_{min} < T_{op} < T_{max}$			40	
		R_L = 600 Ω		45	150	
		$T_{min} < T_{op} < T_{max}$			150	
V_{OL}	Low-level output voltage	R_L = 10 kΩ		15	40	
		$T_{min} < T_{op} < T_{max}$			40	
		R_L = 600 Ω		45	150	
		$T_{min} < T_{op} < T_{max}$			150	
I_{out}	I_{sink}	V_o = 2.5 V, T_{op} = 25 °C	18	32		mA
		$T_{min} < T_{op} < T_{max}$	16			
	I_{source}	V_o = 0 V, T_{op} = 25 °C	18	35		
		$T_{min} < T_{op} < T_{max}$	16			
I_{CC}	Supply current (per channel)	No load, V_{out} = $V_{CC}/2$		0.78	1.1	
		$T_{min} < T_{op} < T_{max}$			1.1	
AC performance						
GBP	Gain bandwidth product	R_L = 2 kΩ, C_L = 100 pF, f = 100 kHz, T_{op} = 25 °C		8		MHz
F_u	Unity gain frequency	R_L = 2 kΩ, C_L = 100 pF, T_{op} = 25 °C		7.2		
ϕm	Phase margin	R_L = 2 kΩ, C_L = 100 pF, T_{op} = 25 °C		45		Degrees

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
G_m	Gain margin	R_L = 2 kΩ, C_L = 100 pF, T_{op} = 25 °C		8		dB
SR	Slew rate	R_L = 2 kΩ, C_L = 100 pF, A_v = 1, T_{op} = 25 °C		4.5		V/μs
e_n	Equivalent input noise voltage	f = 10 kHz, T_{op} = 25 °C		21		nV/√Hz
THD+e_n	Total harmonic distortion	G = 1, f = 1 kHz, R_L = 2 kΩ, BW = 22 kHz, T_{op} = 25 °C, V_{icm} = (V_{CC} + 1)/2, V_{out} = 1.1 V_{pp}		0.001		%

1. *Guaranteed by design*

Table 4. **Electrical characteristics at V_{CC+} = 3.3 V, V_{CC-} = 0 V, V_{icm} = V_{CC}/2, with R_L connected to V_{CC}/2, T = 25 °C (unless otherwise specified)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage, TSV91x	T_{op} = 25 °C		0.1	4.5	mV
		T_{min} < T_{op} < T_{max}			7.5	
	Offset voltage, TSV91xA	T_{op} = 25 °C			1.5	
		T_{min} < T_{op} < T_{max}			3	
$\Delta V_{io}/\Delta T$	Input offset voltage drift			5		μV/°C
I_{io}	Input offset current (1)	T_{op} = 25 °C		1	10	pA
		T_{min} < T_{op} < T_{max}			100	
I_{ib}	Input bias current (1)	T_{op} = 25 °C		1	10	
		T_{min} < T_{op} < T_{max}			100	
CMR	Common mode rejection ratio, 20 log ($\Delta V_{ic}/\Delta V_{io}$)	0 V to 3.3 V, V_{out} = 1.65 V, T_{op} = 25 °C	60	78		dB
		T_{min} < T_{op} < T_{max}	55			
A_{vd}	Large signal voltage gain	R_L = 10 kΩ, V_{out} = 0.5 V to 2.8 V, T_{op} = 25 °C	80	89		
		T_{min} < T_{op} < T_{max}	75			
V_{CC} - V_{OH}	High-level output voltage	R_L = 10 kΩ		15	40	mV
		T_{min} < T_{op} < T_{max}			40	
		R_L = 600 Ω		45	150	
		T_{min} < T_{op} < T_{max}			150	
V_{OL}	Low-level output voltage	R_L = 10 kΩ		15	40	
		T_{min} < T_{op} < T_{max}			40	
		R_L = 600 Ω		45	150	
		T_{min} < T_{op} < T_{max}			150	
I_{out}	I_{sink}	V_o = 3.3 V, T_{op} = 25 °C	18	32		mA
		T_{min} < T_{op} < T_{max}	16			
	I_{source}	V_o = 0 V, T_{op} = 25 °C	18	35		
		T_{min} < T_{op} < T_{max}	16			
I_{CC}	Supply current (per channel)	No load, V_{out} = V_{CC}/2		0.8	1.1	
		T_{min} < T_{op} < T_{max}			1.1	
AC performance						
GBP	Gain bandwidth product	R_L = 2 kΩ, C_L = 100 pF, f = 100 kHz, T_{op} = 25 °C		8		MHz
F_u	Unity gain frequency	R_L = 2 kΩ, C_L = 100 pF, T_{op} = 25 °C		7.2		
ϕm	Phase margin	R_L = 2 kΩ, C_L = 100 pF, T_{op} = 25 °C		45		Degrees
G_m	Gain margin	R_L = 2 kΩ, C_L = 100 pF, T_{op} = 25 °C		8		dB

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SR	Slew rate	R_L = 2 kΩ, C_L = 100 pF, A_v = 1, T_{op} = 25 °C		4.5		V/μs
e_n	Equivalent input noise voltage	f = 10 kHz, T_{op} = 25 °C		21		nV/√Hz
THD+e_n	Total harmonic distortion	G = 1, f = 1 kHz, R_L = 2 kΩ, BW = 22 kHz, T_{op} = 25 °C, V_{icm} = (V_{CC} + 1)/2, V_{out} = 1.9 V_{pp}		0.0007		%

1. Guaranteed by design

Table 5. **Electrical characteristics at V_{CC+} = 5 V, V_{CC-} = 0 V, V_{icm} = V_{CC}/2, with R_L connected to V_{CC}/2, T = 25 °C (unless otherwise specified)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage, TSV91x	T_{op} = 25 °C		0.1	4.5	mV
		T_{min} < T_{op} < T_{max}			7.5	
	Offset voltage, TSV91xA	T_{op} = 25 °C			1.5	
		T_{min} < T_{op} < T_{max}			3	
$\Delta V_{io}/\Delta T$	Input offset voltage drift			5		μV/°C
I_{io}	Input offset current (1)	T_{op} = 25 °C		1	10	pA
		T_{min} < T_{op} < T_{max}			100	
I_{ib}	Input bias current (1)	T_{op} = 25 °C		1	10	
		T_{min} < T_{op} < T_{max}			100	
CMR	Common mode rejection ratio, 20 log ($\Delta V_{ic}/\Delta V_{io}$)	0 V to 5 V, V_{out} = 2.5 V, T_{op} = 25 °C	62	82		dB
		T_{min} < T_{op} < T_{max}	58			
SVR	Supply voltage rejection ratio, 20 log ($\Delta V_{CC}/\Delta V_{io}$)	V_{CC} = 2.5 to 5 V	70	86		
A_{vd}	Large signal voltage gain	R_L = 10 kΩ, V_{out} = 0.5 V to 4.5 V, T_{op} = 25 °C	80	91		
		T_{min} < T_{op} < T_{max}	75			
V_{CC} - V_{OH}	High-level output voltage	R_L = 10 kΩ		15	40	mV
		T_{min} < T_{op} < T_{max}			40	
		R_L = 600 Ω		45	150	
		T_{min} < T_{op} < T_{max}			150	
V_{OL}	Low-level output voltage	R_L = 10 kΩ		15	40	
		T_{min} < T_{op} < T_{max}			40	
		R_L = 600 Ω		45	150	
		T_{min} < T_{op} < T_{max}			150	
I_{out}	I_{sink}	V_o = 5 V, T_{op} = 25 °C	18	32		mA
		T_{min} < T_{op} < T_{max}	16			
	I_{source}	V_o = 0 V, T_{op} = 25 °C	18	35		
		T_{min} < T_{op} < T_{max}	16			
I_{CC}	Supply current (per channel)	No load, V_{out} = 2.5 V		0.78	1.1	
		T_{min} < T_{op} < T_{max}			1.1	
AC performance						
GBP	Gain bandwidth product	R_L = 2 kΩ, C_L = 100 pF, f = 100 kHz, T_{op} = 25 °C		8		MHz
F_u	Unity gain frequency	R_L = 2 kΩ, C_L = 100 pF, T_{op} = 25 °C		7.5		
ϕm	Phase margin	R_L = 2 kΩ, C_L = 100 pF, T_{op} = 25 °C		45		Degrees
G_m	Gain margin	R_L = 2 kΩ, C_L = 100 pF, T_{op} = 25 °C		8		dB

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SR	Slew rate	R_L = 2 kΩ, C_L = 100 pF, A_v = 1, T_{op} = 25 °C		4.5		V/μs
e_n	Equivalent input noise voltage	f = 1 kHz, T_{op} = 25 °C		27		nV/√Hz
		f = 10 kHz, T_{op} = 25 °C		21		
THD+e_n	Total harmonic distortion	G = 1, f = 1 kHz, R_L = 2 kΩ, BW = 22 kHz, T_{op} = 25 °C, V_{icm} = (V_{CC} + 1)/2, V_{out} = 3.6 V_{pp}		0.0004		%

1. Guaranteed by design

4 Electrical characteristic curves

Figure 2. Input offset voltage distribution at T = 25 °C

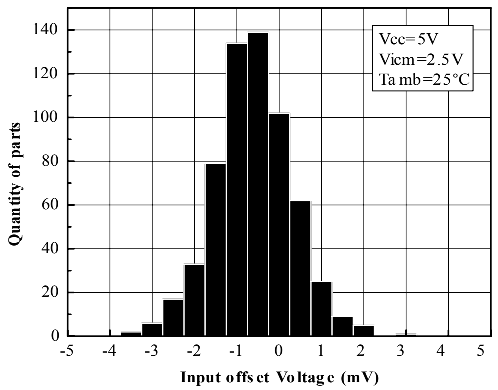


Figure 3. Input offset voltage distribution at T = 125 °C

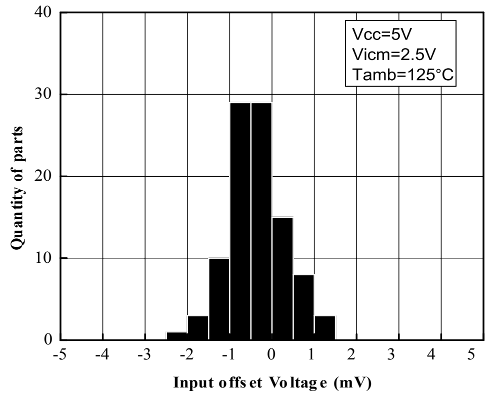


Figure 4. Supply current vs. input common-mode voltage at V_{CC} = 2.5 V

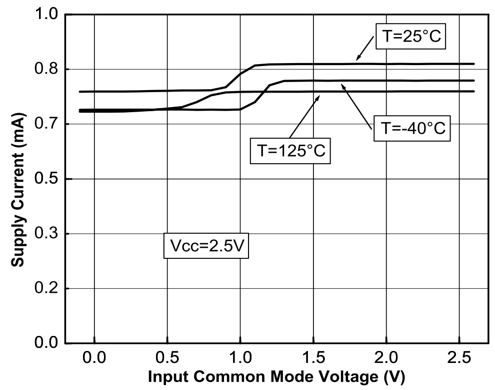


Figure 5. Supply current vs. input common-mode voltage at V_{CC} = 5 V

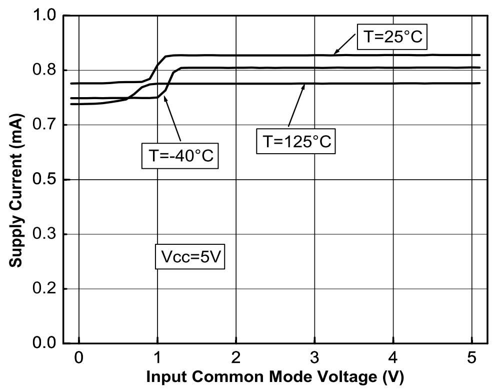


Figure 6. Output current vs. output voltage at V_{CC} = 2.5 V

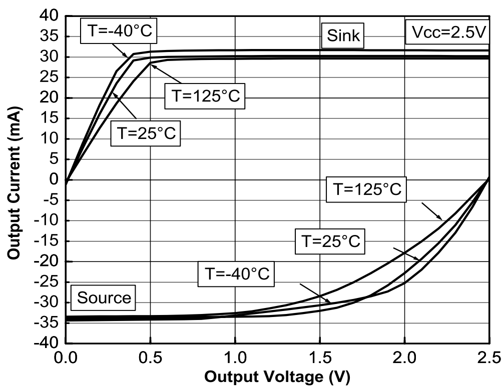


Figure 7. Output current vs. output voltage at V_{CC} = 5 V

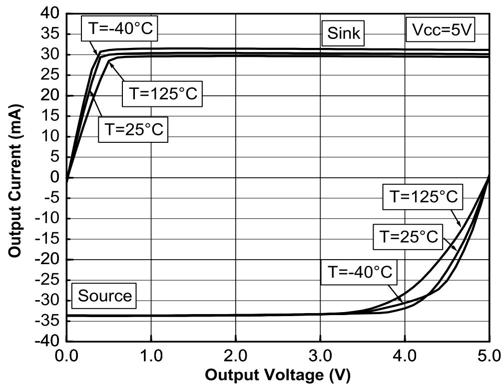


Figure 8. Voltage gain and phase vs. frequency at V_{CC} = 2.5 V and V_{icm} = 0.5 V

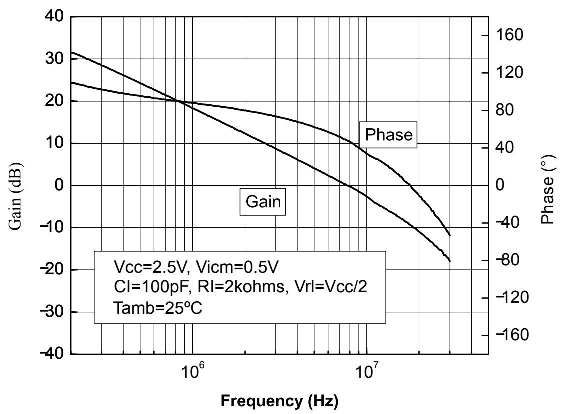


Figure 9. Voltage gain and phase vs. frequency at V_{CC} = 5.5 V and V_{icm} = 0.5 V

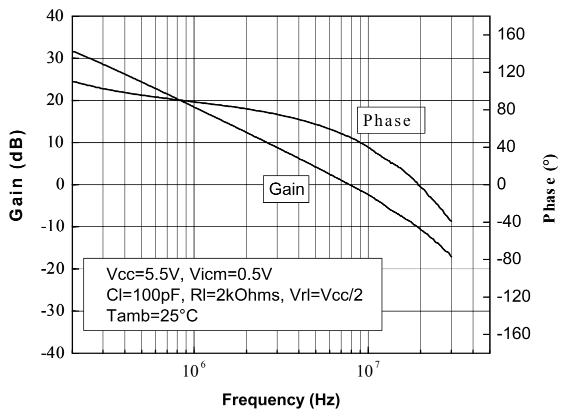


Figure 10. Phase margin vs. capacitive load

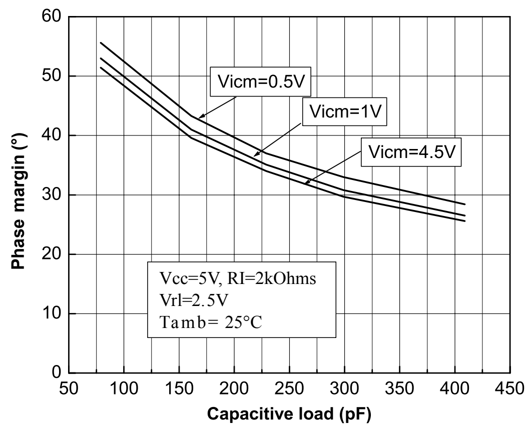


Figure 11. Phase margin vs. output current

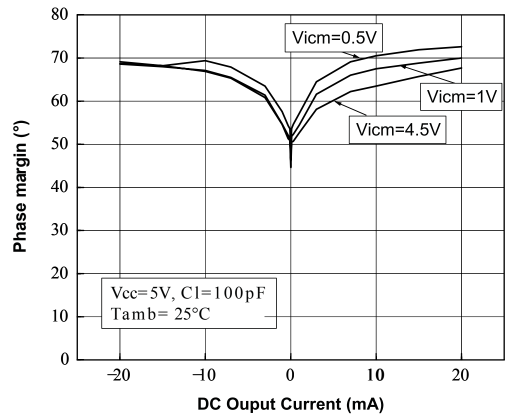


Figure 12. Positive slew rate

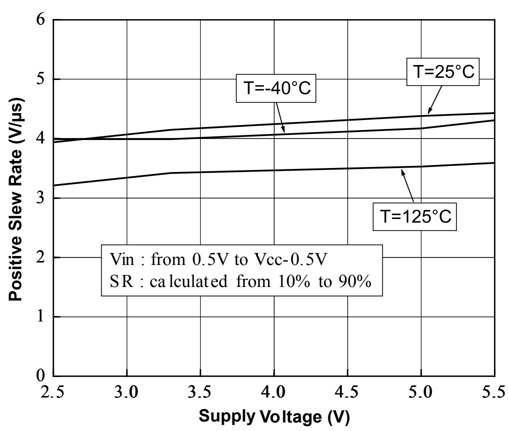


Figure 13. Negative slew rate

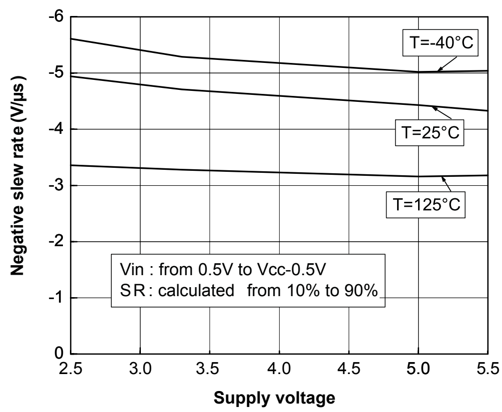


Figure 14. Distortion + noise vs. frequency

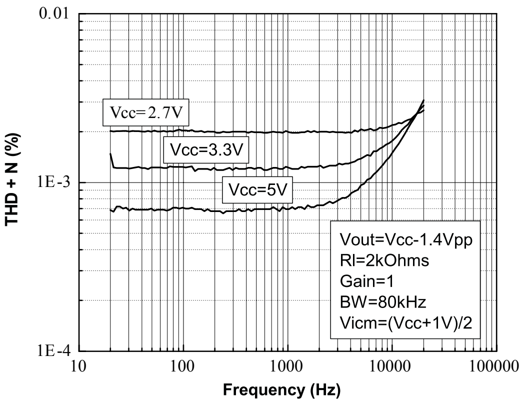


Figure 15. Distortion + noise vs. output voltage

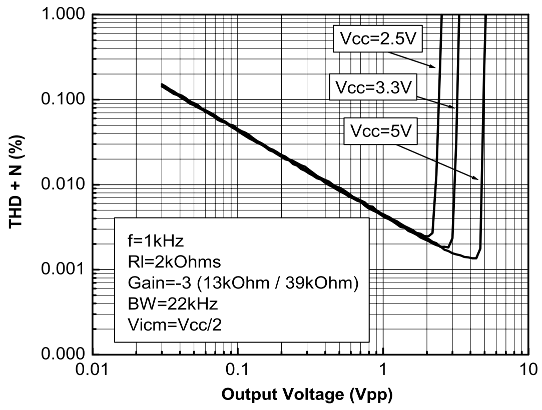


Figure 16. Noise vs. frequency

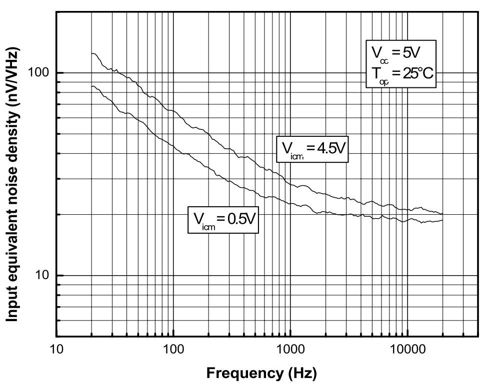


Figure 17. Phase margin vs. capacitive load and serial resistor

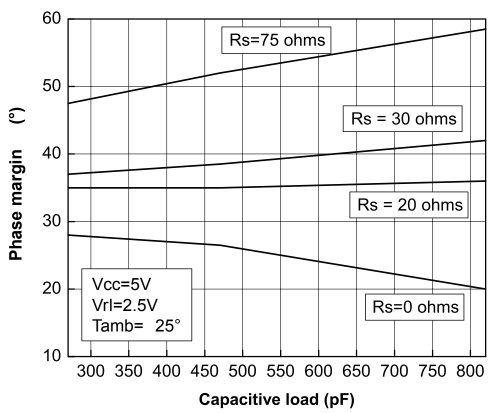
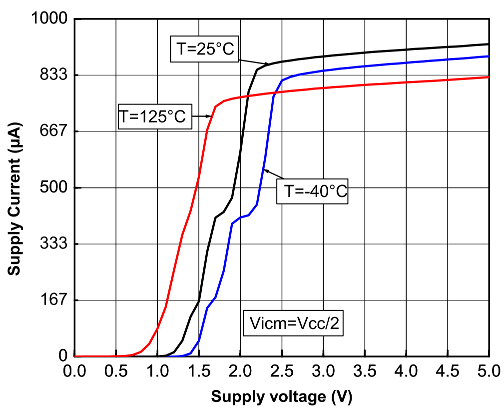


Figure 18. Supply current vs. supply voltage



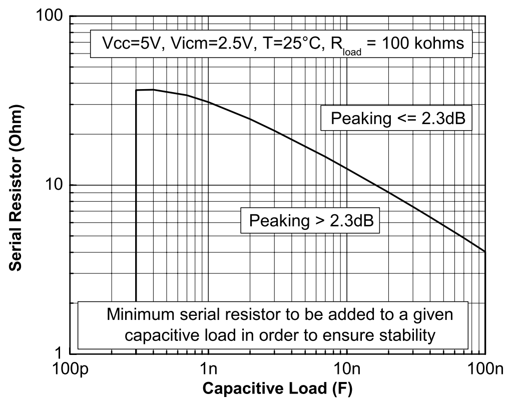
5 Application information

5.1 Driving resistive and capacitive loads

These products are low-voltage, low-power operational amplifiers optimized to drive rather large resistive loads above 2 kΩ.

In a *follower* configuration, these operational amplifiers can drive capacitive loads up to 100 pF with no oscillations. When driving larger capacitive loads, adding a small in-series resistor at the output can improve the stability of the device (figure below shows the recommended in-series resistor values). Once the in-series resistor value has been selected, the stability of the circuit should be tested on bench and simulated with the simulation model.

Figure 19. In-series resistor vs. capacitive load



5.2 PCB layouts

For correct operation, it is advised to add 10 nF decoupling capacitors as close as possible to the power supply pins.

5.3 Macromodel

An accurate macromodel of the TSV91x is available on STMicroelectronics' web site at: ***www.st.com*** . This model is a trade-off between accuracy and complexity (that is, time simulation) of the TSV91x operational amplifiers. It emulates the nominal performances of a typical device within the specified operating conditions mentioned in the datasheet. It helps to validate a design approach and to select the right operational amplifier, *but it does not* replace on-board measurements.

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 SOT23-5 package information

Figure 20. SOT23-5 package outline

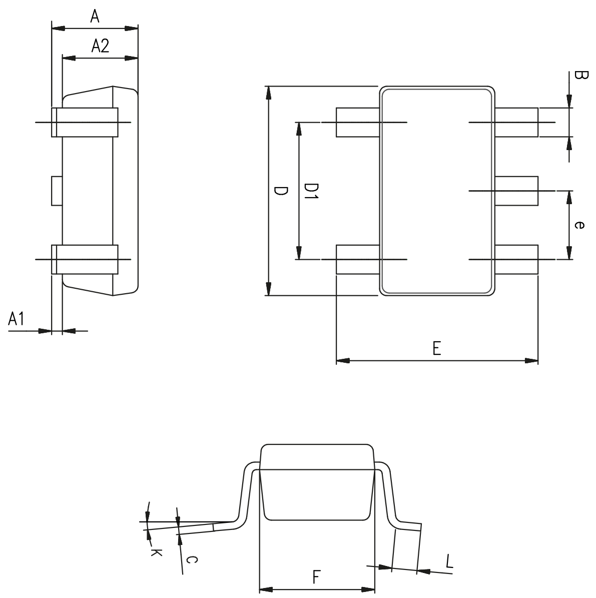


Table 6. SOT23-5 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90	1.20	1.45	0.035	0.047	0.057
A1			0.15			0.006
A2	0.90	1.05	1.30	0.035	0.041	0.051
B	0.35	0.40	0.50	0.014	0.016	0.020
C	0.09	0.15	0.20	0.004	0.006	0.008
D	2.80	2.90	3.00	0.110	0.114	0.118
D1		1.90			0.075	
e		0.95			0.037	
E	2.60	2.80	3.00	0.102	0.110	0.118
F	1.50	1.60	1.75	0.059	0.063	0.069
L	0.10	0.35	0.60	0.004	0.014	0.024
K	0 degrees		10 degrees	0 degrees		10 degrees

6.2 DFN8 2 x 2 package information

Figure 21. DFN8 2 x 2 package outline

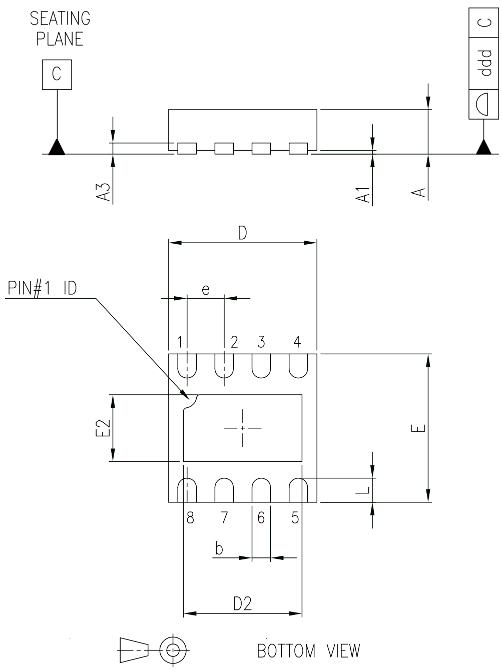
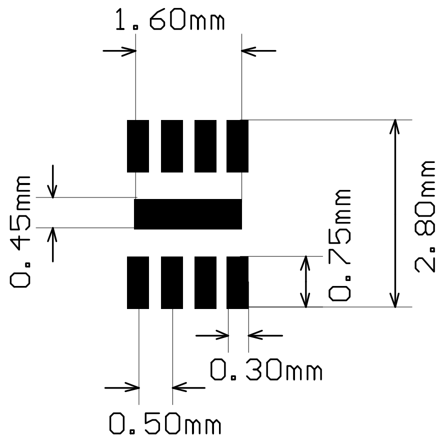


Table 7. DFN8 2 x 2 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.51	0.55	0.60	0.020	0.022	0.024
A1			0.05			0.002
A3		0.15			0.006	
b	0.18	0.25	0.30	0.007	0.010	0.012
D	1.85	2.00	2.15	0.073	0.079	0.085
D2	1.45	1.60	1.70	0.057	0.063	0.067
E	1.85	2.00	2.15	0.073	0.079	0.085
E2	0.75	0.90	1.00	0.030	0.035	0.039
e		0.50			0.020	
L			0.425			0.017
ddd			0.08			0.003

Figure 22. **DFN8 2 x 2 recommended footprint**



Note: *The exposed pad of the DFN8 2x2 package is not internally connected. It can be set to V_{CC}^- or left floating.*

6.3 MiniSO8 package information

Figure 23. MiniSO8 package outline

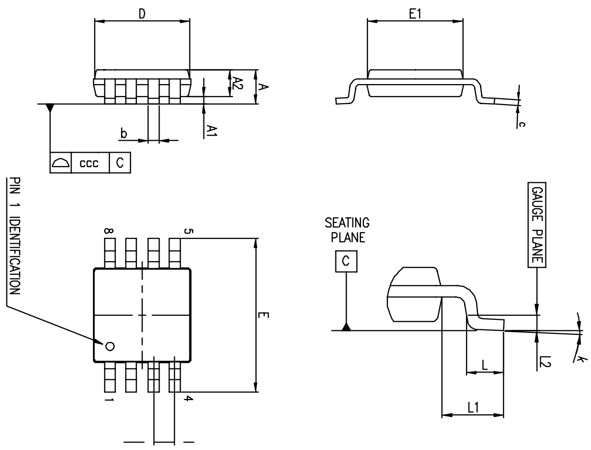


Table 8. MiniSO8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.0006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.22		0.40	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.80	3.00	3.20	0.11	0.118	0.126
E	4.65	4.90	5.15	0.183	0.193	0.203
E1	2.80	3.00	3.10	0.11	0.118	0.122
e		0.65			0.026	
L	0.40	0.60	0.80	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.010	
k	0°		8°	0°		8°
ccc			0.10			0.004

6.4 SO8 package information

Figure 24. SO8 package outline

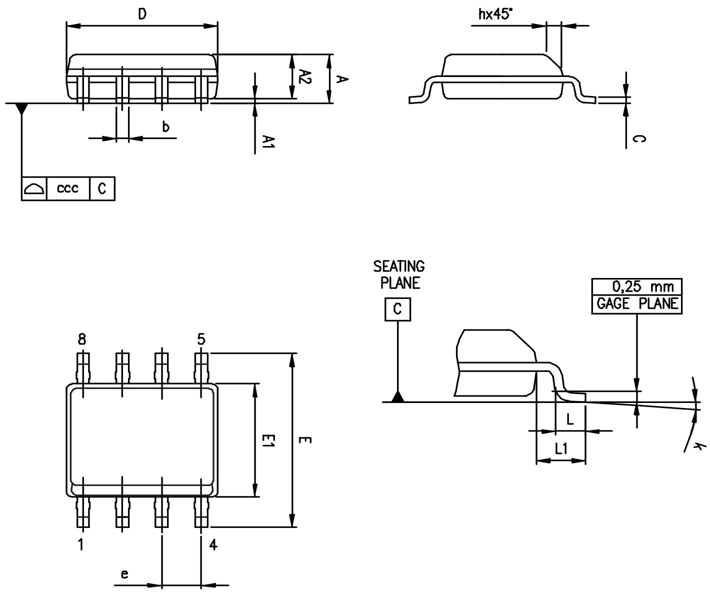


Table 9. SO8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
L1		1.04			0.040	
k	0°		8°	0°		8°
ccc			0.10			0.004

6.5 TSSOP14 package information

Figure 25. **TSSOP14 package outline**

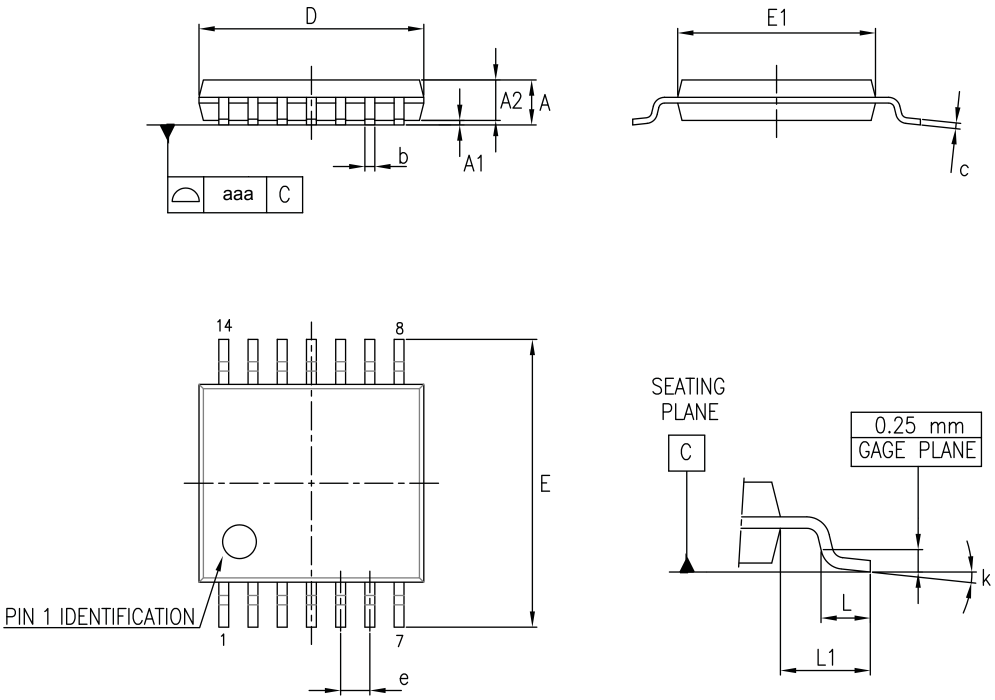


Table 10. **TSSOP14 package mechanical data**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.20			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.90	5.00	5.10	0.193	0.197	0.201
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.176
e		0.65			0.0256	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
k	0°		8°	0°		8°
aaa			0.10			0.004

6.6 SO14 package information

Figure 26. SO14 package outline

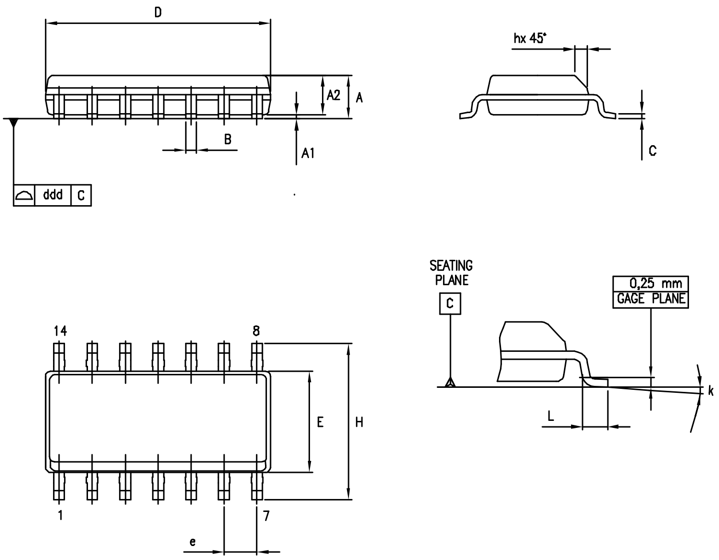


Table 11. SO14 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
			1.75			0.069
A	1.35		1.75	0.05		0.068
A1	0.10		0.25	0.004		0.009
A2	1.10		1.65	0.04		0.06
B	0.33		0.51	0.01		0.02
C	0.19		0.25	0.007		0.009
D	8.55		8.75	0.33		0.34
E	3.80		4.0	0.15		0.15
e		1.27			0.05	
H	5.80		6.20	0.22		0.24
h	0.25		0.50	0.009		0.02
L	0.40		1.27	0.015		0.05
k	8° (max.)					
ddd			0.10			0.004

7 Ordering information

Table 12. Order codes

Order code	Temperature range	Package	Packing	Marking
TSV911IDT	-40 °C to 125 °C	SO8	Tape and reel	V911I
TSV911AIDT				V911AI
TSV911ILT		SOT23-5		K127
TSV911AILT				K128
TSV911RILT				K125
TSV912IST		MiniSO8		K125
TSV912AIST				K126
TSV912IDT		SO8		V912I
TSV912AIDT				V912AI
TSV912IQ2T		DFN8 2x2		K1Q
TSV914IPT		TSSOP14		V914I
TSV914AIPT				V914AI
TSV914IDT		SO14		V914I
TSV914AIDT				V914AI
TSV911IYLT [(1)]		SOT23-5, automotive grade		K147
TSV911AIYLT [(1)]				K148
TSV911IYDT [(1)]		SO-8, automotive grade		V911IY
TSV911AIYDT [(1)]				V911AIY
TSV912IYDT [(1)]				V912IY
TSV912AIYDT [(1)]				V912AIY
TSV912IYST [(1)]		MiniSO8, automotive grade		K147
TSV912AIYST [(1)]				K148
TSV914IYDT [(1)]		SO14, automotive grade		V914IY
TSV914AIYDT [(1)]				V914AIY
TSV914IYPT [(1)]		TSSOP14, automotive grade		V914IY
TSV914AIYPT [(1)]				V914AIY

1. *Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q 002 or equivalent.*

Revision history

Table 13. Document revision history

Date	Revision	Changes
28-Aug-2006	1	First release.
07-Jun-2007	2	Modified ESD CDM parameter for SO-14 package in Table 2: Absolute maximum ratings. Noise parameters updated in Section 2: Electrical characteristics. Added limits in temperature in Section 2: Electrical characteristics. Added automotive grade level description in Table 13: Order codes. Added footnote about SO-14 package in Table 13: Order codes. Added Figure 16: Phase margin vs. capacitive load and serial resistor.
11-Feb-2008	3	Updated footnotes for ESD parameters in Table 2: Absolute maximum ratings. Corrected MiniSO-8 package information in Table 9: MiniSO-8 package mechanical data. Added missing markings for order codes TSV911AILT and TSV912AILT in Table 13: Order codes.
22-Jun-2009	4	Added input current information in Table 2: Absolute maximum ratings. Changed Figure 7 and Figure 8. Added Chapter 3: Application information. Updated package information in Chapter 4. Added automotive order codes: TSV911IYLT, TSV911AIYLT, TSV912IYST, TSV912AIYST, TSV914IYPT and TSV914AIYPT in Table 13: Order codes.
17-Sep-2009	5	Added A versions of devices in title on cover page. Modified ESD value for machine model in Table 2: Absolute maximum ratings. Added Figure 17: Supply current vs. supply voltage on page 10.
18-Mar-2010	6	Added TSV911RILT in Table 13: Order codes, housed in a SOT23-5 package with a new pinout.
24-Jun-2010	7	Added pin connections for TSV911ILT and TSV91RILT on cover page. Added Table 1: Device summary on cover page. Modified supply voltage value in Table 3. Corrected typical value of DV_{io} in Table 4, Table 5 and Table 6. Added TSV911RILT, TSV911IYDT and TSV911AIYDT order codes in Table 13. Modified Note 2 under Table 13.

Date	Revision	Changes
06-Mar-2012	8	Added DFN8 2x2 package and ordering information for TSV912 device to Chapter 4 and Chapter 5.
27-Nov-2015	9	Updated layout Section 2: replaced DV_{io}/DT by $\Delta V_{io}/\Delta T$. Section 5.2: updated name of package and title of drawings and table; added note about exposed pad. Table 13: "Order codes": removed obsolete order codes (TSV911ID, TSV911AID, TSV912ID, TSV912AID, TSV914ID, TSV914AID).
29-Aug-2016	10	Added silhouettes of packages to cover page Placed pinout diagrams in Section 2: "Package pin connections" Added Related products Description: added footnote 1 Section 7.2: "DFN8 2 x 2 package information": modified note about the exposed pad. Section 8: "Ordering information": removed note regarding "moisture sensitivity level 1"
10-Oct-2019	11	Updated Table 12. Order codes.
20-Nov-2019	12	Updated cover page.

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