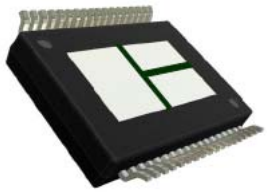
VNH9013Y

Automotive integrated H-bridge

Datasheet - production data



PowerSSO-36 TP

Features

Type	$R_{DS(on)}$	I_{out}	V_{ccmax}
VNH9013Y	13 mΩ typ (per leg)	40(1)	80 V(2)

1. Max current to be set according to the wires capability
2. Per leg: sum of the two BV_{dss} (HSD + LSD); V_{CC} > 40 V whole bridge must be switched off;

- AEC-Q100 qualified
- Maximum V_{CC} voltage: 80 V
- 10 V compatible inputs
- $R_{DS(on)}$ per leg: 13 mΩ typical
- Embedded thermal sensor: -8.1 mV/°K
- Very low stray inductance in power line

Description

The device is an automotive integrated H-bridge intended for a wide range of automotive applications driving DC motors. The device incorporates a dual channel and two single channel MOSFETs. The device is designed using STMicroelectronics® well known and proven proprietary VIPower® M0-S9 technology that allows to integrate in a package four different channels in H-bridge topology.

This package, specifically designed for the harsh automotive environment offers improved thermal performance thanks to exposed die pads. Moreover, its fully symmetrical mechanical design allows superior manufacturability at board level.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
PowerSSO-36 TP	VNH9013Y	VNH9013YTR

Contents

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1 Block diagram and pin description

Figure 1. Block diagram

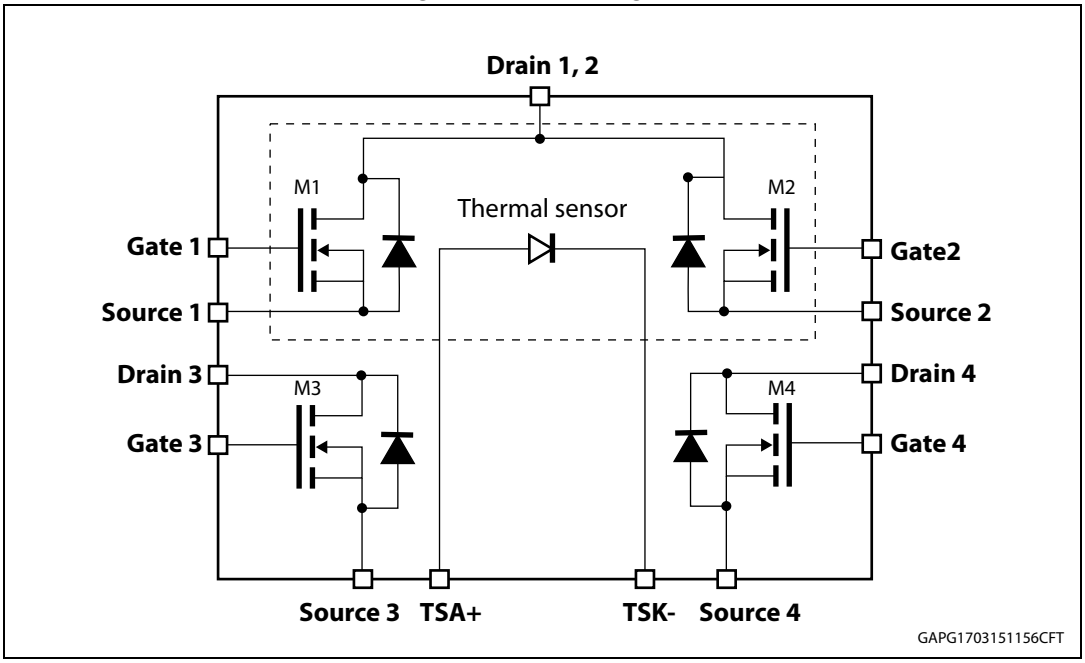


Figure 2. Configuration diagram

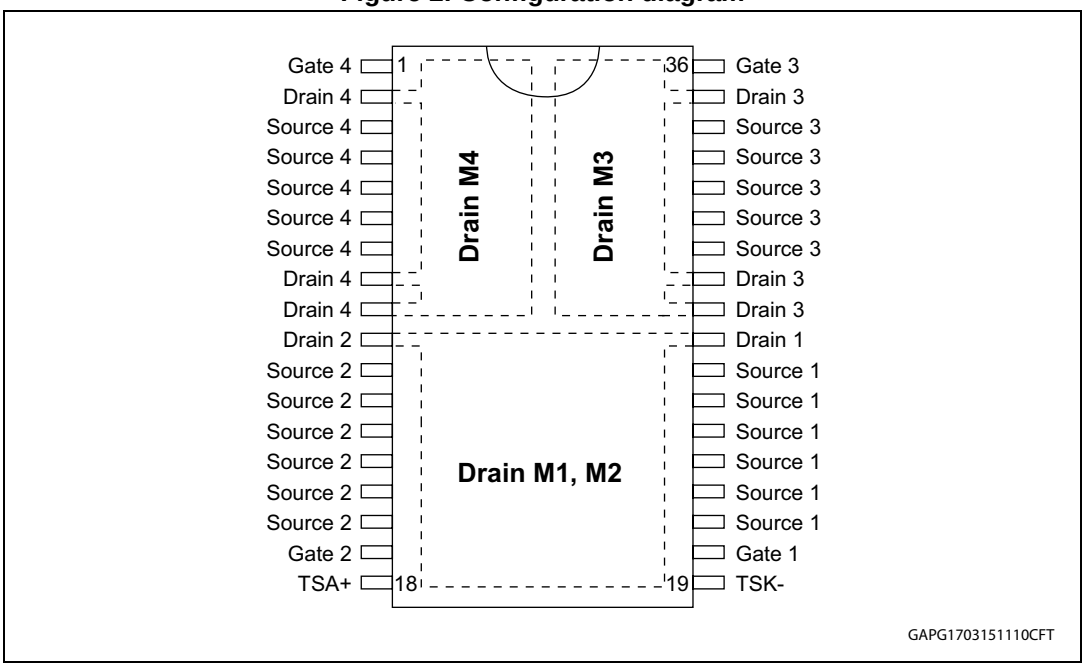


Table 2. Pin definitions and functions

Pin number	Symbol	Function
1	Gate 4	Gate of the LSD 4
2, 8, 9	Drain 4	Drain of the LSD 4
3, 4, 5, 6, 7	Source 4	Source of the LSD 4
10	Drain 2	Drain of the HSD 2
11, 12, 13, 14, 15, 16	Source 2	Source of the HSD 2
17	Gate 2	Gate of the HSD 2
18	TSA+	Thermal sensor anode
19	TSK-	Thermal sensor cathode
20	Gate 1	Gate of the HSD 1
21, 22, 23, 24, 25, 26	Source 1	Source of the HSD 1
27	Drain 1	Drain of the HSD 1
28, 29, 35	Drain 3	Drain of the LSD 3
30, 31, 32, 33, 34	Source 3	Source of the LSD 3
36	Gate 3	Gate of the LSD 3

2 Electrical specifications

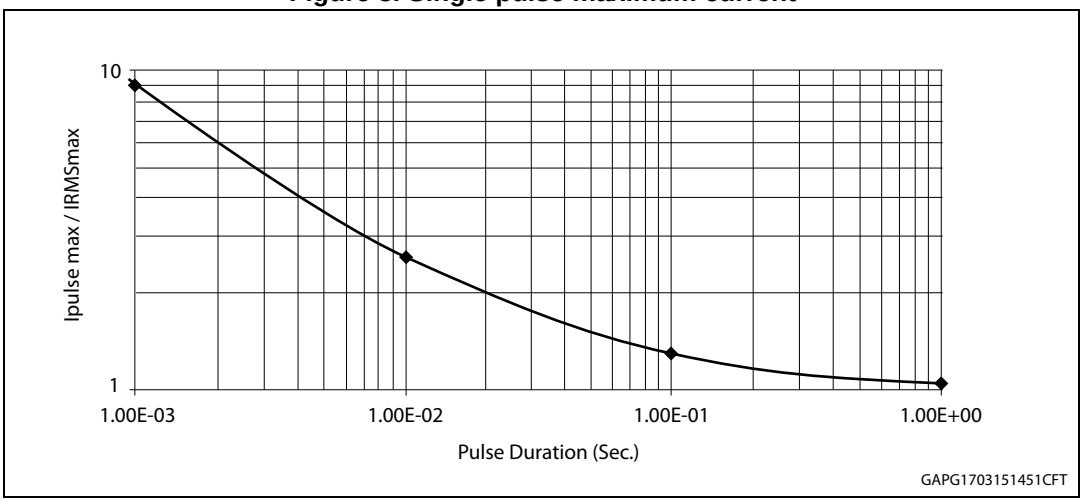
2.1 Absolute maximum rating

Table 3. Absolute maximum rating

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (whole bridge switched off)	80	V
I_{max}	Maximum output current (continuous) at T_C = 150 °C	40	A
V_{GS_max}	Maximum gate source voltage	18	V
I_{Pulse_max}	Maximum Single Pulse output current	80(1)	A
V_{ESD}	Electrostatic discharge HBM (JDEC 22 A-114 F) – DRAIN HS – DRAIN LS – GATE HS – GATE LS – K+ – K-	 4000 4000 1000 1000 750 750	V
T_j	Junction operating temperature	175	°C
T_c	Case operating temperature	-40 to 150	°C
T_{STG}	Storage temperature	-55 to 150	°C
I_S	Diode continuous forward current	TBD	A

1. Pulse duration = 20 ms (see *Figure 3*).

Figure 3. Single pulse maximum current



2.2 Electrical characteristics

Values specified in this section are for V_{CC} = 7 V up to 28 V; -40 °C < T_j < 150 °C, typical values are referred to T_j = 25 °C, unless otherwise specified.

Table 4. Power off

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage for HSD and LSDs	I_D = 10 mA; V_{GS} = 0 V	40	—		V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0 V)	V_{DS} = 28 V; -40 °C < T_j < 150 °C		—	100	µA
		V_{DS} = 28 V; T_j = 25 °C		—	10	µA
I_{GSS}	Gate-source leakage current (V_{DS} = 0 V)	V_{GS} = ±10 V; T_j = 25 °C		—	±100	nA

Table 5. Power on

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA; T_j = 25 °C	2		4	V
$dV_{GS(th)}/dT$ (1)	Gate threshold voltage temperature derating	V_{DS} = V_{GS}; I_D = 1 mA		-5.8		mV/°C
$R_{DS(on)\_HS}$	Static drain-source on resistance	V_{GS} = 10 V; I_D = 6 A; T_j = 25 °C		6.0		mΩ
		V_{GS} = 10 V; I_D = 6 A; T_j = 150 °C			11.3	mΩ
$R_{DS(on)\_LS}$	Static drain-source on resistance	V_{GS} = 10 V; I_D = 6 A; T_j = 25 °C		7.8		mΩ
		V_{GS} = 10 V; I_D = 6 A; T_j = 150 °C			15.3	mΩ

1. Guaranteed by design.

Table 6. Dynamic

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
C_{iss_HS}	Input capacitance	V_{DS} = 25 V; f = 1 MHz; V_{GS} = 0 V	—	2600	—	pF
C_{oss_HS}	Output capacitance		—	383	—	pF
C_{rss_HS}	Reverse transfer capacitance		—	165	—	pF
C_{iss_LS}	Input capacitance	V_{DS} = 25 V; f = 1 MHz; V_{GS} = 0 V	—	1750	—	pF
C_{oss_LS}	Output capacitance		—	257	—	pF
C_{rss_LS}	Reverse transfer capacitance		—	125	—	pF

Note: Parameters in Table 6 are guaranteed by design.

Table 7. Gate resistance

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
R_{G_HS}	Gate resistance HS	V_{DD} = 15 V; f_{gate} = 1 MHz	—	7	—	Ω
R_{G_LS}	Gate resistance LS		—	4.7	—	Ω

Note: Parameters in *Table 7* are guaranteed by design.

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD} (1)	Forward on voltage	I_{SD} = 6 A; V_{GS} = 0 V; T_j = 25 °C	—	0.75	1.1	V
t_{rr} (2)	Reverse recovery time	I_{SD} = 6 A; di/dt = 100 A/µs; V_{DD} = 15 V; T_j = 25 °C (see *Figure 5*)	—	40		ns
Q_{rr} (3)	Reverse recovery charge		—	20		nC
I_{RRM} (2)	Reverse recovery current		—	1		A

1. Pulse width limited by safe operating area.
2. Guaranteed by design.
3. Parameters guaranteed by design.

Table 9. Switching on HSD

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn on delay time	V_{DD} = 15 V; I_D = 6 A; R_G = 4.7 Ω; V_{GS} = 10 V	—	44	—	ns
t_r	Rise time		—	85	—	ns
Q_g (1)	Total gate charge	V_{DD} = 15 V; I_D = 6 A; V_{GS} = 10 V (see *Figure 4*)	—	45	—	nC
Q_{gs} (1)	Gate-source charge		—	8	—	nC
Q_{gd} (1)	Gate-drain charge		—	8	—	nC

1. Parameters guaranteed by design.

Table 10. Switching on LSD

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn on delay time	V_{DD} = 15 V; I_D = 6 A; R_G = 4.7 Ω; V_{GS} = 10 V	—	40	—	ns
t_r	Rise time		—	100	—	ns
Q_g (1)	Total gate charge	V_{DD} = 15 V; I_D = 6 A; V_{GS} = 10 V (see *Figure 4*)	—	40	—	nC
Q_{gs} (1)	Gate-source charge		—	4.9	—	nC
Q_{gd} (1)	Gate-drain charge		—	6.2	—	nC

1. Parameters guaranteed by design.

Table 11. Switching off HSD

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off delay time	V_{DD} = 15 V; I_D = 6 A; R_G = 4.7 Ω; V_{GS} = 10 V (see *Figure 6*)	—	114	—	ns
t_f	Fall time		—	27	—	ns

Table 12. Switching off LSD

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off delay time	V_{DD} = 15 V; I_D = 6 A; R_G = 4.7 Ω; V_{GS} = 10 V (see *Figure 6*)	—	83	—	ns
t_f	Fall time		—	25	—	ns

Table 13. Thermal sensor

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_F	Chain diode forward voltage	T_j = 25 °C; I_F = 250 µA	680	720	760	mV
S_F(1)	Chain temperature coefficient	-40 °C < T_j < 175 °C; I_F = 250 µA		-2		mV/°K

1. Parameters guaranteed by design.

Figure 4. Gate charge test circuit

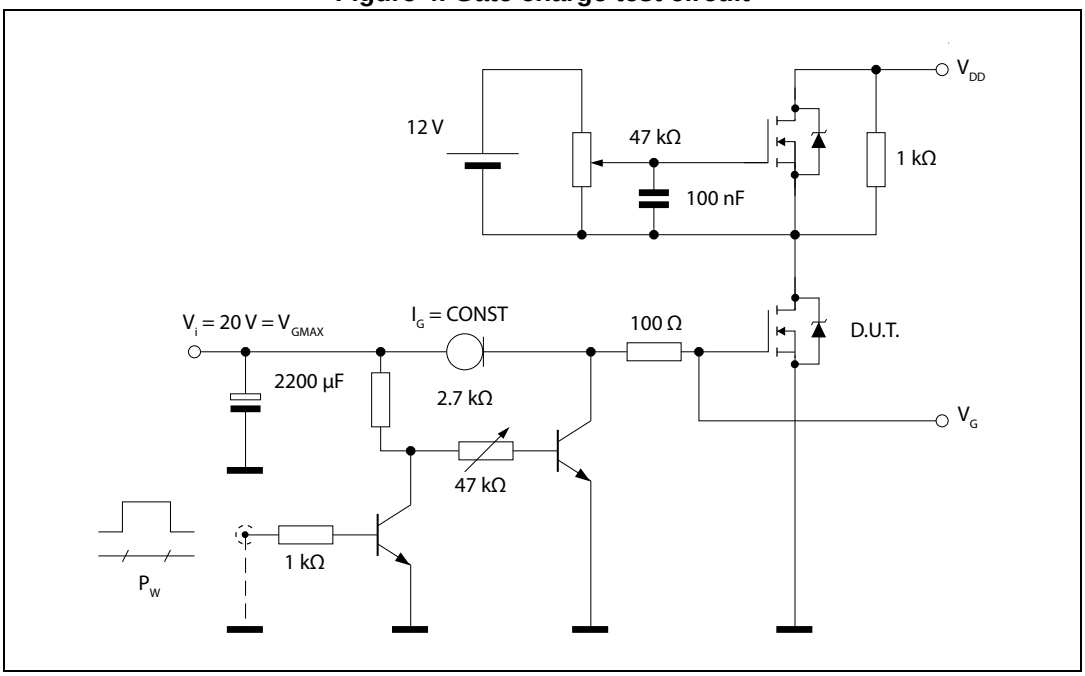


Figure 5. Test circuit for inductive load switching and diode recovery times

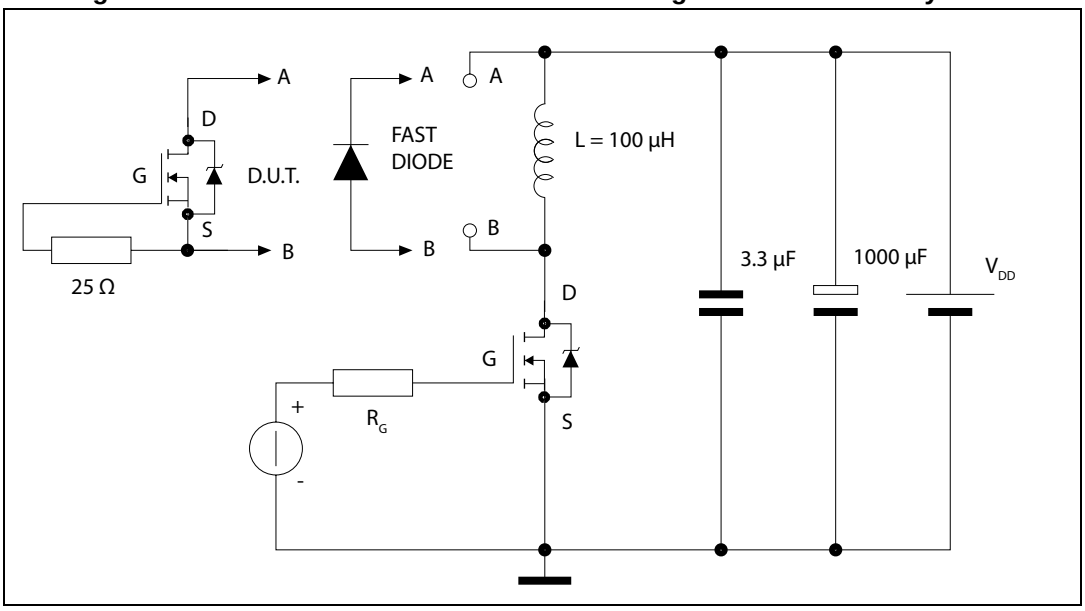
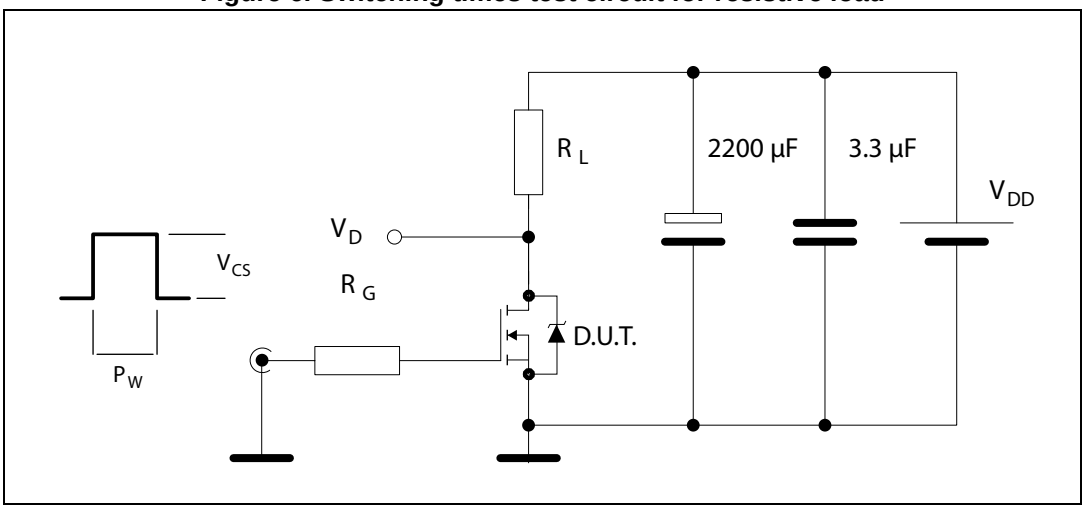


Figure 6. Switching times test circuit for resistive load



3 Package and PCB thermal data

3.1 PowerSSO-36 thermal data

Figure 7. PowerSSO-36™ PC board

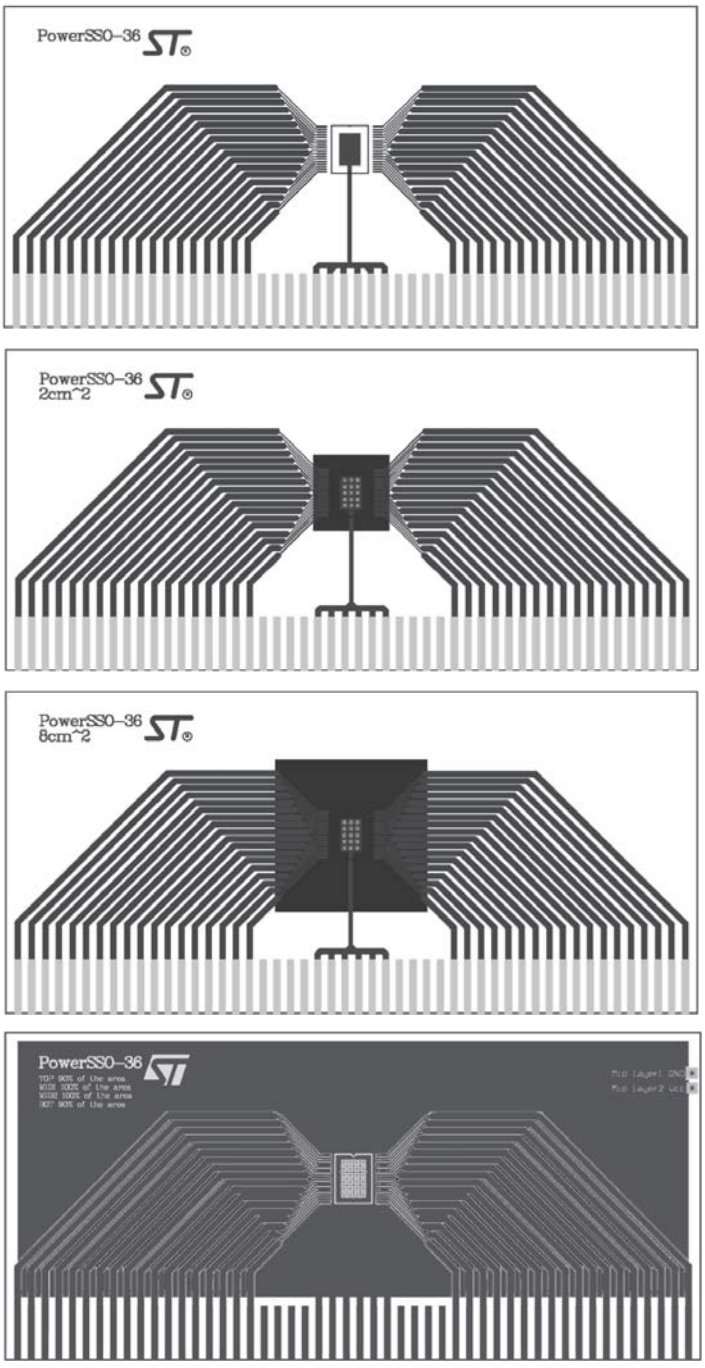


Figure 8. Chipset configuration

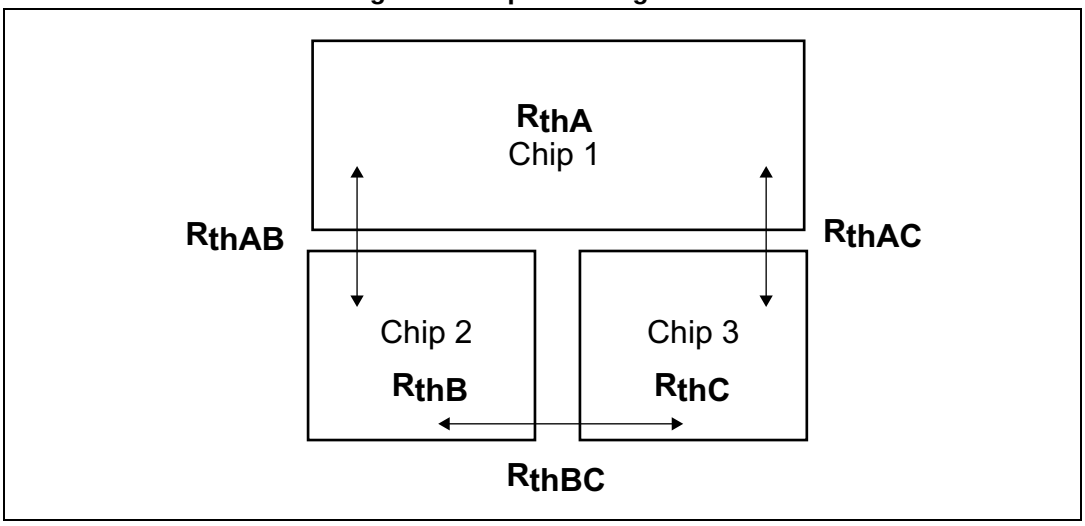
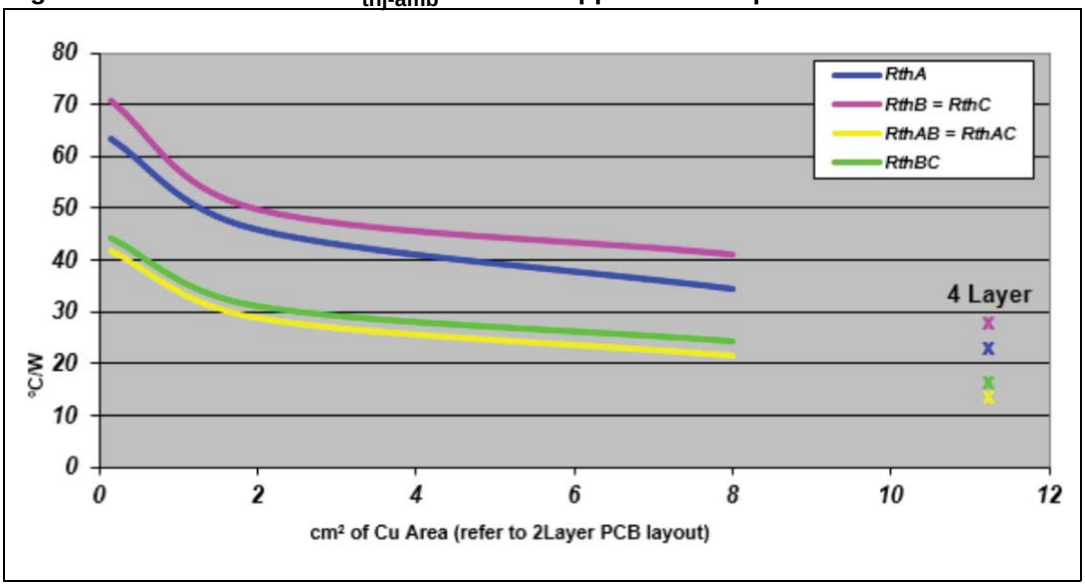


Figure 9. Auto and mutual $R_{thj\text{-}amb}$ vs PCB copper area in open box free air condition



3.1.1 Thermal calculation in clockwise and anti-clockwise operation in steady-state mode

Table 14. Thermal calculation in clockwise and anti-clockwise operation in steady-state mode

HS_A	HS_B	LS_A	LS_B	T_{jHSAB}	T_{jLSA}	T_{jLSB}
ON	OFF	OFF	ON	$P_{dHSA} \times R_{thHS} + P_{dLSB} \times R_{thHSLS} + T_{amb}$	$P_{dHSA} \times R_{thHSLS} + P_{dLSD} \times R_{thLSLS} + T_{amb}$	$P_{dHSA} \times R_{thHSLS} + P_{dLSB} \times R_{thLS} + T_{amb}$
OFF	ON	ON	OFF	$P_{dHSB} \times R_{thHS} + P_{dLSA} \times R_{thHSLS} + T_{amb}$	$P_{dHSB} \times R_{thHSLS} + P_{dLSA} \times R_{thLS} + T_{amb}$	$P_{dHSB} \times R_{thHSLS} + P_{dLSA} \times R_{thLSLS} + T_{amb}$

3.1.2 Thermal resistance definitions (values according to the PCB heatsink area)

- RthHS = RthHSA = RthHSB = high side chip thermal resistance junction to ambient (HSA or HSB in ON state)
- RthLS = RthLSA = RthLSB = low side chip thermal resistance junction to ambient
- RthHSLS = RthHSALSB = RthHSBLSA = mutual thermal resistance junction to ambient between high side and low side chips
- RthLSLS = RthLSALSB = mutual thermal resistance junction to ambient between low side chips

3.1.3 Thermal calculation in transient mode[a]

- TjHSAB = ZthHS x PdHSAB + ZthHSLS x (PdLSA + PdLSB) + Tamb
- TjLSA = ZthHSLS x PdHSAB + ZthLS x PdLSA + ZthLSLS x PdLSB + Tamb
- TjLSB = ZthHSLS x PdHSAB + ZthLSLS x PdLSA + ZthLS x PdLSB + Tamb

3.1.4 Single pulse thermal impedance definitions (values according to the PCB heatsink area)

- ZthHS = high side chip thermal impedance junction to ambient
- ZthLS = ZthLSA = ZthLSB = low side chip thermal impedance junction to ambient
- ZthHSLS = ZthHSABLSA = ZthHSABLSB = mutual thermal impedance junction to ambient between high side and low side chips
- ZthLSLS = ZthLSALSB = mutual thermal impedance junction to ambient between low side chips

Equation 1: pulse calculation formula

$$Z_{THδ} = R_{TH} \times δ + Z_{THtp}(1 - δ)$$

where $δ = t_p / T$

a. Calculation is valid in any dynamic operating condition. P_d values set by user.

Figure 10. PowerSSO-36 HSD thermal impedance junction ambient single pulse

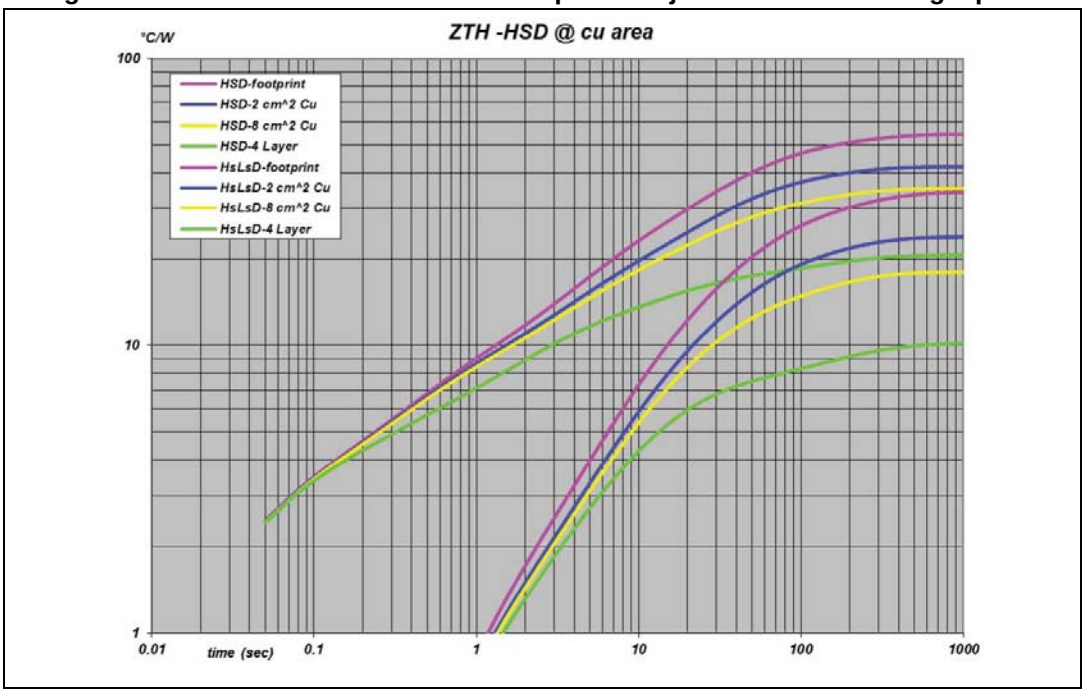


Figure 11. PowerSSO-36 LSD thermal impedance junction ambient single pulse

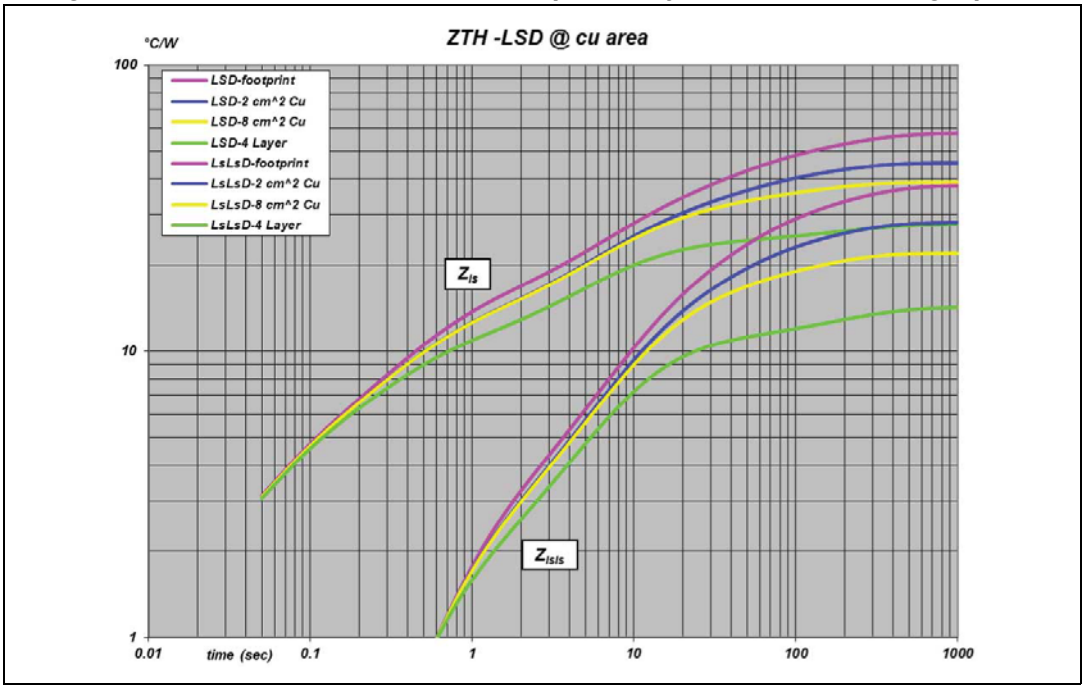


Figure 12. Thermal fitting model of an H-bridge in PowerSSO-36

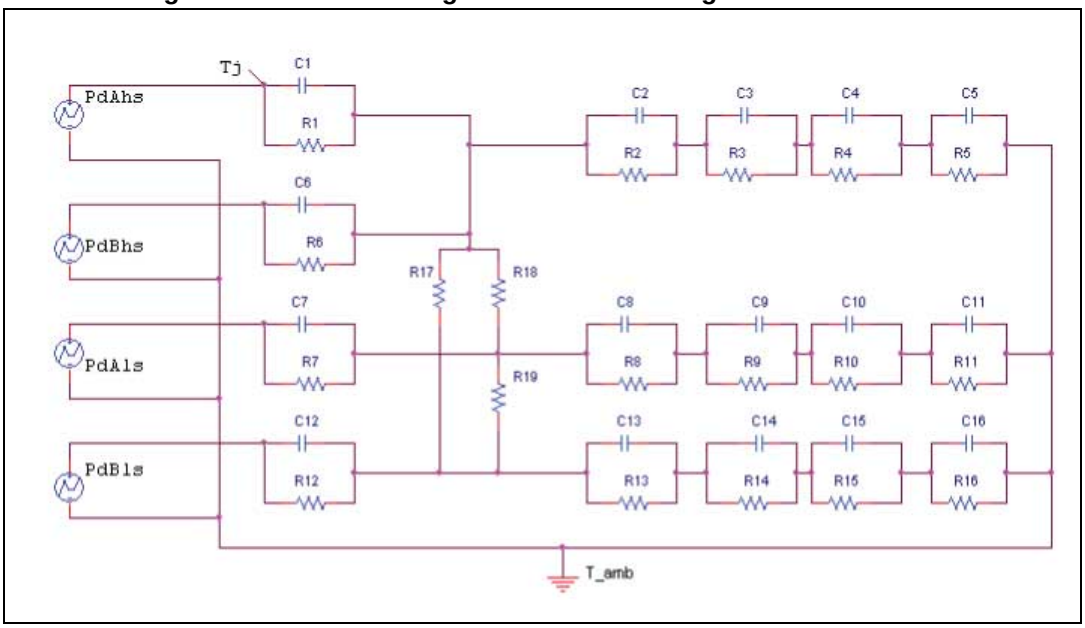


Table 15. Thermal parameters(1)

Area/island (cm^2)	FP	2	8	4L
R1 (°C/W)	2.4			
R2 (°C/W)	4	4	4	2
R3 (°C/W)	14	10	10	8
R4 (°C/W)	50	32	22	9
R5 (°C/W)	34	26	21	8
R6 (°C/W)	2.4			
R7 (°C/W)	2.8			
R8 (°C/W)	12	10	10	8
R9 (°C/W)	37	35	35	30
R10 (°C/W)	41	30	20	10
R11 (°C/W)	50	31	20	15
R12 (°C/W)	2.8			
R13 (°C/W)	12	10	10	8
R14 (°C/W)	37	35	35	30
R15 (°C/W)	41	30	20	10
R16 (°C/W)	50	31	20	15
R17 (°C/W)	73	70	70	50
R18 (°C/W)	73	70	70	50
R19 (°C/W)	53	45	45	35

Table 15. Thermal parameters[1] (continued)

Area/island (cm^2)	FP	2	8	4L
C1 (W·s/°C)	0.015			
C2 (W·s/°C)	0.1			
C3 (W·s/°C)	0.4	0.4	0.4	0.3
C4 (W·s/°C)	0.8	1	1.2	1.5
C5 (W·s/°C)	3	4	6	15
C6 (W·s/°C)	0.015			
C7 (W·s/°C)	0.015			
C8 (W·s/°C)	0.05			
C9 (W·s/°C)	0.3			
C10 (W·s/°C)	0.8	1	1	1.5
C11 (W·s/°C)	4	5	6	15
C12 (W·s/°C)	0.015			
C13 (W·s/°C)	0.05			
C14 (W·s/°C)	0.3			
C15 (W·s/°C)	0.8	1	1	1.5
C16 (W·s/°C)	4	5	6	15

1. The blank space means that the value is the same as the previous one.

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

4.1 PowerSSO-36 TP package information

Figure 13. PowerSSO-36 TP package outline

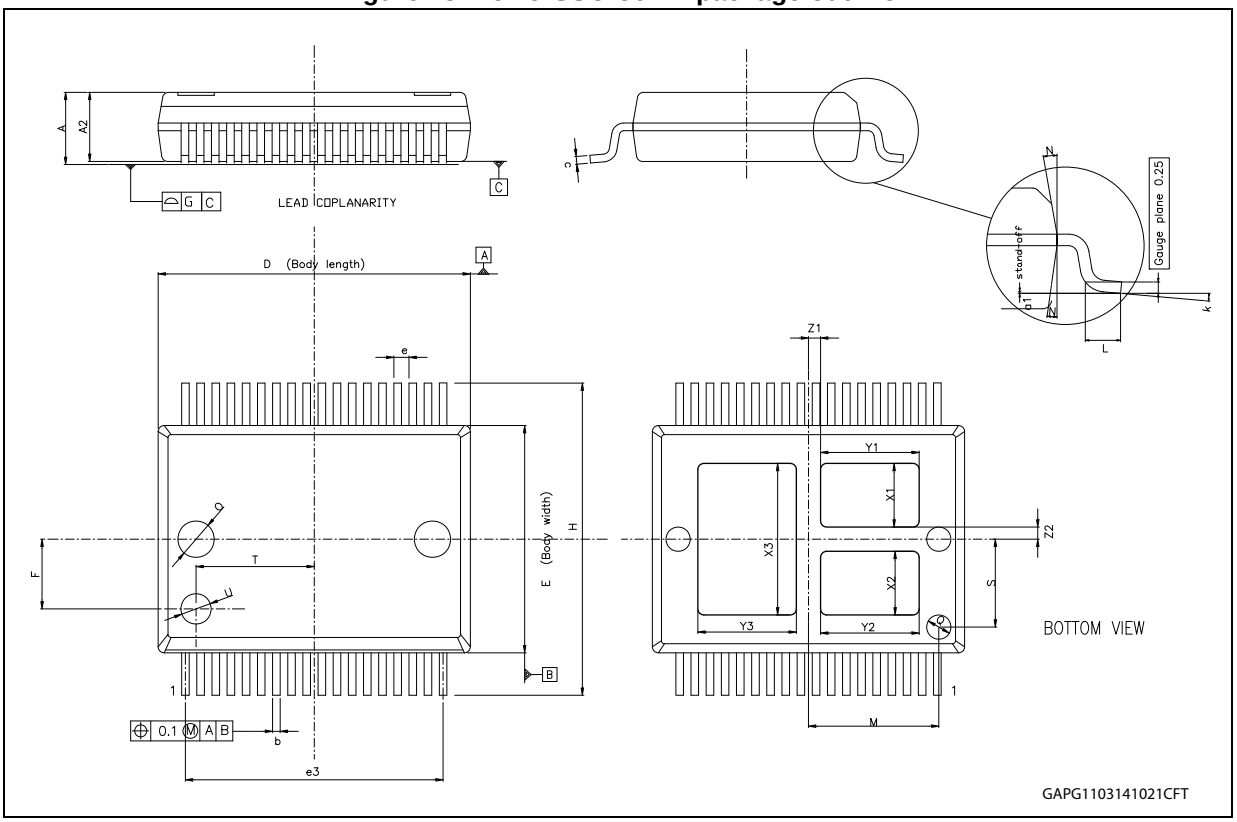
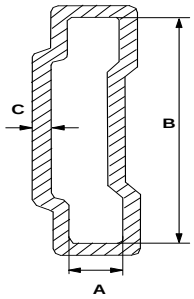


Table 16. PowerSSO-36 TP mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	2.15		2.47
A2	2.15		2.40
a1	0		0.1
b	0.18		0.36
c	0.23		0.32
D	10.10		10.50
E	7.4		7.6
e		0.5	
e3		8.5	
F		2.3	
G			0.1
H	10.1		10.5
h			0.4
k	0 deg		8 deg
L	0.6		1
M		4.3	
N			10 deg
O		1.2	
Q		0.8	
S		2.9	
T		3.65	
U		1.0	
X1	1.85		2.35
Y1	3		3.5
X2	1.85		2.35
Y2	3		3.5
X3	4.7		5.2
Y3	3		3.5
Z1		0.4	
Z2		0.4	

4.2 PowerSSO-36 TP packing information

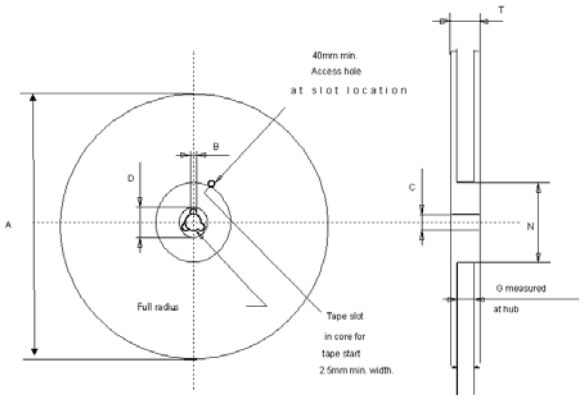
Figure 14. PowerSSO-36 TP tube shipment (no suffix)



Base Qty	49
Bulk Qty	1225
Tube length (±0.5)	532
A	3.5
B	13.8
C (±0.1)	0.6

All dimensions are in mm.

Figure 15. PowerSSO-36 TP tape and reel shipment (suffix "TR")



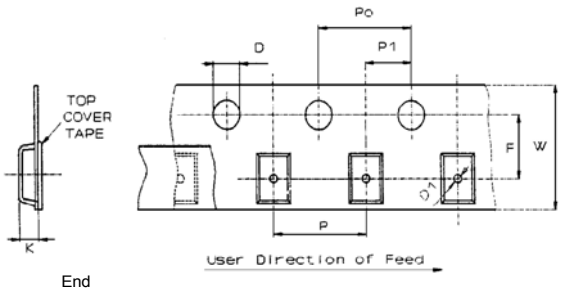
Reel dimensions

Base Qty	1000
Bulk Qty	1000
A (max)	330
B (min)	1.5
C (±0.2)	13
F	20.2
G (+2 / -0)	24.4
N (min)	100
T (max)	30.4

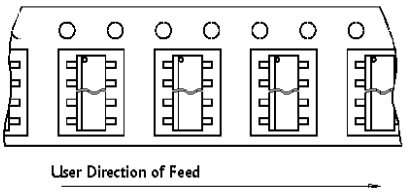
Tape dimensions
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

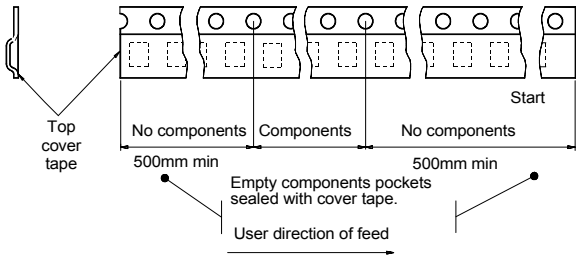
Tape width	**W**	24
Tape Hole Spacing	**P0 (±0.1)**	4
Component Spacing	**P**	12
Hole Diameter	**D (±0.05)**	1.55
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (±0.1)**	11.5
Compartment Depth	**K (max)**	2.85
Hole Spacing	**P1 (±0.1)**	2

All dimensions are in mm.



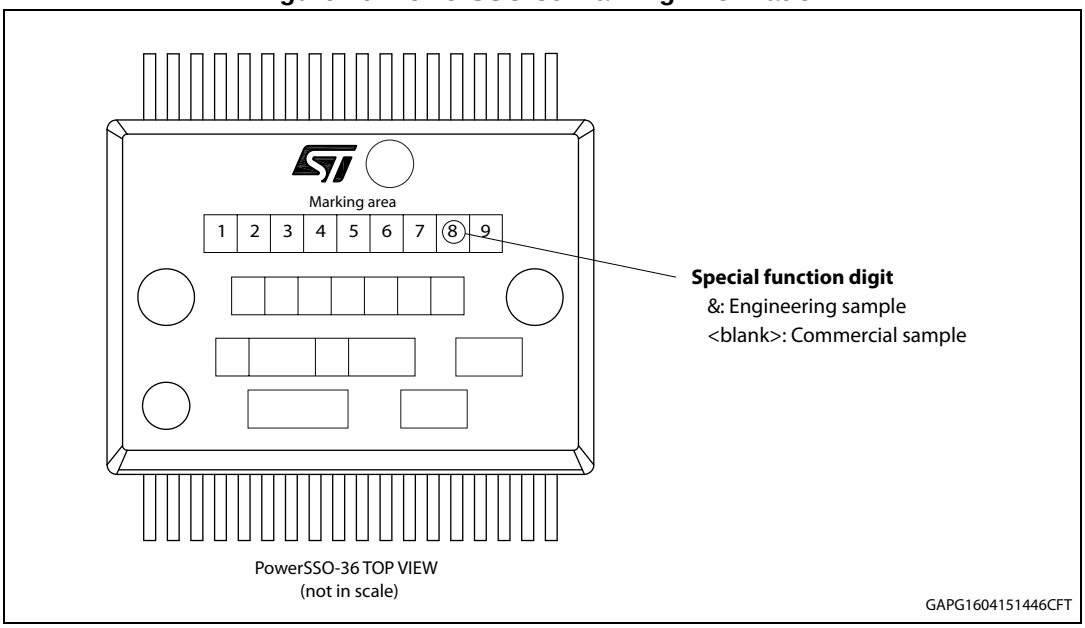
End





4.3 PowerSSO-36 marking information

Figure 16. PowerSSO-36 marking information



Note: Parts marked as "&" are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

Note: Commercial Samples: fully qualified parts from ST standard production with no usage restrictions.

5 Revision history

Table 17. Document revision history

Date	Revision	Changes
14-Oct-2015	1	Initial release
26-Apr-2016	2	Updated following tables: – *Table 4: Power off* – *Table 5: Power on* – *Table 6: Dynamic* – *Table 7: Gate resistance* – *Table 8: Source drain diode* – *Table 9: Switching on HSD* – *Table 10: Switching on LSD* – *Table 11: Switching off HSD* – *Table 12: Switching off LSD* – *Table 13: Thermal sensor*
20-Jun-2016	3	Updated *Table 3: Absolute maximum rating*, *Table 5: Power on, Table 6: Dynamic, Table 7: Gate resistance, Table 8: Source drain diode, Table 9: Switching on HSD, Table 10: Switching on LSD* and *Table 13: Thermal sensor.* Document status changed from target to preliminary data.
13-Jul-2016	4	Updated *Table 4: Power off*
28-Nov-2016	5	Removed table thermal data on page 8. Updated *Section 4: Package information*. Added *Section 3: Package and PCB thermal data*. Minor text changes.
17-Jan-2017	6	Updated *Features* Updated following tables: – *Table 3: Absolute maximum rating* – *Table 6: Dynamic* – *Table 7: Gate resistance* – *Table 8: Source drain diode* – *Table 9: Switching on HSD* – *Table 10: Switching on LSD* – *Table 11: Switching off HSD* – *Table 12: Switching off LSD* – *Table 13: Thermal sensor*

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