

Quad channel high side driver

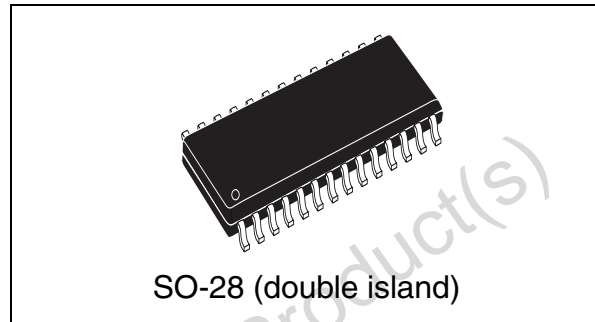
Features

| Type | $R_{DS(on)}$ | I_{OUT} | V_{CC} |
|--------|------------------------------|---------------------|----------|
| VNQ810 | 160m Ω ⁽¹⁾ | 3.5A ⁽¹⁾ | 36V |

1. Per each channel.

- CMOS compatible inputs
- Open Drain status outputs
- On state open load detection
- Off state open load detection
- Shorted load protection
- Undervoltage and overvoltage shutdown
- Loss of ground protection
- Very low standby current
- Reverse battery protection^(a)

a. See [Application schematic on page 18](#)



Description

The VNQ810 is a quad HSD formed by assembling two VND810 chips in the same SO-28 package. The VND810 is a monolithic device made using STMicroelectronics VIPower M0-3 Technology. The VNQ830 is intended for driving any type of multiple load with one side connected to ground.

The Active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table). Active current limitation combined with thermal shutdown and automatic restart protects the device against overload. The device detects the open load condition in both the on and off state.

In the off state the device detects if the output is shorted to V_{CC} . The device automatically turns off in the case where the ground pin becomes disconnected.

Table 1. Device summary

| Package | Order codes | |
|-----------------------|-------------|---------------|
| | Tube | Tape and reel |
| SO-28 (double island) | VNQ810 | VNQ81013TR |

Contents

| | | |
|----------|--|-----------|
| 1 | Block diagram and pin description | 5 |
| 2 | Electrical specifications | 7 |
| 2.1 | Absolute maximum ratings | 7 |
| 2.2 | Thermal data | 8 |
| 2.3 | Electrical characteristics | 8 |
| 2.4 | Electrical characteristics curves | 15 |
| 3 | Application information | 18 |
| 3.1 | GND protection network against reverse battery | 18 |
| 3.1.1 | Solution 1: a resistor in the ground line (RGND only) | 18 |
| 3.1.2 | Solution 2: a diode (D _{GND}) in the ground line | 19 |
| 3.2 | Load dump protection | 19 |
| 3.3 | MCU I/O protection | 19 |
| 3.4 | Open load detection in off state | 20 |
| 3.5 | Maximum demagnetization energy (V _{CC} = 13.5V) | 21 |
| 4 | Package and PCB thermal data | 22 |
| 4.1 | SO-28 thermal data | 22 |
| 5 | Package and packing information | 25 |
| 5.1 | ECOPACK® packages | 25 |
| 5.2 | SO-28 packing information | 26 |
| 6 | Revision history | 27 |

List of tables

| | | |
|-----------|---|----|
| Table 1. | Device summary | 1 |
| Table 2. | Suggested connections for unused and not connected pins | 6 |
| Table 3. | Absolute maximum ratings | 7 |
| Table 4. | Thermal data (per island) | 8 |
| Table 5. | Power output. | 9 |
| Table 6. | Protections | 9 |
| Table 7. | V_{CC} - output diode | 10 |
| Table 8. | Switching ($V_{CC} = 13V$; $T_j = 25^{\circ}C$) | 10 |
| Table 9. | Logic inputs. | 10 |
| Table 10. | Status pin | 10 |
| Table 11. | Openload detection. | 11 |
| Table 12. | Truth table. | 12 |
| Table 13. | Electrical transient requirements | 13 |
| Table 14. | Thermal calculation according to the PCB heatsink area | 22 |
| Table 15. | Thermal parameters | 24 |
| Table 16. | SO-28 mechanical data | 25 |
| Table 17. | Document revision history | 27 |

List of figures

| | | |
|------------|--|----|
| Figure 1. | Block diagram | 5 |
| Figure 2. | Configuration diagram (top view) | 6 |
| Figure 3. | Current and voltage conventions | 8 |
| Figure 4. | Status timings | 11 |
| Figure 5. | Switching characteristics | 11 |
| Figure 6. | Waveforms | 14 |
| Figure 7. | Off state output current | 15 |
| Figure 8. | High level input current | 15 |
| Figure 9. | Input clamp voltage | 15 |
| Figure 10. | Turn-on voltage slope | 15 |
| Figure 11. | Overvoltage shutdown | 15 |
| Figure 12. | Turn-off voltage slope | 15 |
| Figure 13. | ILIM vs Tcase | 16 |
| Figure 14. | On state resistance vs VCC | 16 |
| Figure 15. | Input high level | 16 |
| Figure 16. | Input hysteresis voltage | 16 |
| Figure 17. | On state resistance vs Tcase | 16 |
| Figure 18. | Input low level | 16 |
| Figure 19. | Status leakage current | 17 |
| Figure 20. | Status low output voltage | 17 |
| Figure 21. | Status clamp voltage | 17 |
| Figure 22. | Openload On state detection threshold | 17 |
| Figure 23. | Openload Off state voltage detection threshold | 17 |
| Figure 24. | Application schematic | 18 |
| Figure 25. | Openload detection in Off state | 20 |
| Figure 26. | Maximum turn-off current versus load inductance | 21 |
| Figure 27. | SO-28 PC board | 22 |
| Figure 28. | Rthj-amb Vs PCB copper area in open box free air condition | 23 |
| Figure 29. | Thermal impedance junction ambient single pulse | 23 |
| Figure 30. | Thermal fitting model of a quad channel HSD in SO-28 | 24 |
| Figure 31. | SO-28 package dimensions | 25 |
| Figure 32. | SO-28 tube shipment (no suffix) | 26 |
| Figure 33. | SO-28 tape and reel shipment (suffix "TR") | 26 |

1 Block diagram and pin description

Figure 1. Block diagram

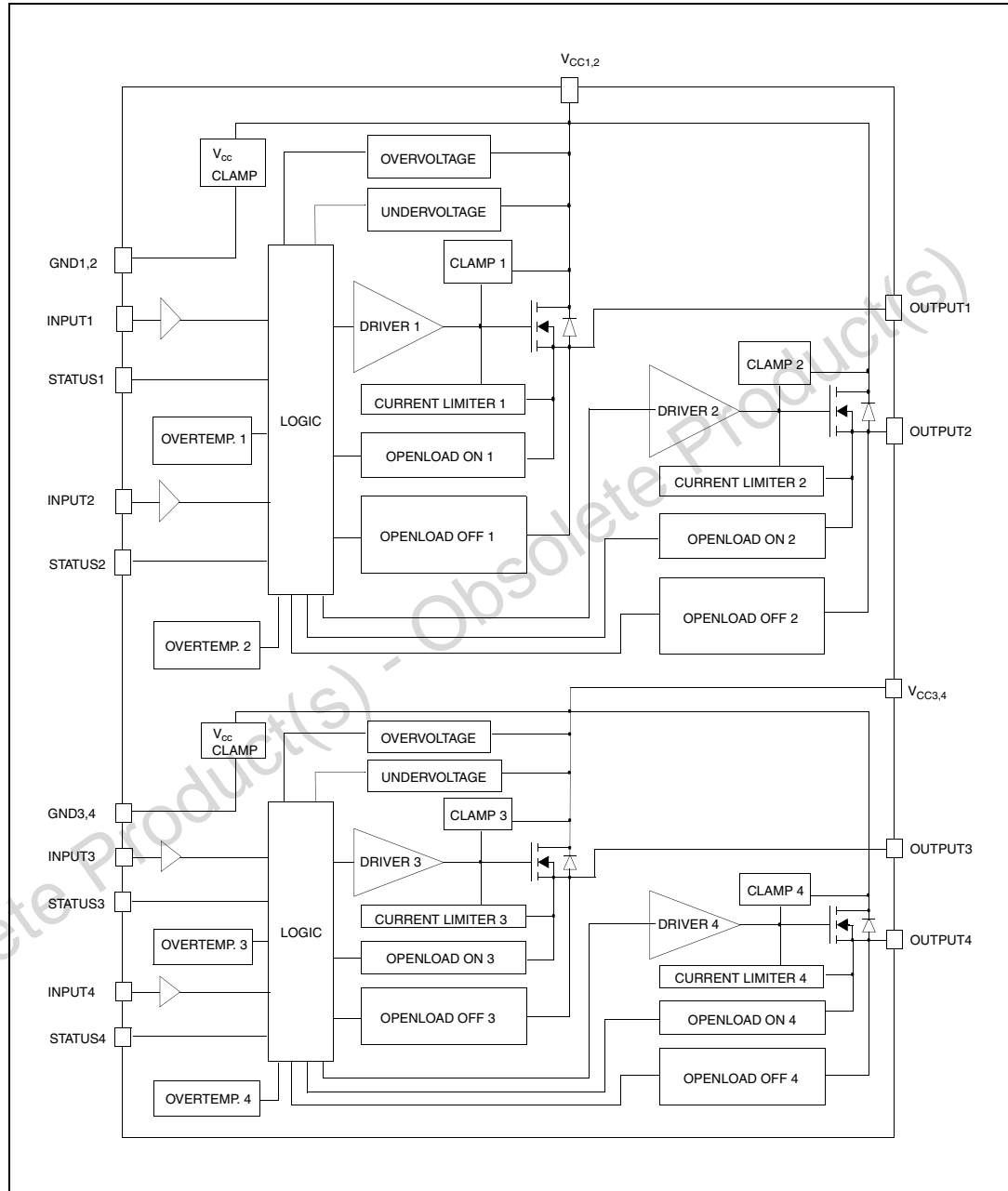


Figure 2. Configuration diagram (top view)

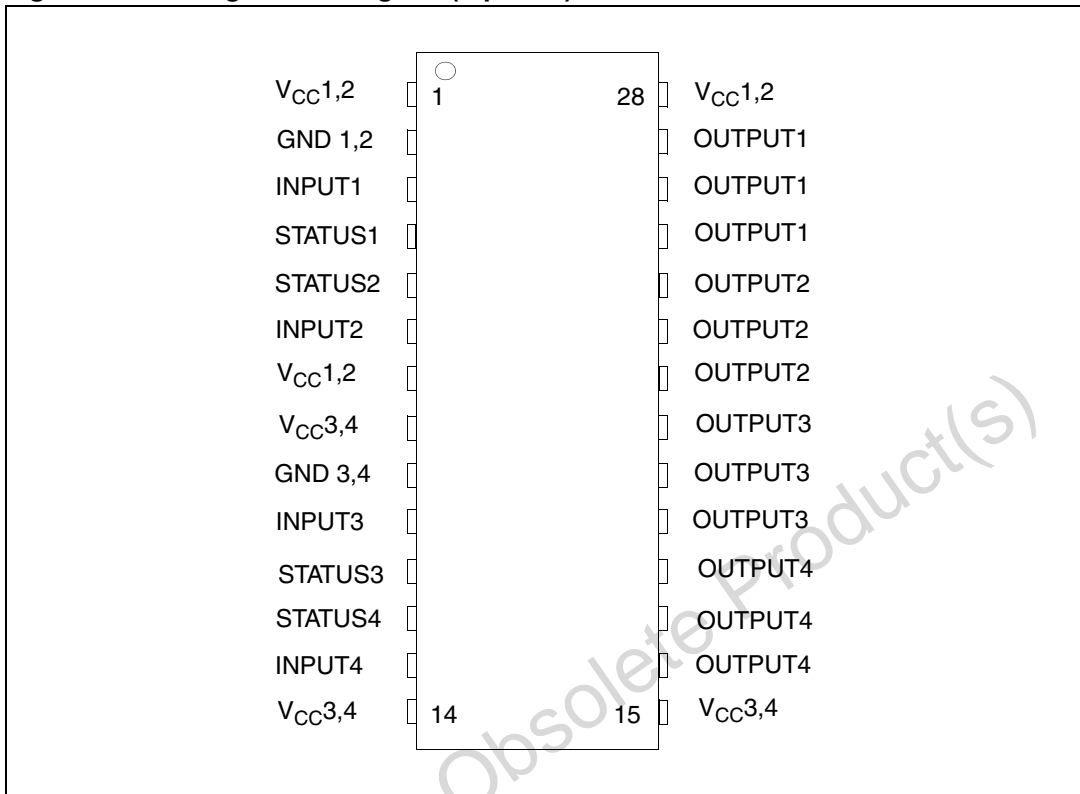


Table 2. Suggested connections for unused and not connected pins

| Connection / pin | Status | N.C. | Output | Input |
|------------------|--------|------|--------|-----------------------|
| Floating | X | X | X | X |
| To ground | | X | | Through 10KΩ resistor |

2 Electrical specifications

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality document.

Table 3. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|------------|---|--------------------|------------|
| V_{CC} | DC supply voltage | 41 | V |
| $-V_{CC}$ | Reverse DC supply voltage | - 0.3 | V |
| $-I_{GND}$ | DC reverse ground pin current | - 200 | mA |
| I_{OUT} | DC output current | Internally limited | A |
| $-I_{OUT}$ | Reverse DC output current | - 6 | A |
| I_{IN} | DC input current | +/- 10 | mA |
| I_{STAT} | DC Status current | +/- 10 | mA |
| V_{ESD} | Electrostatic discharge (human body model: $R=1.5K\Omega$; $C = 100pF$) | | |
| | - INPUT | 4000 | V |
| | - STATUS | 4000 | V |
| | - OUTPUT | 5000 | V |
| | - V_{CC} | 5000 | V |
| E_{MAX} | Maximum switching energy ($L = 2.5mH$; $R_L = 0\Omega$; $V_{bat} = 13.5V$; $T_{jstart} = 150^\circ C$; $I_L = 9A$) | 23 | mJ |
| P_{tot} | Power dissipation (per island) at $T_{lead} = 25^\circ C$ | 6.25 | W |
| T_j | Junction operating temperature | Internally limited | $^\circ C$ |
| T_{stg} | Storage temperature | - 55 to 150 | $^\circ C$ |

2.2 Thermal data

Table 4. Thermal data (per island)

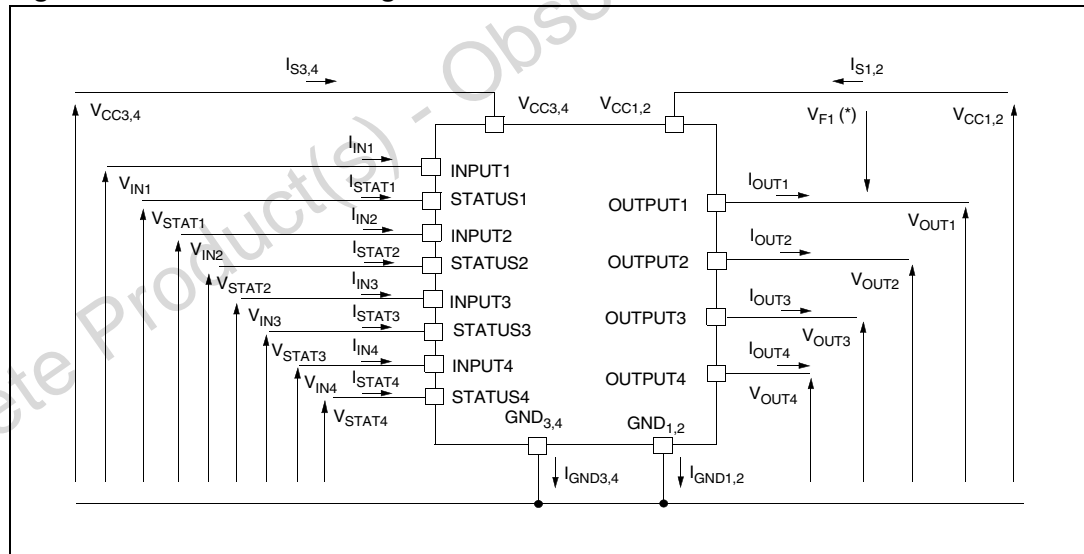
| Symbol | Parameter | Value | | Unit |
|----------------|--|-------------------|-------------------|------|
| $R_{thj-lead}$ | Thermal resistance junction-lead | 20 | | °C/W |
| $R_{thj-amb}$ | Thermal resistance junction-ambient (one chip ON) | 60 ⁽¹⁾ | 44 ⁽²⁾ | °C/W |
| $R_{thj-amb}$ | Thermal resistance junction-ambient (two chips ON) | 46 ⁽¹⁾ | 31 ⁽²⁾ | °C/W |

1. When mounted on a standard single-sided FR-4 board with 0.5cm² of Cu (at least 35 μm thick) connected to all V_{CC} pins. Horizontal mounting and no artificial air flow.
2. When mounted on a standard single-sided FR-4 board with 6cm² of Cu (at least 35 μm thick) connected to all V_{CC} pins. Horizontal mounting and no artificial air flow.

2.3 Electrical characteristics

Values specified in this section are for 8V < V_{CC} < 36V; -40°C < T_j < 150°C, unless otherwise stated.

Figure 3. Current and voltage conventions



Note: $V_{Fn} = V_{CCn} - V_{OUTn}$ during reverse battery condition.

Table 5. Power output

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|--------------------------|--|------|------|------------|--------------------------|
| V_{CC} | Operating supply voltage | | 5.5 | 13 | 36 | V |
| V_{USD} | Undervoltage shutdown | | 3 | 4 | 5.5 | V |
| V_{OV} | Overvoltage shutdown | | 36 | | | V |
| R_{ON} | On state resistance | $I_{OUT} = 1A; T_j = 25^\circ C$ $I_{OUT} = 1A; V_{CC} > 8V$ | | | 160 320 | m Ω m Ω |
| I_S | Supply current | Off State; $V_{CC} = 13V$; $V_{IN} = V_{OUT} = 0V$ | | 12 | 40 | μA |
| | | Off State; $V_{CC} = 13V$; $V_{IN} = V_{OUT} = 0V$; $T_j = 25^\circ C$ | | 12 | 25 | μA |
| | | On State; $V_{CC} = 13V; V_{IN} = 5V$; $I_{OUT} = 0A$ | | 5 | 7 | mA |
| $I_{L(off1)}$ | Off state output current | $V_{IN} = V_{OUT} = 0V$ | 0 | | 50 | μA |
| $I_{L(off2)}$ | Off state output current | $V_{IN} = 0V; V_{OUT} = 3.5V$ | -75 | | 0 | μA |
| $I_{L(off3)}$ | Off state output current | $V_{IN} = V_{OUT} = 0V; V_{CC} = 13V$; $T_j = 125^\circ C$ | | | 5 | μA |
| $I_{L(off4)}$ | Off state output current | $V_{IN} = V_{OUT} = 0V; V_{CC} = 13V$; $T_j = 25^\circ C$ | | | 3 | μA |

Table 6. Protections

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-------------|-------------------------------------|-------------------------|---------------|---------------|---------------|------------|
| T_{TSD} | Shutdown temperature | | 150 | 175 | 200 | $^\circ C$ |
| T_R | Reset temperature | | 135 | | | $^\circ C$ |
| T_{hyst} | Thermal hysteresis | | 7 | 15 | | $^\circ C$ |
| t_{SDL} | Status delay in overload conditions | $T_j > T_{TSD}$ | | | 20 | μs |
| I_{lim} | Current limitation | $V_{CC} = 13V$ | 3.5 | 5 | 7.5 | A |
| | | $5.5V < V_{CC} < 36V$ | | | 7.5 | A |
| V_{demag} | Turn-off output clamp voltage | $I_{OUT} = 1A; L = 6mH$ | $V_{CC} - 41$ | $V_{CC} - 48$ | $V_{CC} - 55$ | V |

Note: To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 7. V_{CC} - output diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------|--------------------|--------------------------------------|------|------|------|------|
| V_F | Forward on voltage | $-I_{OUT} = 0.5A; T_j = 150^\circ C$ | | | 0.6 | V |

Table 8. Switching ($V_{CC} = 13V; T_j = 25^\circ C$)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------------|------------------------|--|------|-------------------------------|------|-----------|
| $t_{d(on)}$ | Turn-on delay time | $R_L = 13\Omega$ from V_{IN} rising edge to $V_{OUT} = 1.3V$ (see Figure 5) | | 30 | | μs |
| $t_{d(off)}$ | Turn-off delay time | $R_L = 13\Omega$ from V_{IN} falling edge to $V_{OUT} = 11.7V$ (see Figure 5) | | 30 | | μs |
| $dV_{OUT}/dt_{(on)}$ | Turn-on voltage slope | $R_L = 13\Omega$ from $V_{OUT} = 1.3V$ to $V_{OUT} = 10.4V$ (see Figure 5) | | See Figure 10 | | $V/\mu s$ |
| $dV_{OUT}/dt_{(off)}$ | Turn-off voltage slope | $R_L = 13\Omega$ from $V_{OUT} = 11.7V$ to $V_{OUT} = 1.3V$ (see Figure 5) | | See Figure 12 | | $V/\mu s$ |

Table 9. Logic inputs

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|--------------------------|-----------------------------------|------|--------------|------|---------|
| V_{IL} | Input low level | | | | 1.25 | V |
| I_{IL} | Low level input current | $V_{IN} = 1.25V$ | 1 | | | μA |
| V_{IH} | Input high level | | 3.25 | | | V |
| I_{IH} | High level input current | $V_{IN} = 3.25V$ | | | 10 | μA |
| $V_{I(hyst)}$ | Input hysteresis voltage | | 0.5 | | | V |
| V_{ICL} | Input clamp voltage | $I_{IN} = 1mA$ $I_{IN} = -1mA$ | 6 | 6.8 - 0.7 | 8 | V V |

Table 10. Status pin

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-------------|------------------------------|---------------------------------------|------|--------------|------|---------|
| V_{STAT} | Status low output voltage | $I_{STAT} = 1.6mA$ | | | 0.5 | V |
| I_{LSTAT} | Status leakage current | Normal operation; $V_{STAT} = 5V$ | | | 10 | μA |
| C_{STAT} | Status pin Input capacitance | Normal operation; $V_{STAT} = 5V$ | | | 100 | pF |
| V_{SCL} | Status clamp voltage | $I_{STAT} = 1mA$ $I_{STAT} = -1mA$ | 6 | 6.8 - 0.7 | 8 | V V |

Table 11. Openload detection

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------------|--|-----------------|------|------|------|---------|
| I_{OL} | Openload On state detection threshold | $V_{IN} = 5V$ | 20 | 40 | 80 | mA |
| $t_{DOL(on)}$ | Openload On state detection delay | $I_{OUT} = 0A$ | | | 200 | μs |
| V_{OL} | Openload Off state voltage detection threshold | $V_{IN} = 0V$ | 1.5 | 2.5 | 3.5 | V |
| $t_{DOL(off)}$ | Openload detection delay at turn-off | | | | 1000 | μs |

Figure 4. Status timings

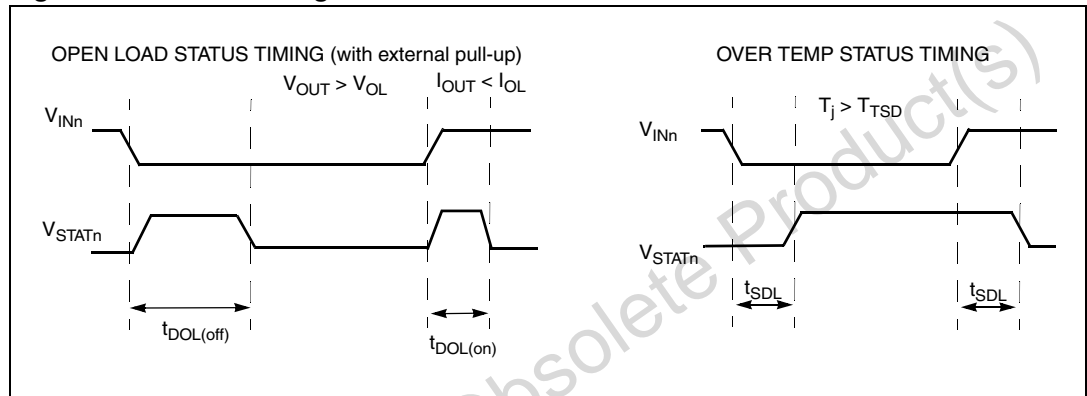


Figure 5. Switching characteristics

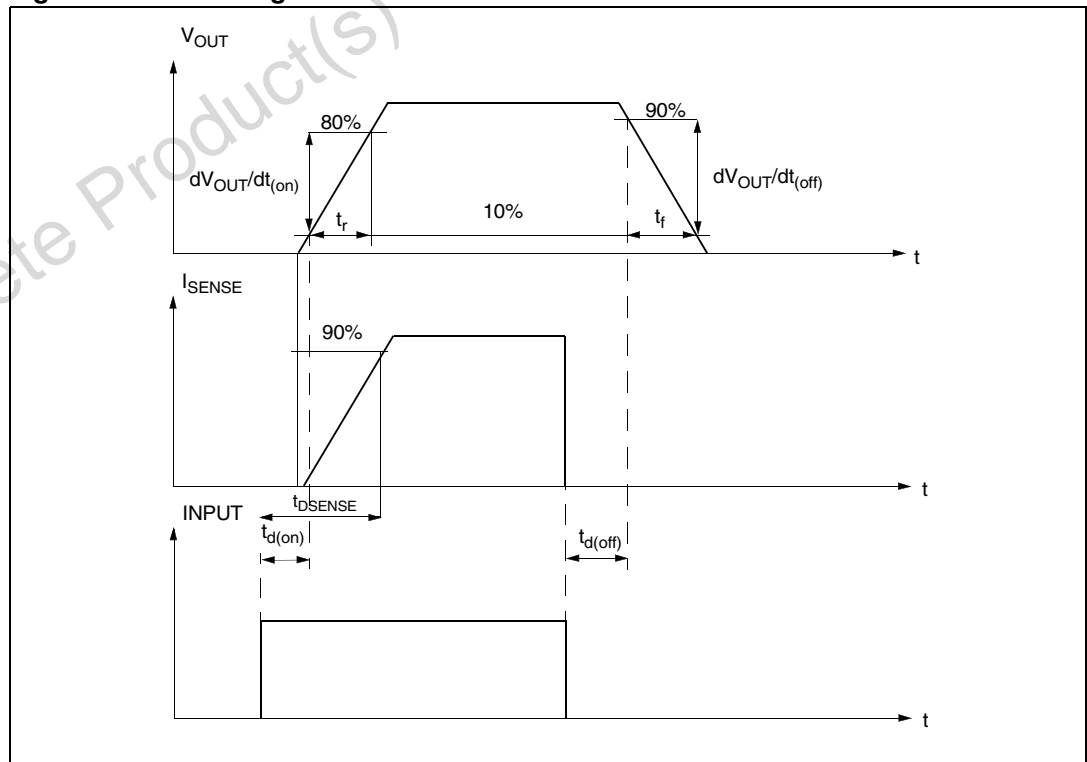


Table 12. Truth table

| Conditions | Input | Output | Status |
|---------------------------|-------|--------|---------------------|
| Normal operation | L | L | H |
| | H | H | H |
| Current limitation | L | L | H |
| | H | X | $(T_j < T_{TSD})$ H |
| | H | X | $(T_j > T_{TSD})$ L |
| Overtemperature | L | L | H |
| | H | L | L |
| Undervoltage | L | L | X |
| | H | L | X |
| Overvoltage | L | L | H |
| | H | L | H |
| Output voltage $> V_{OL}$ | L | H | L |
| | H | H | H |
| Output current $< I_{OL}$ | L | L | H |
| | H | H | L |

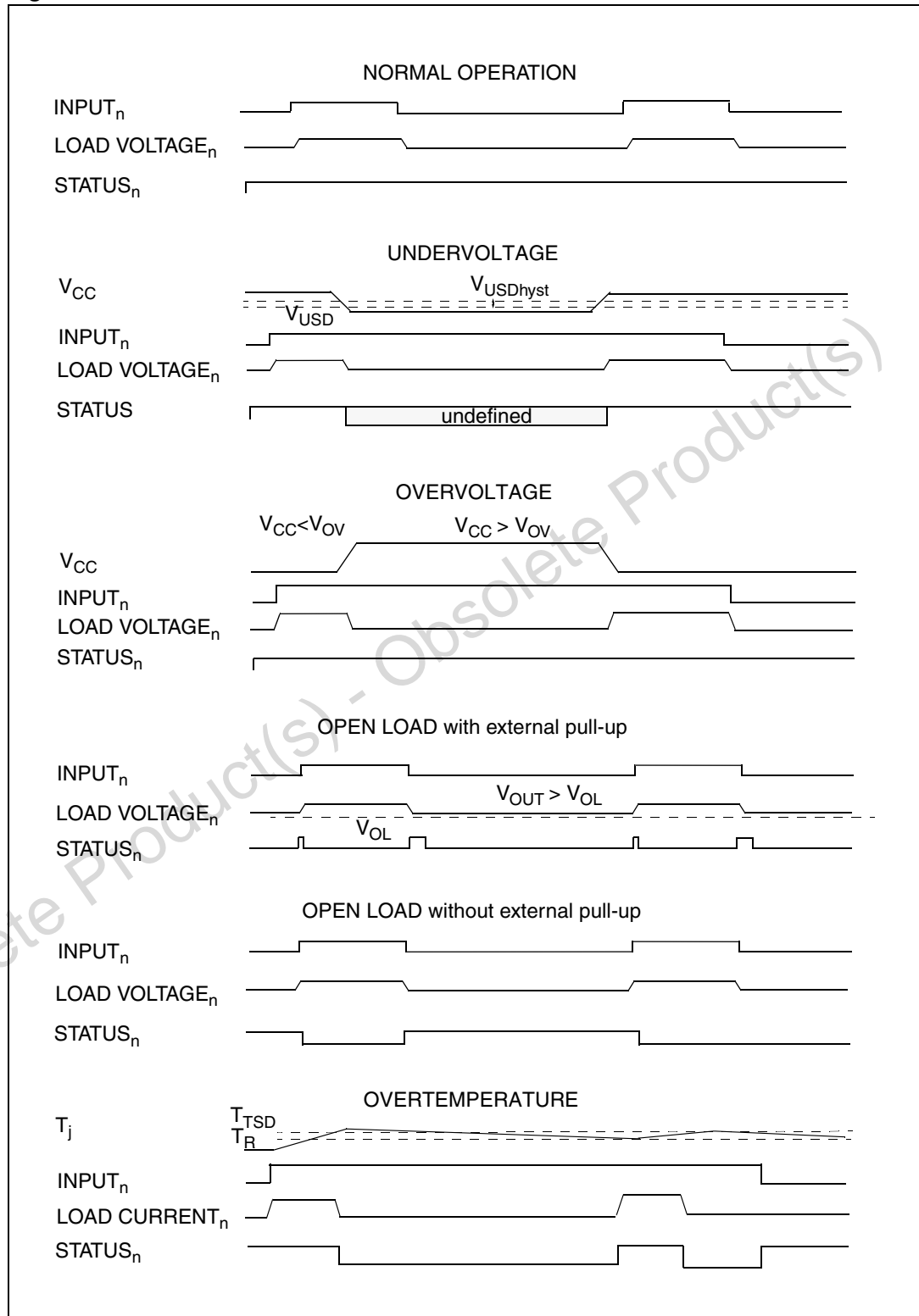
Table 13. Electrical transient requirements

| ISO T/R 7637/1 Test pulse | Test level | | | | Delays and impedance |
|---------------------------------|------------|---------|---------|---------|----------------------|
| | I | II | III | IV | |
| 1 | - 25V | - 50V | - 75V | - 100V | 2ms, 10Ω |
| 2 | + 25V | + 50V | + 75V | + 100V | 0.2ms, 10Ω |
| 3a | - 25V | - 50V | - 100V | - 150V | 0.1μs, 50Ω |
| 3b | + 25V | + 50V | + 75V | + 100V | 0.1μs, 50Ω |
| 4 | - 4V | - 5V | - 6V | - 7V | 100ms, 0.01Ω |
| 5 | + 26.5V | + 46.5V | + 66.5V | + 86.5V | 400ms, 2Ω |

| ISO T/R 7637/1 Test pulse | Test level | | | |
|---------------------------------|------------|----|-----|----|
| | I | II | III | IV |
| 1 | C | C | C | C |
| 2 | C | C | C | C |
| 3a | C | C | C | C |
| 3b | C | C | C | C |
| 4 | C | C | C | C |
| 5 | C | E | E | E |

| Class | Contents |
|-------|--|
| C | All functions of the device are performed as designed after exposure to disturbance. |
| E | One or more functions of the device is not performed as designed after exposure and cannot be returned to proper operation without replacing the device. |

Figure 6. Waveforms



2.4 Electrical characteristics curves

Figure 7. Off state output current

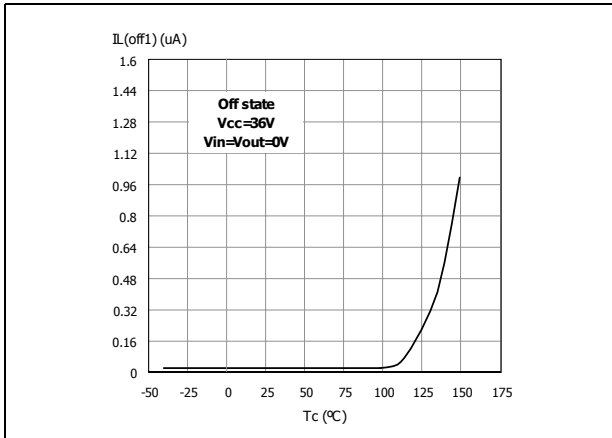


Figure 8. High level input current

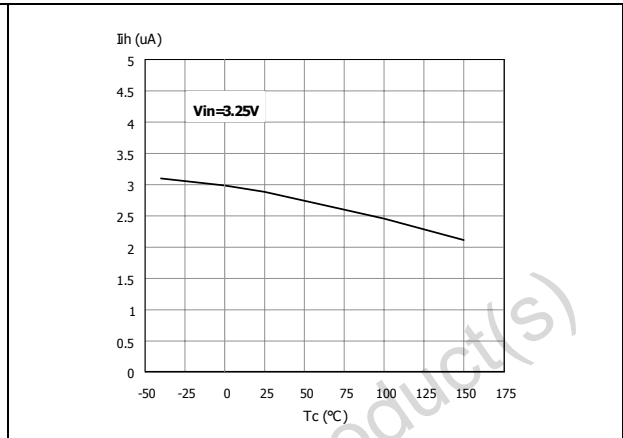


Figure 9. Input clamp voltage

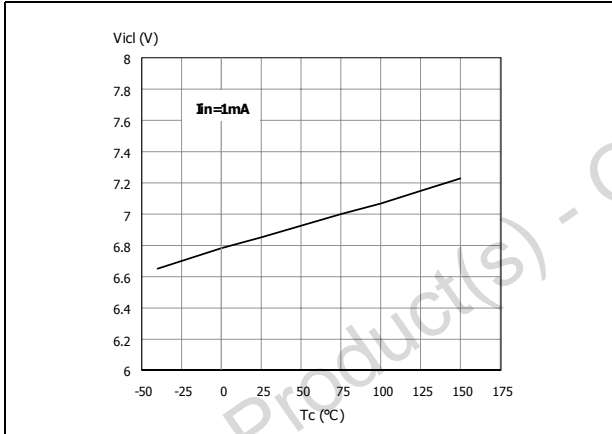


Figure 10. Turn-on voltage slope

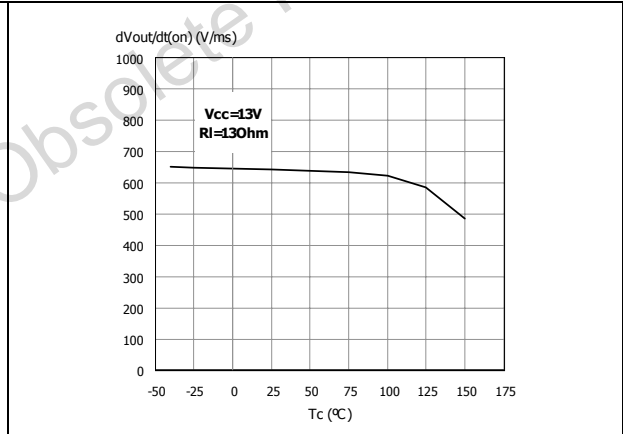


Figure 11. Overvoltage shutdown

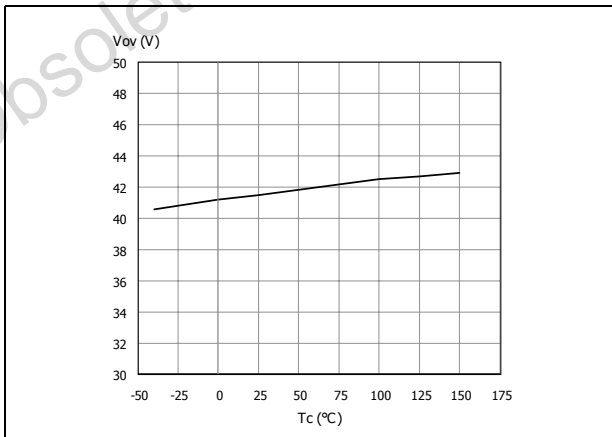


Figure 12. Turn-off voltage slope

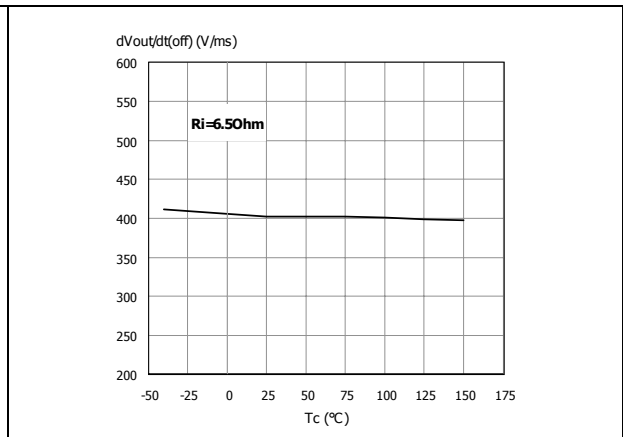


Figure 13. I_{LIM} vs T_{case}

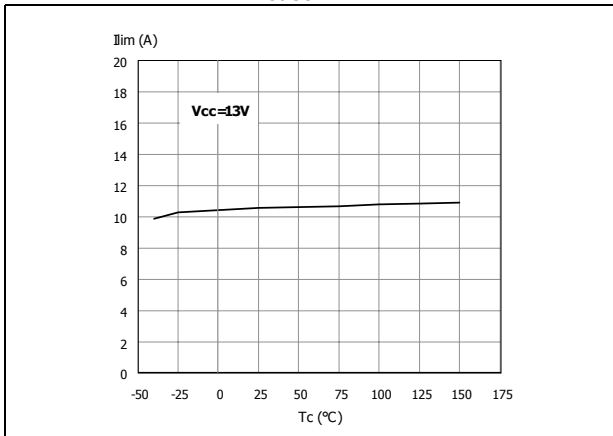


Figure 14. On state resistance vs V_{CC}

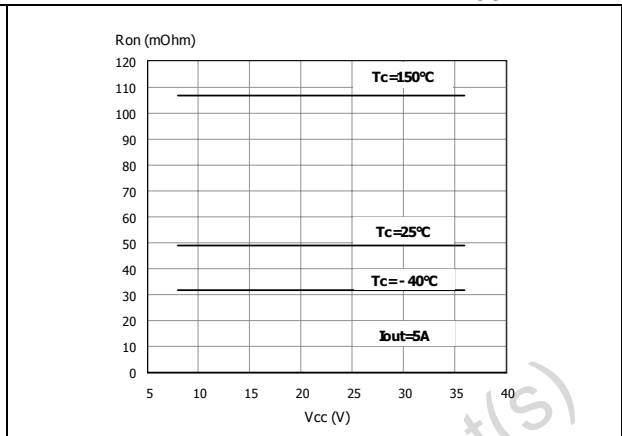


Figure 15. Input high level

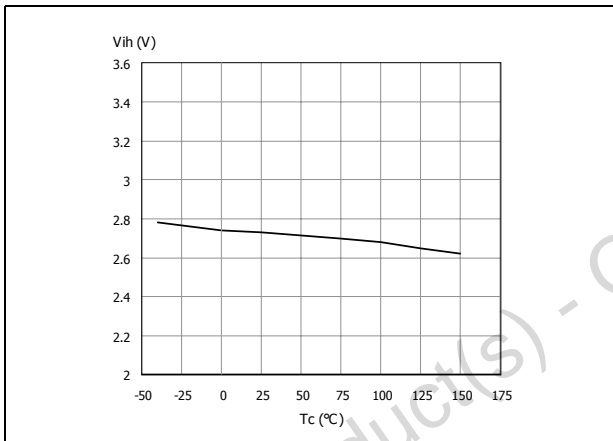


Figure 16. Input hysteresis voltage

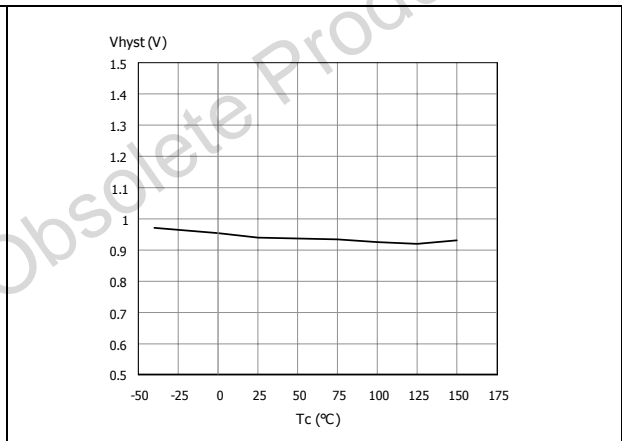


Figure 17. On state resistance vs T_{case}

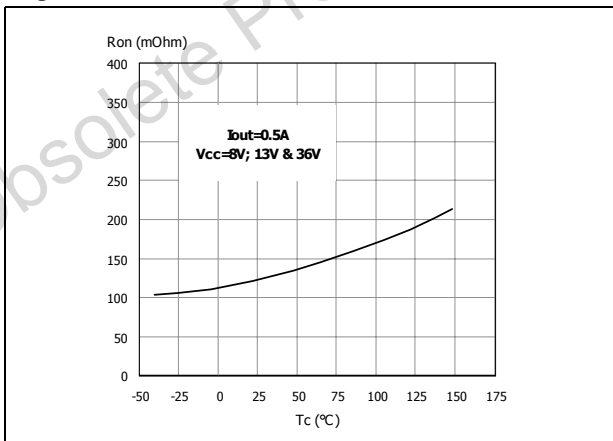


Figure 18. Input low level

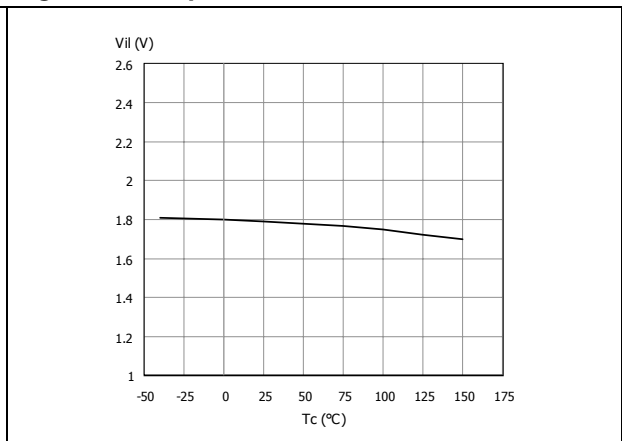


Figure 19. Status leakage current

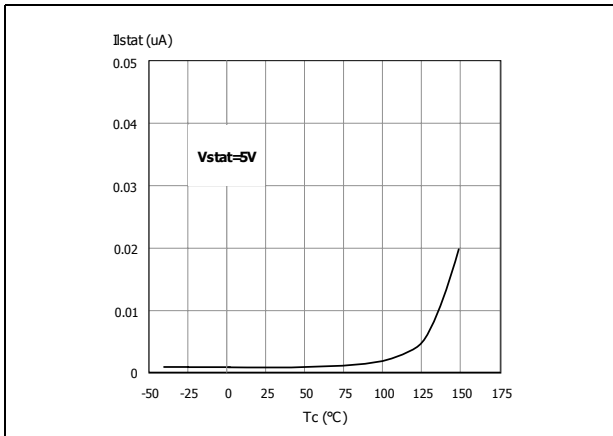


Figure 20. Status low output voltage

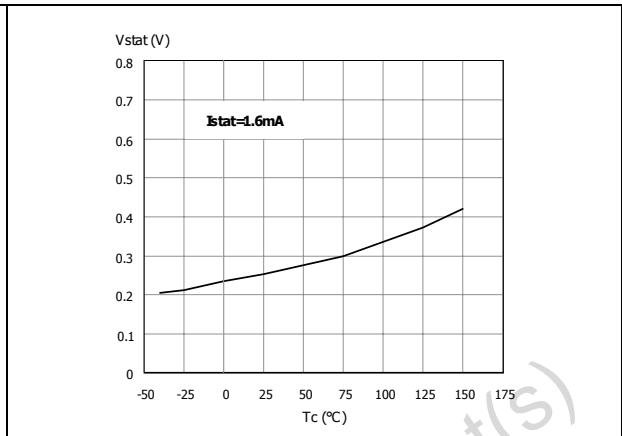


Figure 21. Status clamp voltage

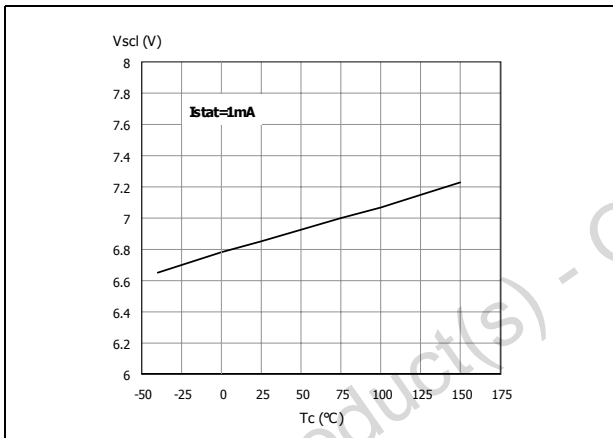


Figure 22. Openload On state detection threshold

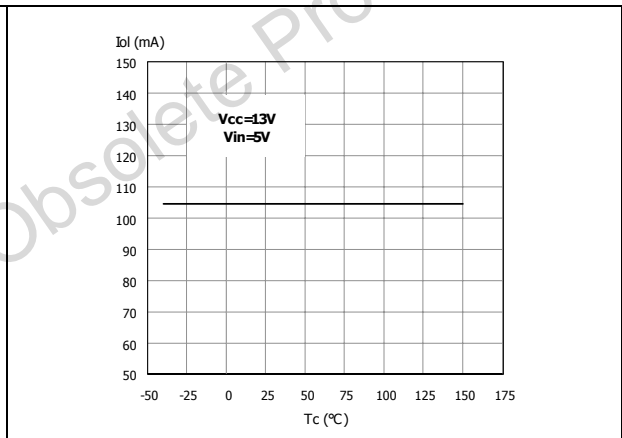
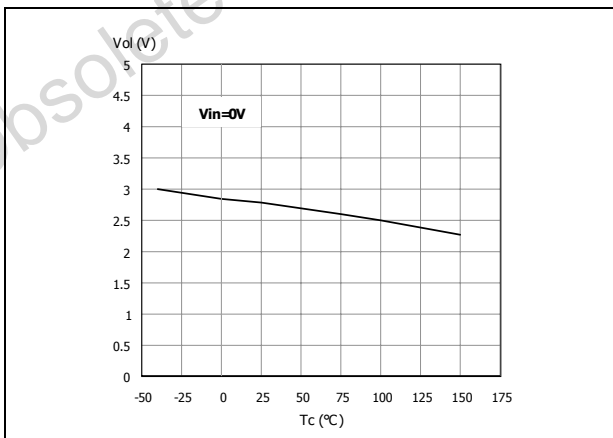
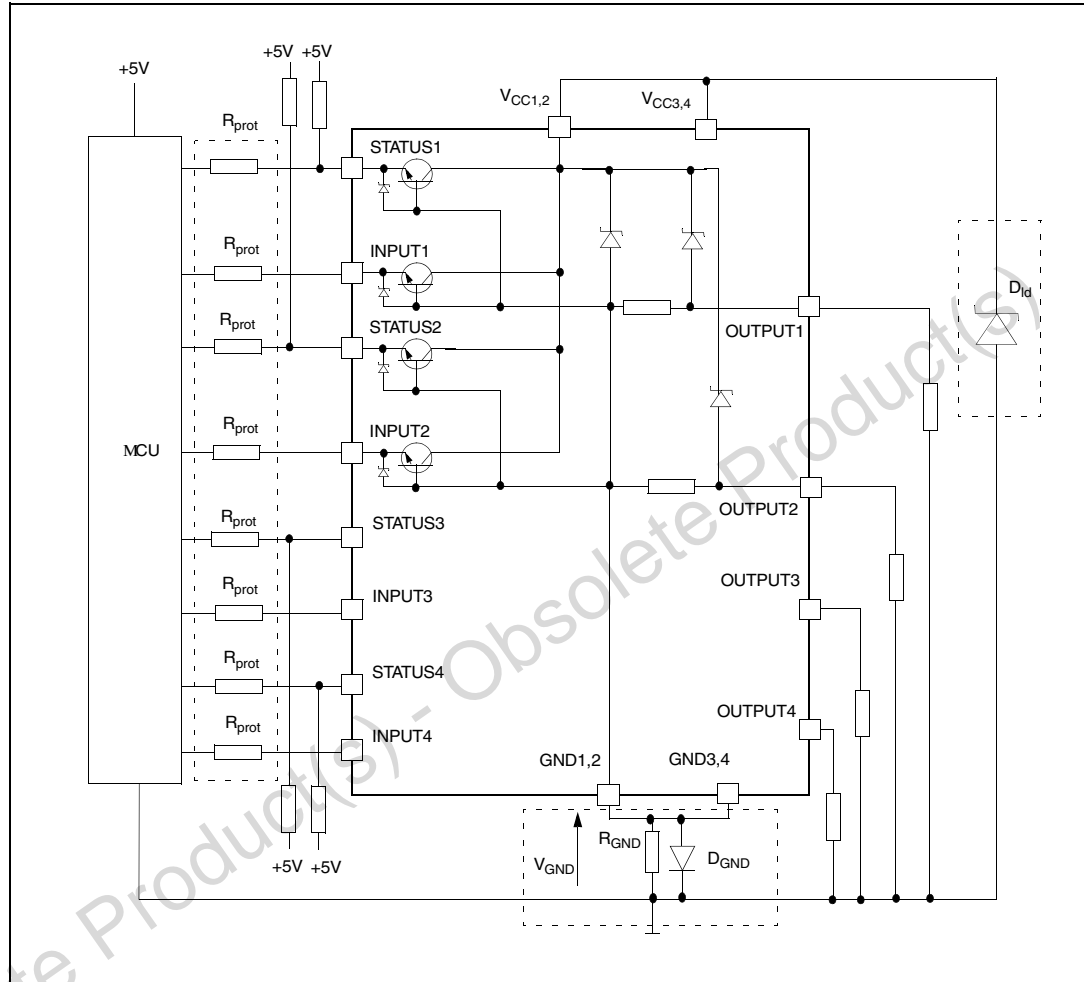


Figure 23. Openload Off state voltage detection threshold



3 Application information

Figure 24. Application schematic



Note: Channels 3 & 4 have the same internal circuit as channel 1 & 2.

3.1 GND protection network against reverse battery

This section provides two solutions for implementing a ground protection network against reverse battery.

3.1.1 Solution 1: a resistor in the ground line (R_{GND} only)

This can be used with any type of load.

The following show how to dimension the R_{GND} resistor:

1. $R_{GND} \leq 600mV / 2 (I_{S(on)max})$
2. $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power dissipation in R_{GND} (when $V_{CC} < 0$ during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that, if the microprocessor ground is not shared by the device ground, then the R_{GND} will produce a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND} .

If the calculated power dissipation requires the use of a large resistor, or several devices have to share the same resistor, then ST suggests using solution 2 below.

3.1.2 Solution 2: a diode (D_{GND}) in the ground line

A resistor ($R_{GND} = 1k\Omega$) should be inserted in parallel to D_{GND} if the device will be driving an inductive load. This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift ($\approx 600mV$) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network. Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the Absolute Maximum Rating. Safest configuration for unused INPUT and STATUS pin is to leave them unconnected.

3.2 Load dump protection

D_{ld} is necessary (voltage transient suppressor) if the load dump peak voltage exceeds the V_{CC} maximum DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than those shown in the ISO T/R 7637/1 table.

3.3 MCU I/O protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the μC I/O pins from latching up.

The value of these resistors is a compromise between the leakage current of μC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of μC I/Os:

$$-V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Example

For the following conditions:

$$V_{CCpeak} = - 100V$$

$$I_{latchup} \geq 20mA$$

$$V_{OH\mu C} \geq 4.5V$$

$$5k\Omega \leq R_{prot} \leq 65k\Omega$$

Recommended values are:

$$R_{prot} = 10k\Omega$$

3.4 Open load detection in off state

Off state open load detection requires an external pull-up resistor (R_{PU}) connected between OUTPUT pin and a positive supply voltage (V_{PU}) like the +5V line used to supply the microprocessor.

The external resistor has to be selected according to the following requirements:

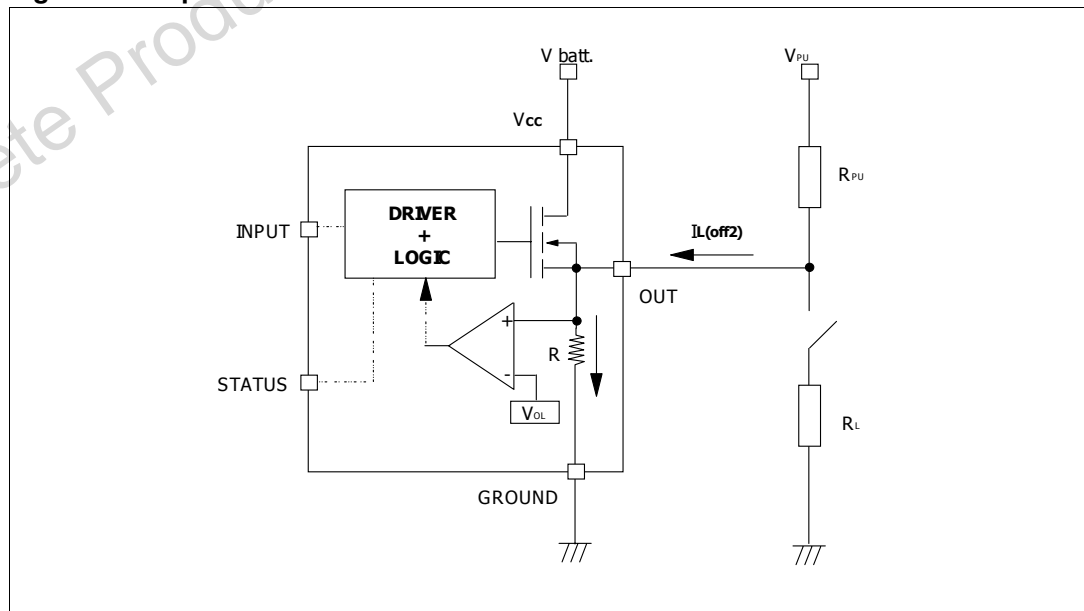
1) no false open load indication when load is connected: in this case we have to avoid V_{OUT} to be higher than V_{OLmin} ; this results in the following condition

$$V_{OUT} = (V_{PU} / (R_L + R_{PU}))R_L < V_{OLmin}.$$

2) no misdetection when load is disconnected: in this case the V_{OUT} has to be higher than V_{OLmax} ; this results in the following condition $R_{PU} < (V_{PU} - V_{OLmax}) / I_{L(off2)}$.

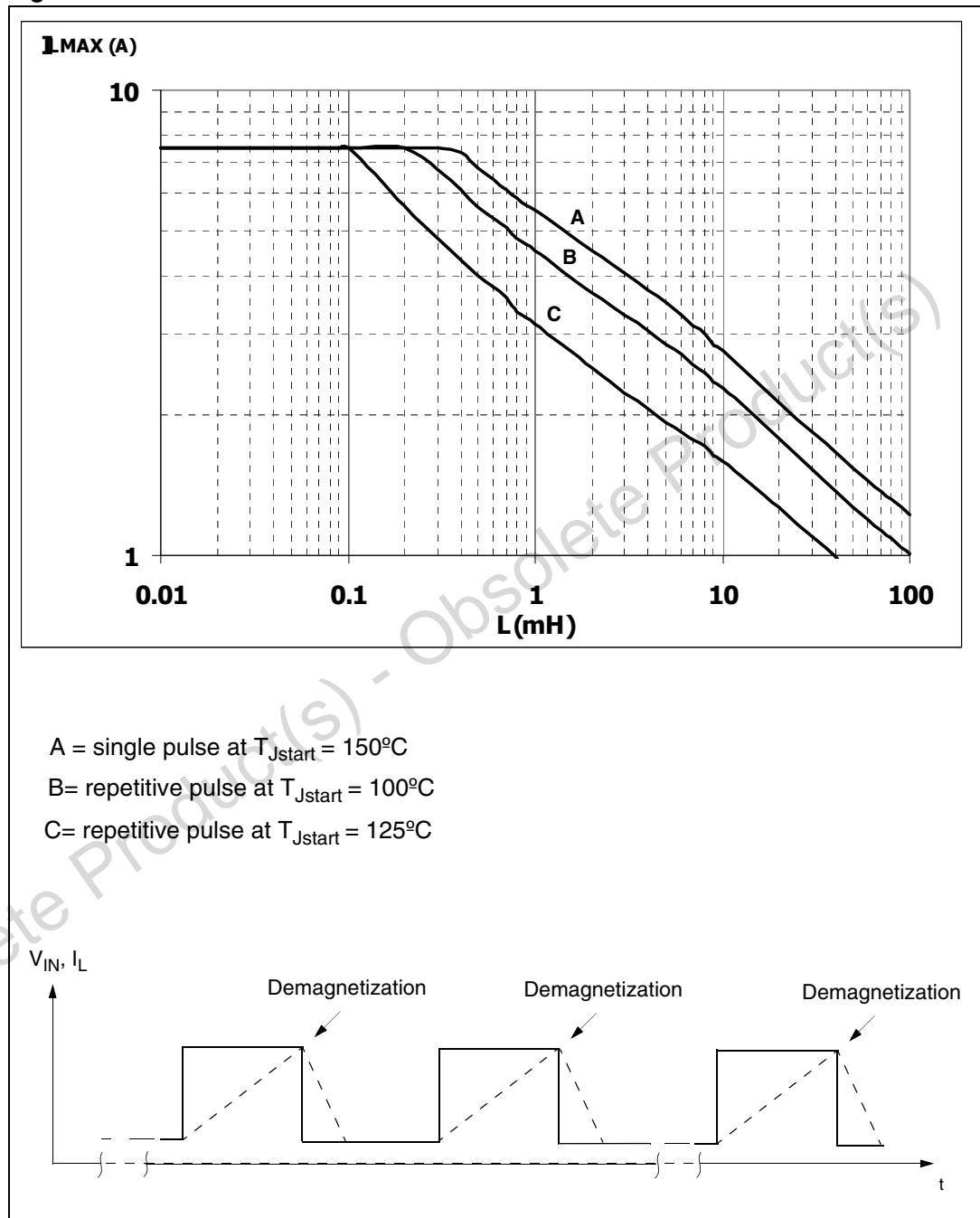
Because $I_{s(OFF)}$ may significantly increase if V_{out} is pulled high (up to several mA), the pull-up resistor R_{PU} should be connected to a supply that is switched OFF when the module is in standby.

Figure 25. Openload detection in Off state



3.5 Maximum demagnetization energy ($V_{CC} = 13.5V$)

Figure 26. Maximum turn-off current versus load inductance

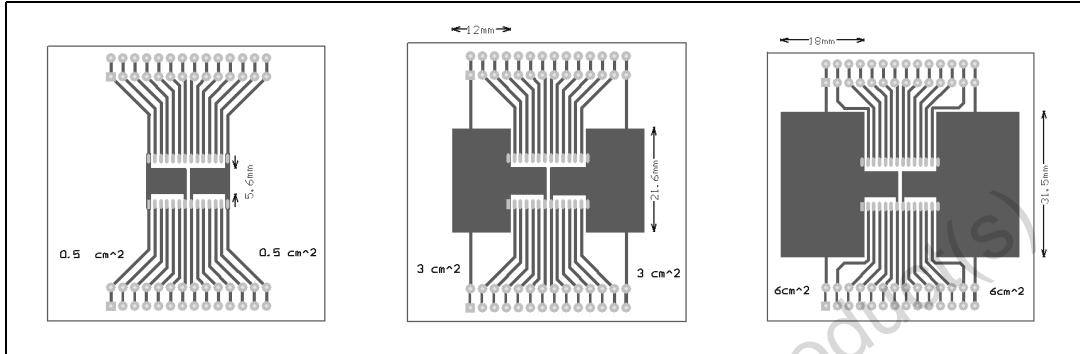


Note: Values are generated with $R_L = 0\Omega$
 In case of repetitive pulses, T_{Jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

4 Package and PCB thermal data

4.1 SO-28 thermal data

Figure 27. SO-28 PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 58mm x 58mm, PCB thickness = 2mm, Cu thickness = 35 μ m, Copper areas: 0.5 cm², 3 cm², 6 cm²).

Table 14. Thermal calculation according to the PCB heatsink area

| Chip 1 | Chip 2 | T_{jchip1} | T_{jchip2} | Note |
|--------|--------|---|---|------------------------------|
| ON | OFF | $R_{thA} \times P_{dchip1} + T_{amb}$ | $R_{thC} \times P_{dchip1} + T_{amb}$ | |
| OFF | ON | $R_{thC} \times P_{dchip2} + T_{amb}$ | $R_{thA} \times P_{dchip2} + T_{amb}$ | |
| ON | ON | $R_{thB} \times (P_{dchip1} + P_{dchip2}) + T_{amb}$ | $R_{thB} \times (P_{dchip1} + P_{dchip2}) + T_{amb}$ | $P_{dchip1} = P_{dchip2}$ |
| ON | ON | $(R_{thA} \times P_{dchip1}) + R_{thC} \times P_{dchip2} + T_{amb}$ | $(R_{thA} \times P_{dchip2}) + R_{thC} \times P_{dchip1} + T_{amb}$ | $P_{dchip1} \neq P_{dchip2}$ |

R_{thA} = thermal resistance junction to ambient with one chip ON

R_{thB} = thermal resistance junction to ambient with both chips ON and $P_{dchip1} = P_{dchip2}$

R_{thC} = mutual thermal resistance

Figure 28. $R_{thj-amb}$ Vs PCB copper area in open box free air condition

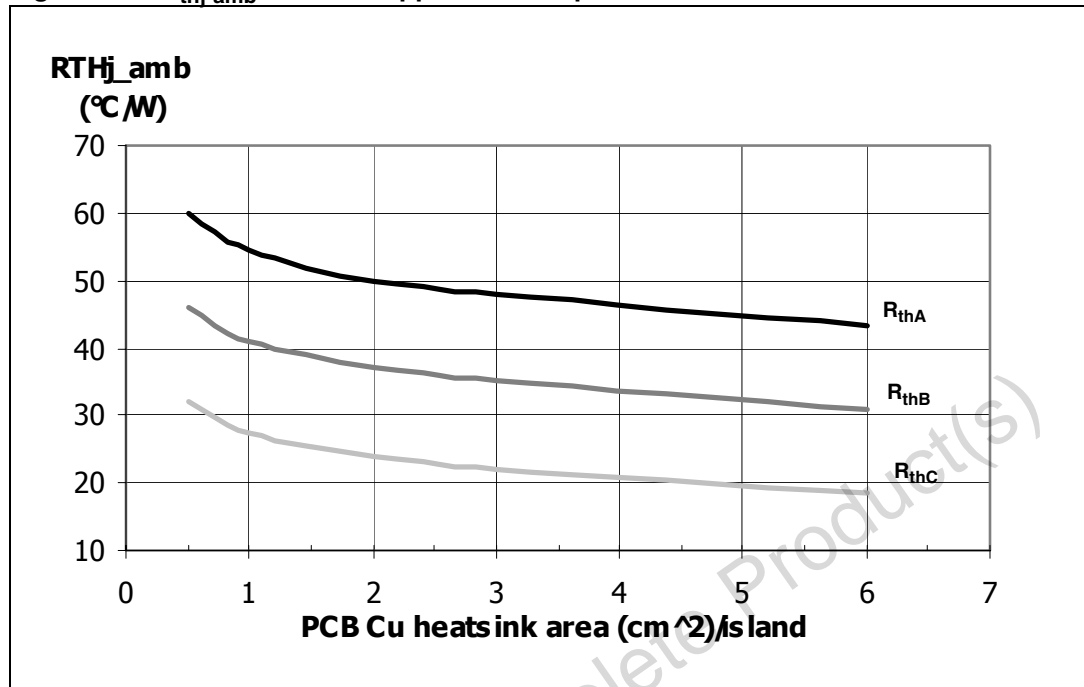
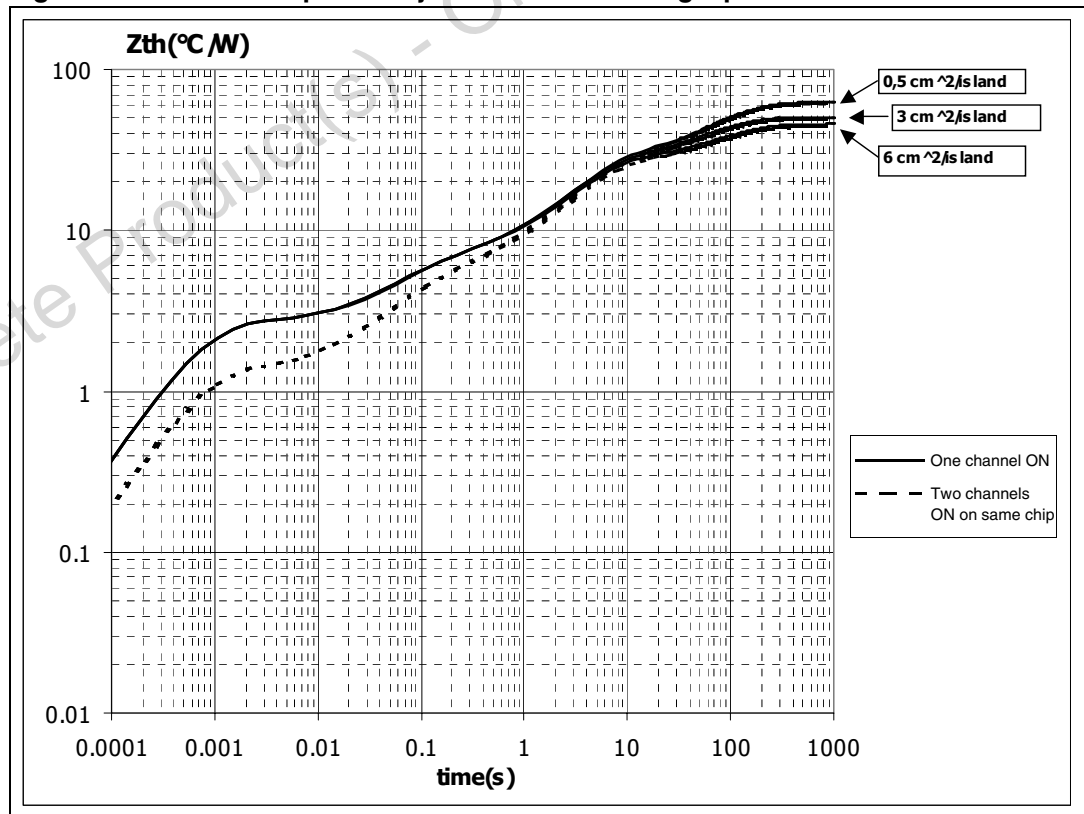


Figure 29. Thermal impedance junction ambient single pulse



Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p / T$

Figure 30. Thermal fitting model of a quad channel HSD in SO-28

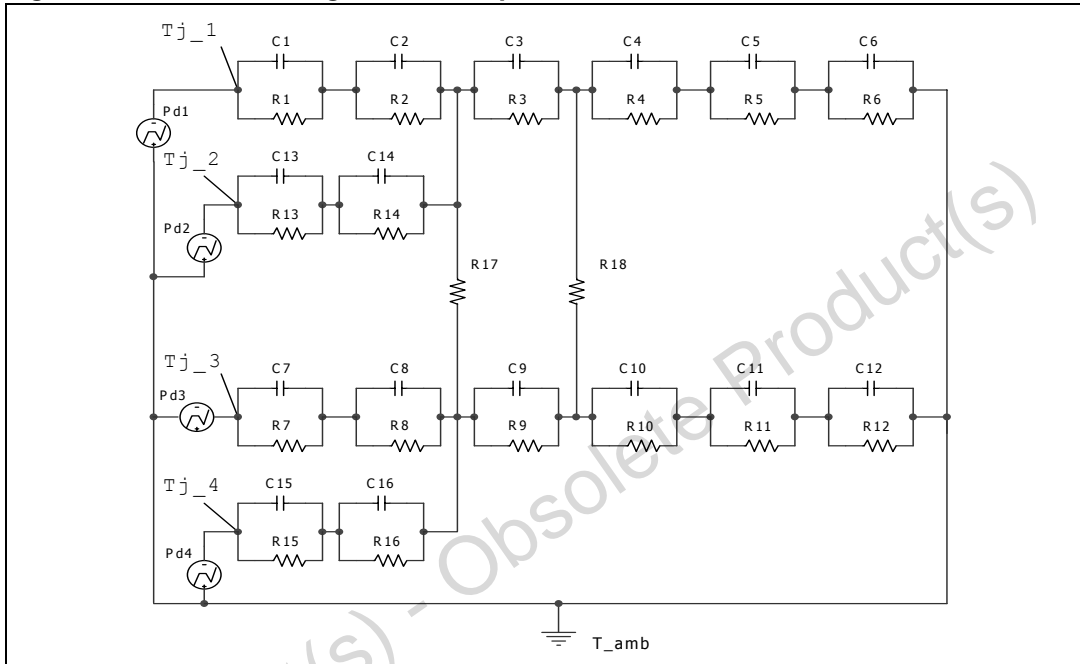


Table 15. Thermal parameters

| Area / island (cm ²) | Footprint | 6 |
|----------------------------------|-----------|----|
| R1 = R7 = R13 = R15 (°C/W) | 0.35 | |
| R2 = R8 = R14 = R16 (°C/W) | 1.8 | |
| R3 = R9 (°C/W) | 4.5 | |
| R4 = R10 (°C/W) | 11 | |
| R5 = R11 (°C/W) | 15 | |
| R6 = R12 (°C/W) | 30 | 13 |
| C1 = C7 = C13 = C15 (W.s/°C) | 0.0001 | |
| C2 = C8 = C14 = C16 (W.s/°C) | 7E-04 | |
| C3 = C9 (W.s/°C) | 6E-03 | |
| C4 = C10 (W.s/°C) | 0.2 | |
| C5 = C11 (W.s/°C) | 1.5 | |
| C6 = C12 (W.s/°C) | 5 | 8 |
| R17 = R18 (°C/W) | 150 | |

5 Package and packing information

5.1 ECOPACK[®] packages

In order to meet environmental requirements, ST offers these devices in ECOPACK[®] packages. These packages have a Lead-free second-level interconnect. The category of Second-Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 31. SO-28 package dimensions

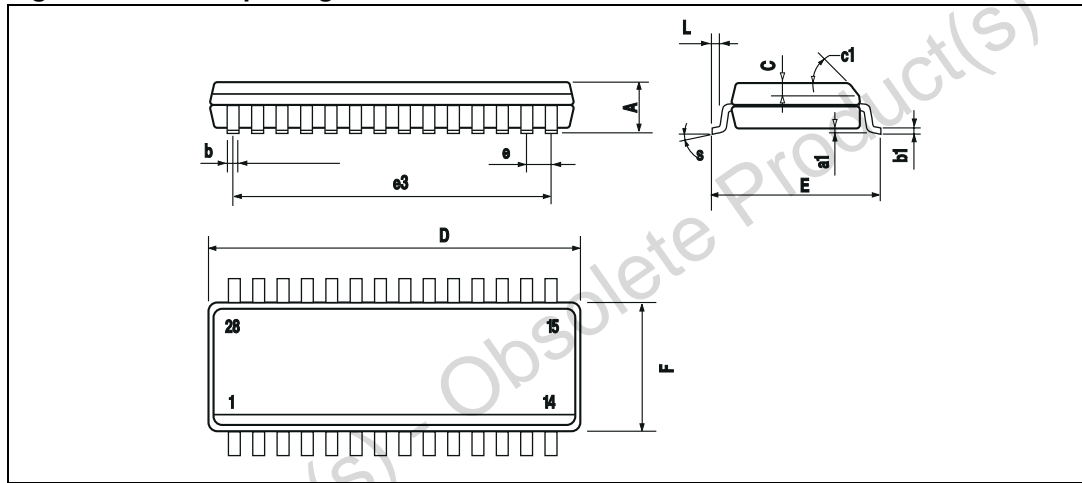


Table 16. SO-28 mechanical data

| Symbol | Millimeters | | |
|--------|-------------|-------|-------|
| | Min. | Typ. | Max. |
| A | | | 2.65 |
| a1 | 0.10 | | 0.30 |
| b | 0.35 | | 0.49 |
| b1 | 0.23 | | 0.32 |
| C | | 0.50 | |
| c1 | 45° (typ.) | | |
| D | 17.7 | | 18.1 |
| E | 10.00 | | 10.65 |
| e | | 1.27 | |
| e3 | | 16.51 | |
| F | 7.40 | | 7.60 |
| L | 0.40 | | 1.27 |
| S | 8° (max.) | | |

5.2 SO-28 packing information

Figure 32. SO-28 tube shipment (no suffix)

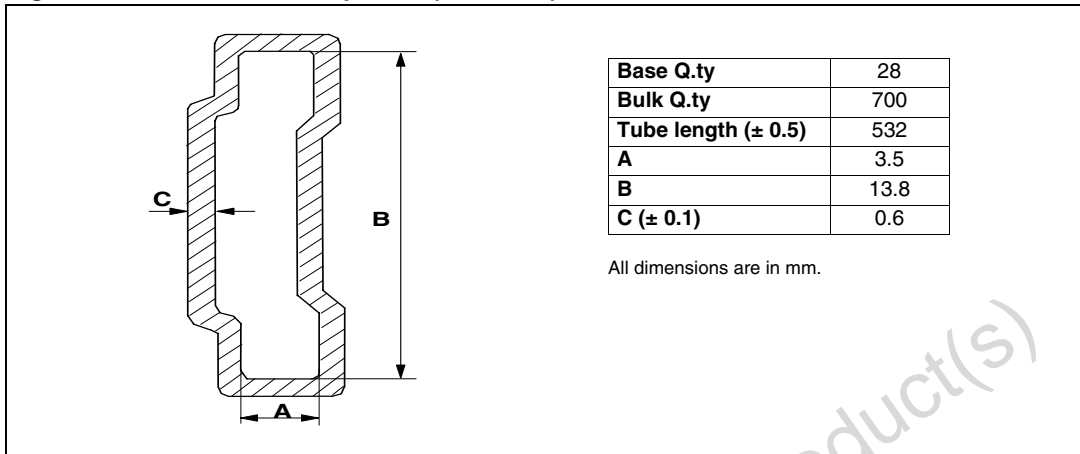
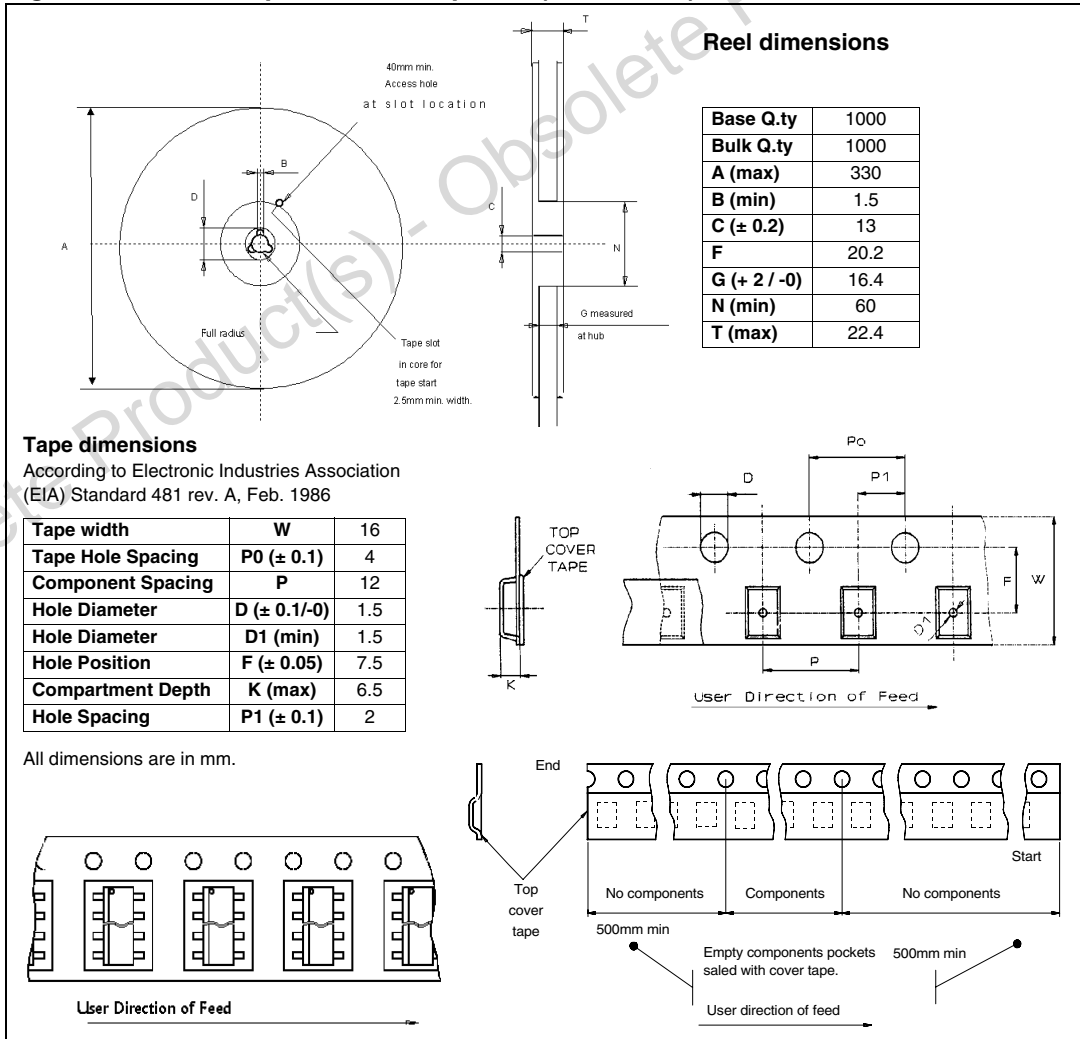


Figure 33. SO-28 tape and reel shipment (suffix “TR”)



6 Revision history

Table 17. Document revision history

| Date | Revision | Changes |
|-------------|----------|---|
| 09-Sep-2004 | 1 | Initial release. |
| 03-May-2006 | 2 | Minor changes Current and voltage convention update (page 3). Configuration diagram (top view) & suggested connections for unused and n.c. pins insertion (page 3). 6 cm ² Cu condition insertion in thermal data table (page 4). V _{CC} - output diode section update (page 4). Protections note insertion (page 5) Revision history table insertion (page 20). Disclaimers update (page 21). |
| 01-Dec-2008 | 3 | Document reformatted and restructured. Added contents, list of tables and figures. Added <i>ECOPACK</i> [®] packages information. |
| 25-Sep-2013 | 4 | Updated disclaimer. |

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER'S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR "AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL" INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2013 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com



X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for [Gate Drivers](#) category:

Click to view products by [STMicroelectronics](#) manufacturer:

Other Similar products are found below :

[00053P0231](#) [8967380000](#) [56956](#) [CR7E-30DB-3.96E\(72\)](#) [57.404.7355.5](#) [LT4936](#) [57.904.0755.0](#) [5803-0901](#) [58410](#) [5882900001](#) [00600P0005](#)
[00-9050-LRPP](#) [00-9090-RDPP](#) [5951900000](#) [01-1003W-10/32-15](#) [LTLA6E-1S-WH-RC-FN12VXCR1](#) [0131700000](#) [00-2240](#) [LTP70N06](#)
[LVP640](#) [0158-624-00](#) [5J0-1000LG-SIL](#) [020017-13](#) [LY1D-2-5S-AC120](#) [LY2-0-US-AC120](#) [LY2-US-AC240](#) [LY3-UA-DC24](#) [00-5150](#)
[00576P0020](#) [00600P0010](#) [LZNQ2M-US-DC5](#) [LZNQ2-US-DC12](#) [LZP40N10](#) [00-8196-RDPP](#) [00-8274-RDPP](#) [00-8275-RDNP](#) [00-8609-](#)
[RDPP](#) [00-8722-RDPP](#) [00-8728-WHPP](#) [00-8869-RDPP](#) [00-9051-RDPP](#) [00-9091-LRPP](#) [00-9291-RDPP](#) [0207100000](#) [0207400000](#) [60100564](#)
[01312](#) [0134220000](#) [6035](#) [M15730061](#)