



SK5129 Product Description

Rev 0.9.4 July 24, 2018

This datasheet is intended for customer's evaluation and application of the SK5129 device. Under no circumstances it should be circulated outside the customer's company. This datasheet is preliminary and SunTek reserves the right to modify and to improve the data.

PRODUCT DESCRIPTION

SK5129 is a high-gain, low-noise amplifier (LNA) designed for GPS, Galileo, Glonass and Beidou GNSS applications. Designed in a standard low-cost RF CMOS process, the LNA achieves up to 30dB gain and 1dB noise figure. SK5129 forms the optimal RF front-end for the reception of GNSS satellites. Packaged in a 6-pin μ DFN package, the SK5129 sits on a small form factor PCB space. It can operate from a 1.6V to 3.6V single supply and draws only 6.5mA DC current. The shutdown leakage current is only 1uA.

FEATURES

- Ultra-low-noise figure of 1dB
- High-power gain up to 30dB
- Integrated 50-Ohm output matching circuit
- Low-power of 6.5mA operated from a single 1.6V to 3.6V voltage
- Small footprint of 1.6mmx1.6mm
- Thin profile of 0.55mm
- Lead-free and RoHS-compliant package
- High integration with few off-chip BOM and low cost
- Temperature from -40° to 85° range

APPLICATIONS

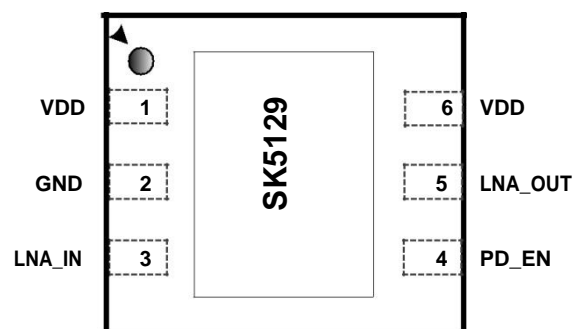
- PNDs (Personal Navigation Devices)
- Location-Enabled MID
- PMPs (Personal Media Players)
- Automobile Navigation Systems
- GNSS tracking systems
- GNSS industrial applications
- Software GPS
- iPad like Mobile PCs

TECHNOLOGY

- Device in DFNWB1.6x1.6-6L package, pin compatible with the 6-pin plastic TSOP
- RoHS-compliant package
- Low noise linear regulator for power management
- Silicon CMOS 0.18um process with 1.8/3.3V operation

PIN ASSIGNMENT

PIN 1 Mark



PIN CONNECTIONS AND INTERNAL BLOCK DIAGRAM

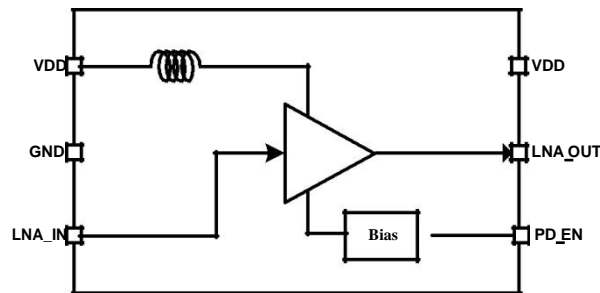


Figure 1 Block Diagram for LNA

Pin Out Description

Pin No.	Name	Description	Connection
1	VDD	power supply for LNA	Supply Voltage.
2	GND	Ground connection	Connect to PCB ground plane.
3	LNA_IN	RF Input	Requires a DC-blocking capacitor and external matching components.
4	PD_EN	Shutdown Input	A logic-low disables the device.
5	LNA_OUT	RF Output	Requires a DC-blocking capacitor and external matching components.
6	VDD	power supply for LNA	Supply Voltage.
Die Pad	GND	Ground connection	Main IC GND connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Supply Voltage	VDD	$T_A=+25^{\circ}\text{C}$		4.0	V
Power Down Voltage	V _{PD_EN}	$T_A=+25^{\circ}\text{C}$		4.0	V
LNA Max RF Input Power	P _{in}			0	dBm
ESD: HBM, 150pF/1.5KOhm	-		2.5		kV
Storage Temperature	T _{STG}		-40	+150	°C
Solder Reflow Temperature	T _{SLDR}			+260	°C

This device should be handled with care within the above stress ratings. This IC has ESD protection circuits within but must be handled and assembled according to the industry practice and at the ESD protected work platforms.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Ambient Operating Temperature	T _A	-40	+25	+85	°C
Supply Voltage	VDD	1.6	2.7	3.6	V
Power Down Turn-on Voltage	V _{PD_on}	1.6	-	VDD	
Power Down Turn-off Voltage	V _{PD_off}	0	-	0.4	V

ELECTRICAL CHARACTERISTICS

($T_A = +25^{\circ}\text{C}$, VDD= V_{PD_EN} = 2.7V, f_{in} = 1 575.42MHz, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
circuit current	I _{cc}	No Signal	5.0	6.5	8.0	mA
Power Gain (Note1)	G _p	Pin=-35dBm	28	30	32	dB
Noise Figure	NF		-	0.85	1.2	dB
Input Return Loss	RL _{in}		-	10	-	dB
Output Return Loss	RL _{out}		12	15	-	dB

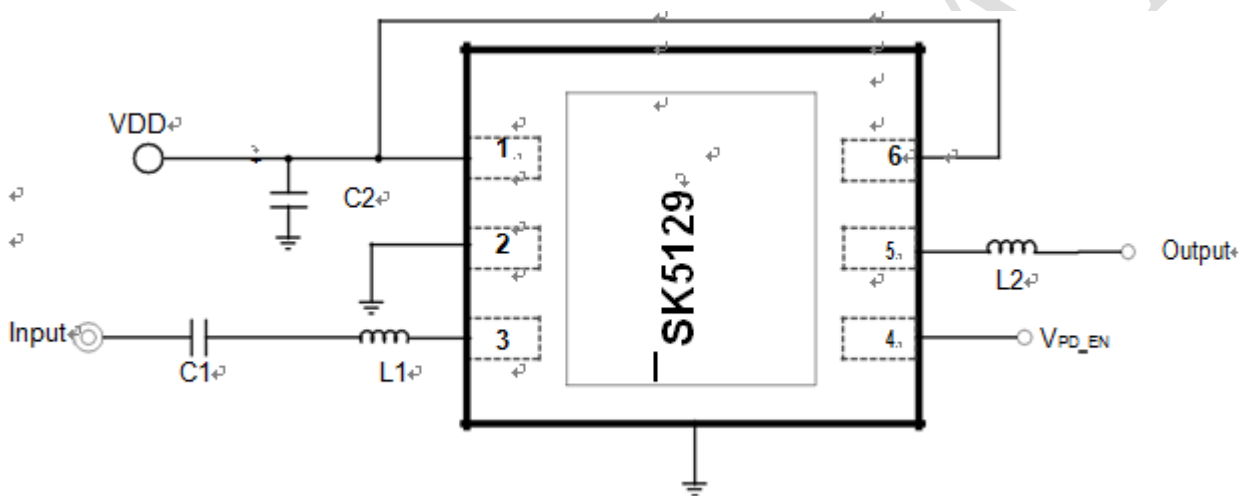
Note1: If low gain is needed modify output inductor value.

STANDARD CHARACTERISTICS FOR REFERENCE

($T_A = +25^{\circ}\text{C}$, $V_{DD} = V_{PD_EN} = 2.7\text{V}$, $f_{in} = 1\,575.42\text{MHz}$, unless otherwise specified)

Parameter	Symbol	Test Conditions	Reference	Unit
Isolation	ISL		45	dB
Input 3rd Order Distortion Intercept Point	IIP ₃	$f_{in1} = 1\,575\text{ MHz}$ $f_{in2} = 1\,574\text{ MHz}$	-15	dBm
Gain 1 dB Compression Input Power	$P_{in(1dB)}$		-25	dBm

Typical Application Diagram



BOM LIST

BOM Descriptions	Symbol	Size	Value	Unit
Chip Capacitor	C1	0402	100	pF
Chip inductor	L1	0402	8.2	nH
Chip Capacitor	L2	0402	10	nH
Chip Capacitor	2	0402	10	nF

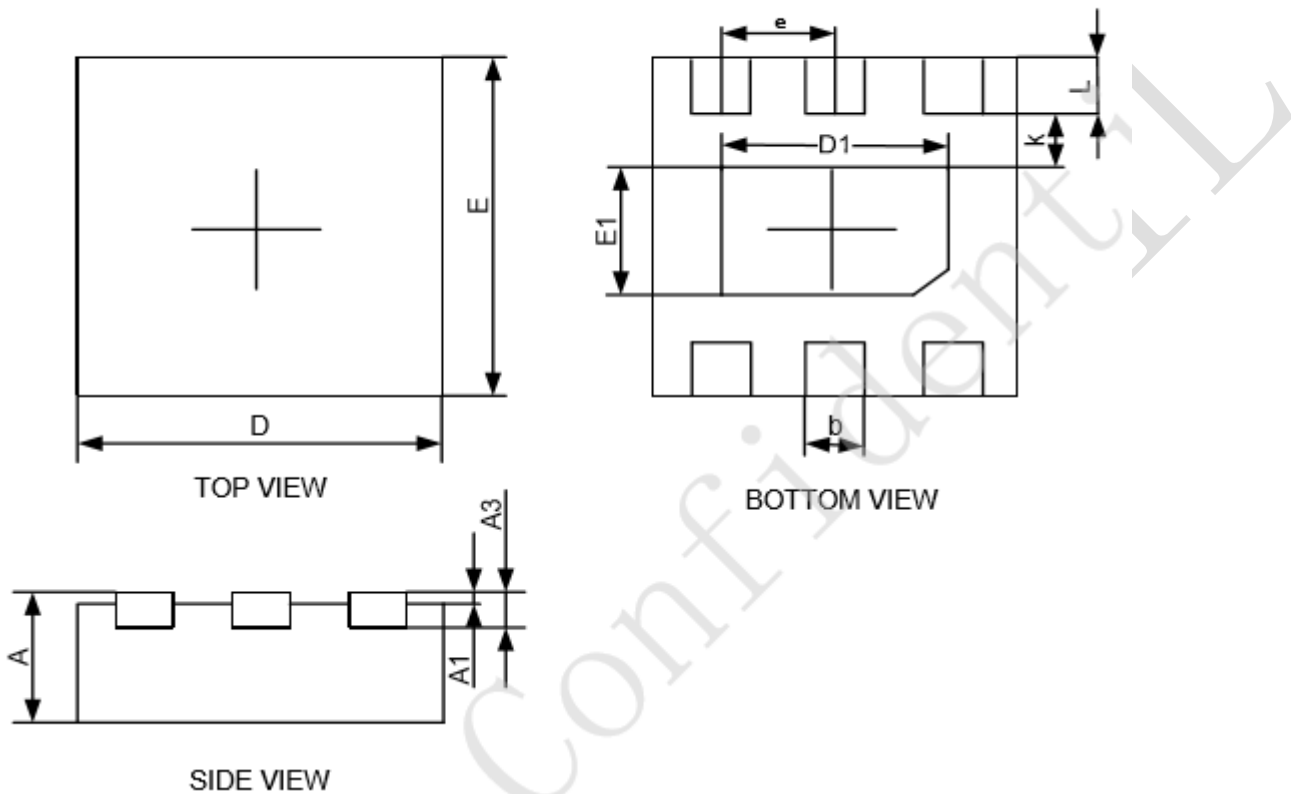
These component values are for reference only and are subject to change with customer specific PCB layout design.

PACKAGE DIMENSIONS

*Pin compatible with 6-pin plastic TSON

DFNWB1.6X1.6—6L(P0.50T0.50/0.60)

PACKAGE OUTLINE DIMENSIONS



symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.450 / 0.550	0.550 / 0.650	0.018 / 0.022	0.022 / 0.026
A1	0.000	0.050	0.000	0.002
A3	0.152REF.		0.006REF.	
D	1.550	1.650	0.061	0.065
E	1.550	1.650	0.061	0.065
E1	0.550	0.650	0.022	0.026
D1	0.950	1.050	0.037	0.041
k	0.200MIN.		0.008REF.	
b	0.200	0.300	0.008	0.012
e	0.500BSC.		0.020BSC.	
L	0.164	0.316	0.006	0.012

RECOMMENDED REFLOW PROFILE

Table2 Reflow Test Condition

Profile Feature	Pb-Free Assembly
Preheat & Soak	
Temperature min (T _{smin})	150°C
Temperature max (T _{smax})	200°C
Time (T _{smin} to T _{smax})(t _s)	60-120 seconds
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.
Liquidous temperature (TL)	217°C
Time at liquidous (tL)	60-150 seconds
Peak package body temperature (T _p) *	See classification temp in Table 3
Time (t _p)** within 5°C of the specified classification temperature (T _c)	30**seconds
Average ramp-down rate (T _p to T _{smax})	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

Remark: All temperatures refer to the package body surface temperature. The highest temperature of reflow profile can not exceed 265°C.

Note 1: All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), T_p shall be within $\pm 2^{\circ}\text{C}$ of the live-bug T_p and still meet the T_c requirements, otherwise, the profile shall be adjusted to achieve the latter. To accurately measure actual peak package body temperatures refer to JEP140 for recommended thermocouple use.

Note 2: Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table 2. For example, if T_c is 260°C and time t_p is 30 seconds, this means the following for the supplier and the user. For a supplier: The peak temperature must be at least 260°C. The time above 255°C must be at least 30 seconds. For a user: The peak temperature must not exceed 260°C. The time above 255°C must not exceed 30 seconds.

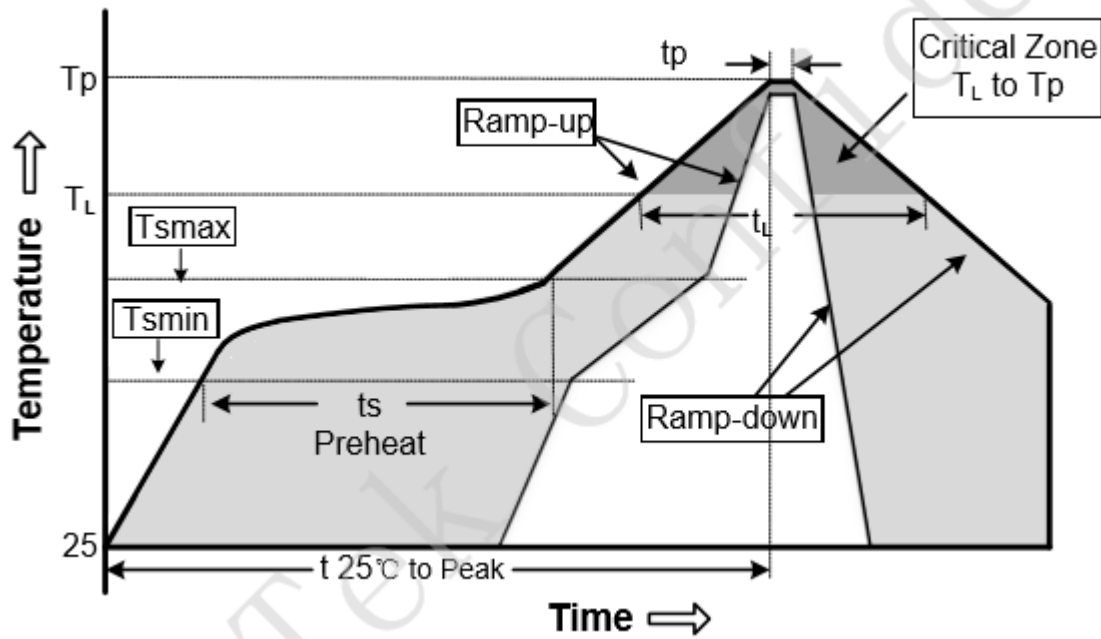
Note 3: All components in the test load shall meet the classification profile requirements.

Note 4: SMD packages classified to a given moisture sensitivity level by using Procedures or Criteria defined within any previous version of J-STD-020, JESD22-A112 (rescinded), IPC-SM-786 (rescinded) do not need to be reclassified to the current revision unless a change in classification level or a higher peak classification temperature is desired.

Table 3 Pb-Free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm ³ < 350	Volume mm ³ 350 - 2000	Volume mm ³ > 2000
< 1.6 mm	260°C	260°C	260°C
1.6 mm - 2.5 mm	260°C	250°C	245°C
> 2.5 mm	250°C	245°C	245°C

Reflow Profile



The reflow profile shown above should not be exceeded, since excessive temperatures or transport times during reflow can damage the chip.

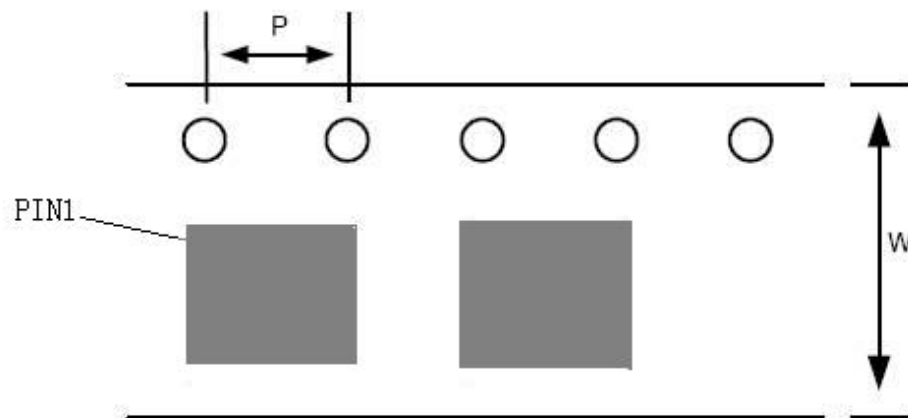
PACKING SPEC

PKG	TAPE	REEL	BOX	PCS/REEL	REEL/BOX	PCS/BOX	BOX/CARTON	PCS/CARTON
DFN1.6x1.6	IC-ZD-78-1	7" IC-JP-05	TR-1-01	3000	10	30000	4	120000

■ Tape & Reel Dimension

$P = 4 \text{ mm}$

$W = 8 \text{ mm}$



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