



SUPER-SEMI



## SUPER-MOSFET

Super Junction Metal Oxide Semiconductor Field Effect Transistor

800V Super Junction Power MOSFET  
SS\*80R850S

Rev. 1.5  
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# SSF80R850S/SSP80R850S/SST80R850S/SSU80R850S 800V N-Channel MOSFET

## Description

SSMOS-FET is new generation of high voltage MOSFET family that is utilizing an advanced charge balance mechanism for outstanding low on-resistance and lower gate charge performance. This advanced technology has been tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate and higher avalanche energy. SJ-FET is suitable for various AC/DC power conversion in switching mode operation for higher efficiency.

## Features

- Multi-Epi process SJ-FET
- 850V @T<sub>J</sub> = 150 °C
- Typ. R<sub>DS(on)</sub> = 0.8Ω ( TO-220F )
- Ultra Low Gate Charge (typ. Q<sub>g</sub> = 9.5nC)
- 100% avalanche tested

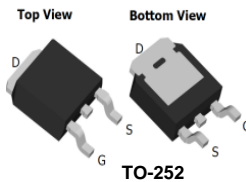
SSF80R850S



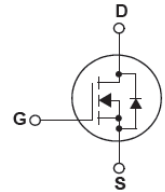
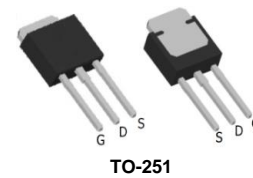
SSP80R850S



SST80R850S



SSU80R850S



## Absolute Maximum Ratings

Symbol	Parameter	SSP_T_U80R850S	SSF80R850S	Unit
V <sub>DSS</sub>	Drain-Source Voltage	800		V
I <sub>D</sub>	Drain Current -Continuous (TC = 25°C) -Continuous (TC = 100°C)	6.6* 4.2*		A
I <sub>DM</sub>	Drain Current - Pulsed (Note 1)	20*		A
V <sub>GSS</sub>	Gate-Source voltage	±30		V
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note 2)	86		mJ
I <sub>AR</sub>	Avalanche Current (Note 1)	1.7		A
E <sub>AR</sub>	Repetitive Avalanche Energy (Note 1)	0.2		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	15		V/ns
dVds/dt	Drain Source voltage slope (V <sub>ds</sub> =640V)	50		V/ns
P <sub>D</sub>	Power Dissipation (TC = 25°C)	63	28	W
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range	-55 to +150		°C
T <sub>L</sub>	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300		°C

\* Drain current limited by maximum junction temperature. Maximum duty cycle D=0.75.

## Thermal Characteristics

Symbol	Parameter	SSP_T_U80R850S	SSF80R850S	Unit
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case	2.0	4.5	°C/W
R <sub>θCS</sub>	Thermal Resistance, Case-to-Sink Typ.	0.5	-	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient	62	80	°C/W



# Electrical Characteristics TC = 25°C unless otherwise noted

SSF80R850S/SSP80R850S/SST80R850S/SSU80R850S 800V N-Channel MOSFET

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA, T <sub>J</sub> = 25°C	800	-	-	V
		V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA, T <sub>J</sub> = 150°C	-	850	-	V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250μA, Referenced to 25°C	-	0.6	-	V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 800V, V <sub>GS</sub> = 0V -T <sub>J</sub> = 150°C	-	- 10	1 -	μA μA
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30V, V <sub>DS</sub> = 0V	-	-	100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30V, V <sub>DS</sub> = 0V	-	-	-100	nA
<b>On Characteristics</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	2.5	3.5	4.5	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 3.5A (TO-220F/TO-220)	-	0.8	0.9	Ω
		V <sub>GS</sub> = 10V, I <sub>D</sub> = 3.5A (TO-251/TO-252)	-	0.85	0.93	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 40V, I <sub>D</sub> = 7A	-	6	-	S
<b>Dynamic Characteristics</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25V, V <sub>GS</sub> = 0V, f = 1MHz	-	380	-	pF
C <sub>oss</sub>	Output Capacitance		-	115	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		-	9	-	pF
<b>Switching Characteristics</b>						
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 400V, I <sub>D</sub> = 3.5A, R <sub>G</sub> = 25Ω(Notes 4)	-	23	-	ns
t <sub>r</sub>	Turn-On Rise Time		-	19	-	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		-	44	-	ns
t <sub>f</sub>	Turn-Off Fall Time		-	18	-	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 450V, I <sub>D</sub> = 3.5A, V <sub>GS</sub> = 10V (Note 4)	-	9.5	-	nC
Q <sub>gs</sub>	Gate-Source Charge		-	1.9	-	nC
Q <sub>gd</sub>	Gate-Drain Charge		-	4.5	-	nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current		-	-	7	A
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current		-	-	20	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0V, I <sub>S</sub> = 7A	-	0.9	1.5	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>R</sub> = 400V, V <sub>GS</sub> = 0V, I <sub>F</sub> = 7A, di/dt = 100A/μs	-	550	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge		-	4.8	-	μC
I <sub>rrm</sub>	Peak reverse recovery Current		-	15.5	-	A

**NOTES:**

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. I<sub>AS</sub> = 1.7A, V<sub>DD</sub> = 50V, Starting T<sub>J</sub> = 25 °C
3. I<sub>SD</sub> ≤ I<sub>D</sub>, di/dt ≤ 200A/μs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, Starting T<sub>J</sub> = 25 °C
4. Essentially Independent of Operating Temperature Typical Characteristics

# Typical Performance Characteristics

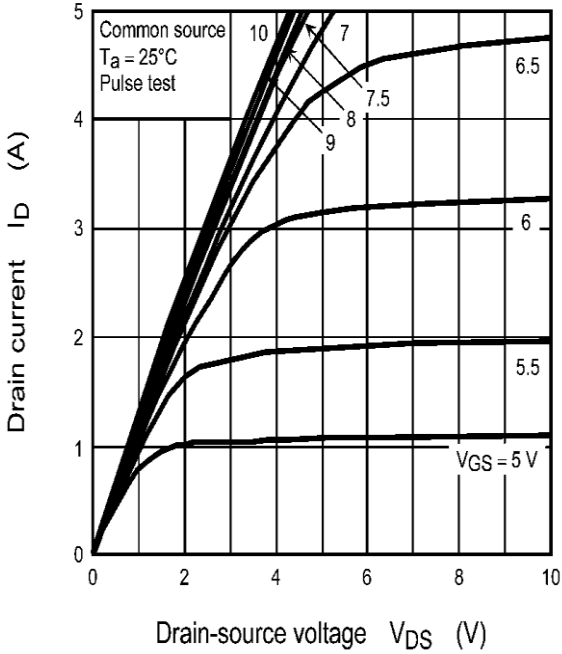


Figure 1: On-Region Characteristics@25°C

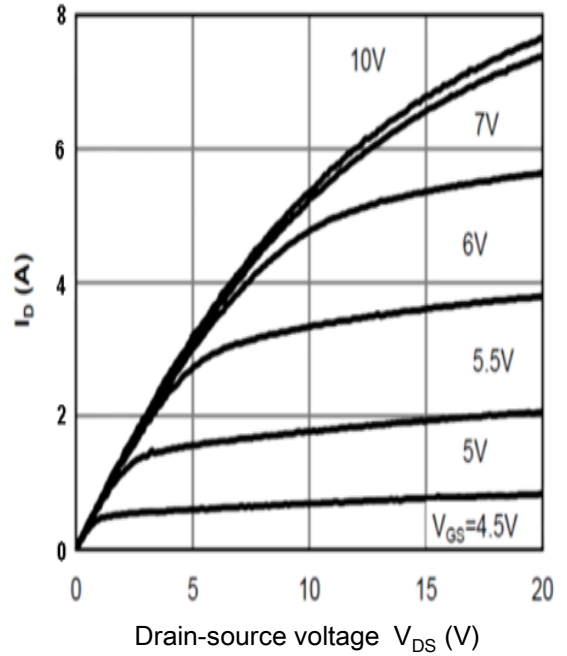


Figure 2: On-Region Characteristics@125°C

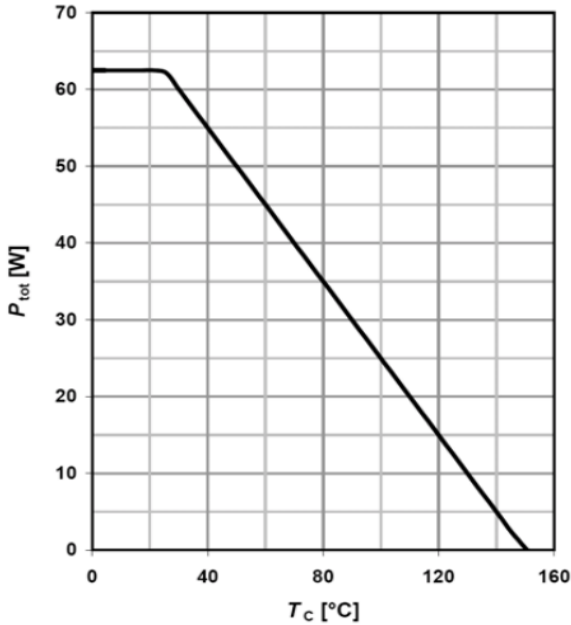


Figure 3: Power Dissipation  
 TO-220, TO-252, TO-251

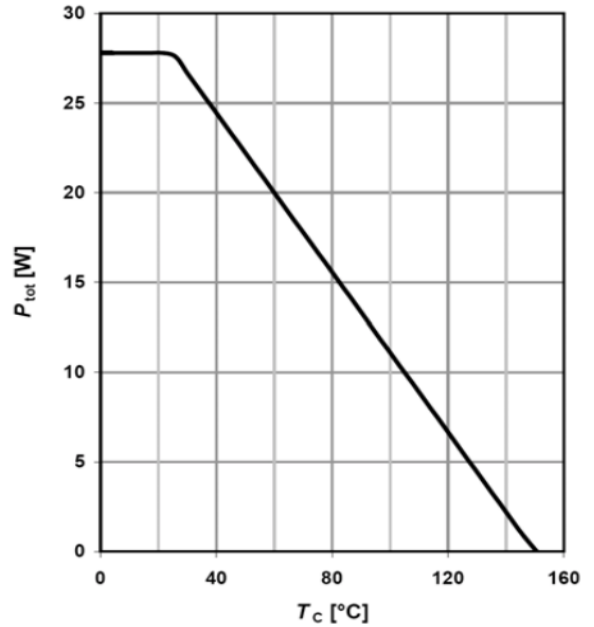


Figure 4 : Power dissipation  
 TO-220FullPAK

# Typical Performance Characteristics

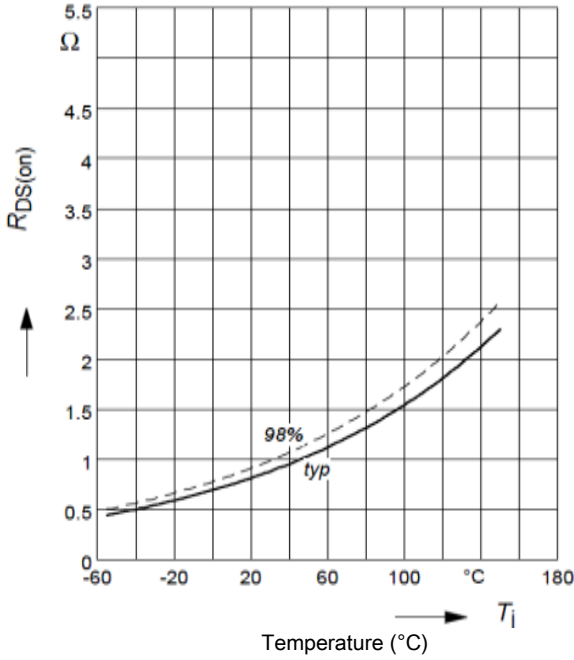


Figure 5: On-Resistance vs. Junction Temperature  
TO-220FullPAK

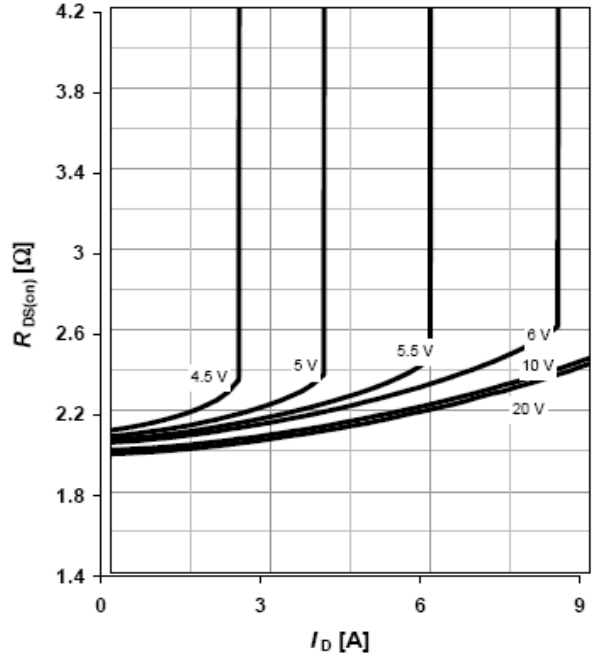


Figure 6: On-Resistance vs. Drain Current,  $T_j=150^{\circ}\text{C}$

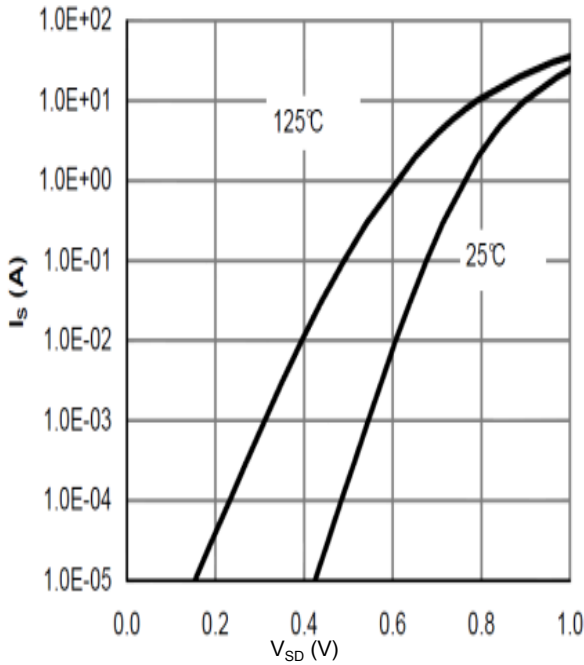


Figure 7: Body-Diode Characteristics

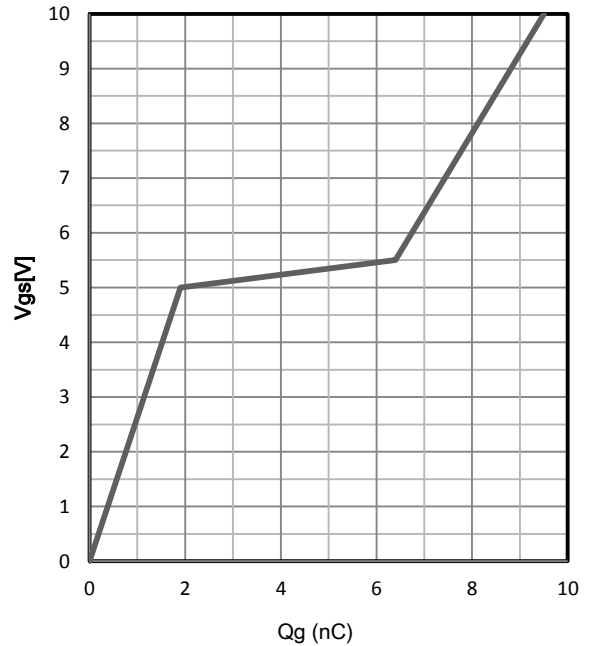


Figure 8: Gate-Charge Characteristics

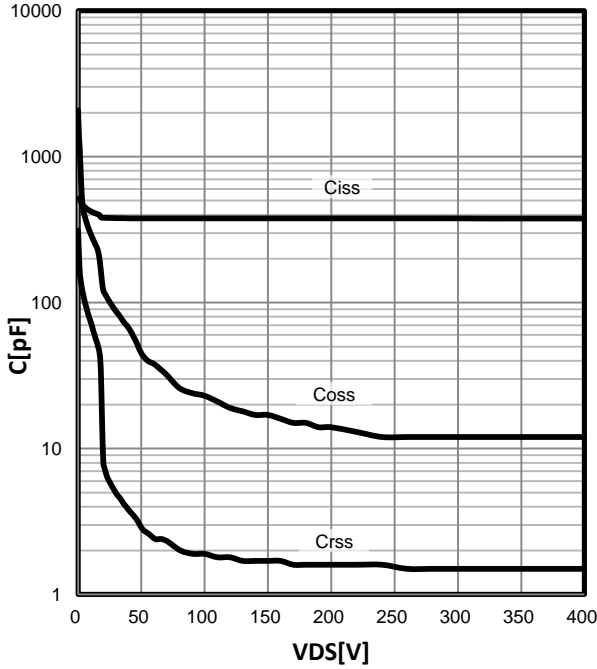


Figure 9: Capacitance Characteristics

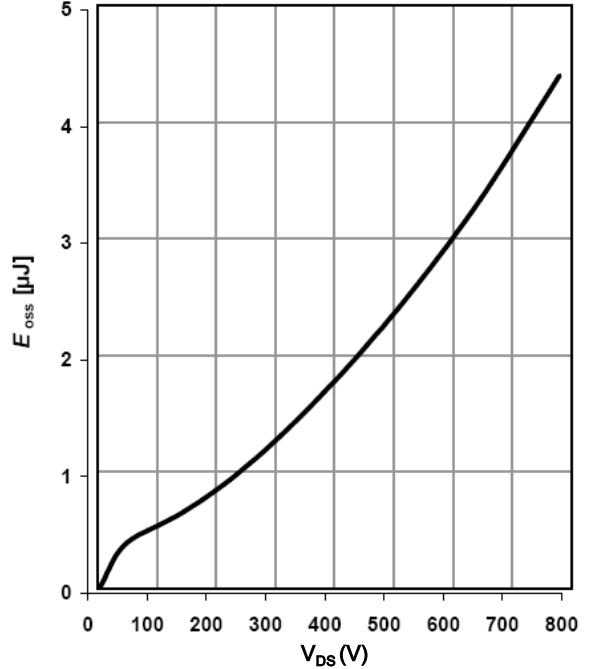


Figure 10:  $C_{oss}$  stored Energy

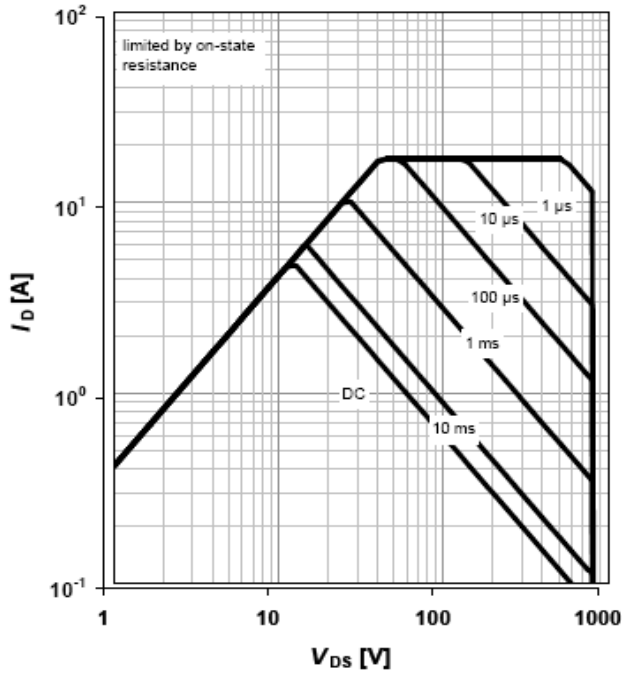


Figure 11: Maximum Forward Biased Safe Operating Area  
Tc=25°C (TO-220, TO-252, TO-251)

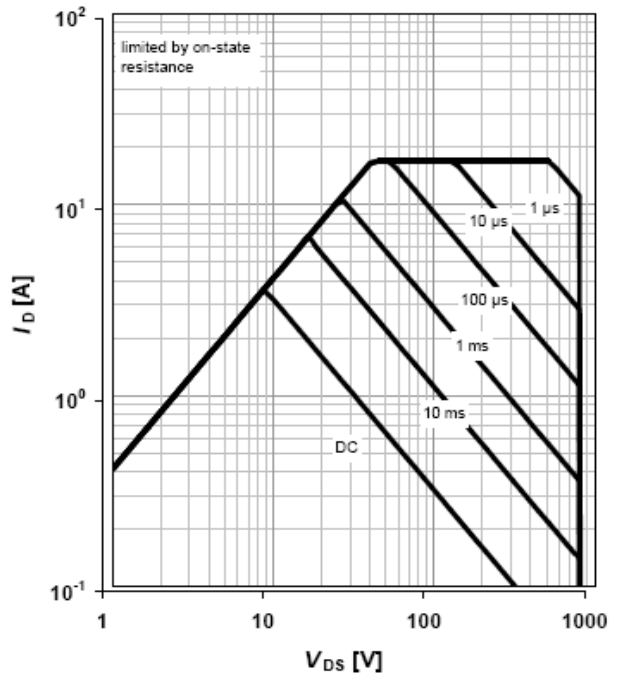


Figure 12: Maximum Forward Biased Safe Operating Area  
Tc=25°C (TO-220 FullPAK )

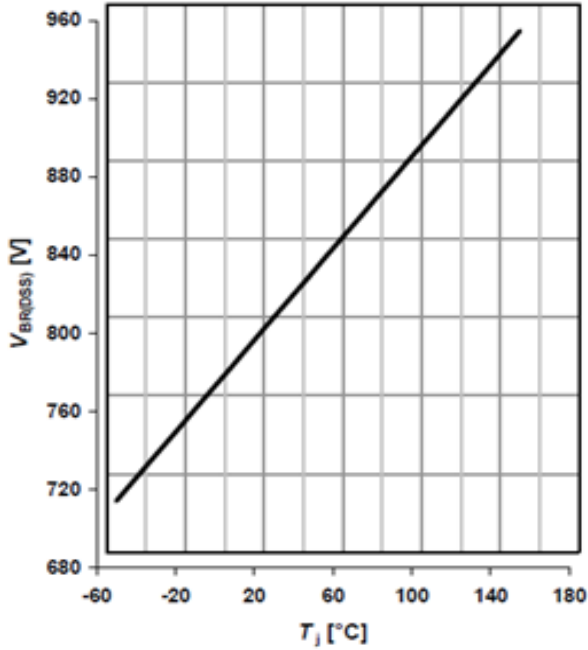


Figure 13: Break Down vs. Junction Temperature

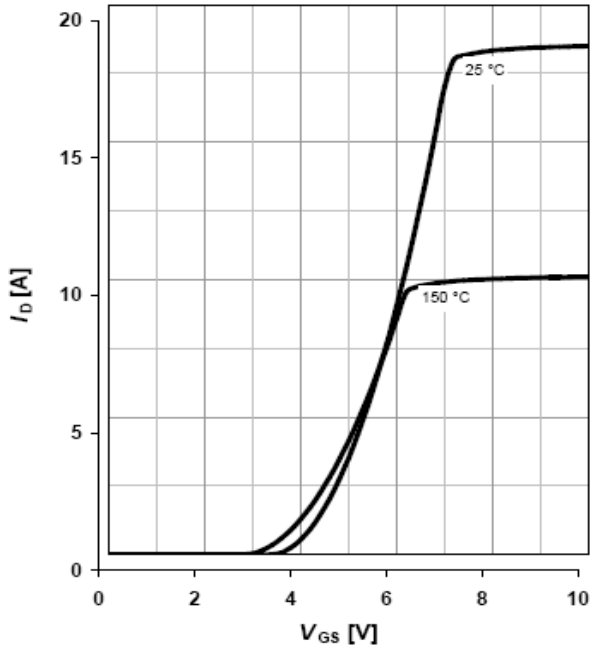


Figure 14: Typical transfer characteristics

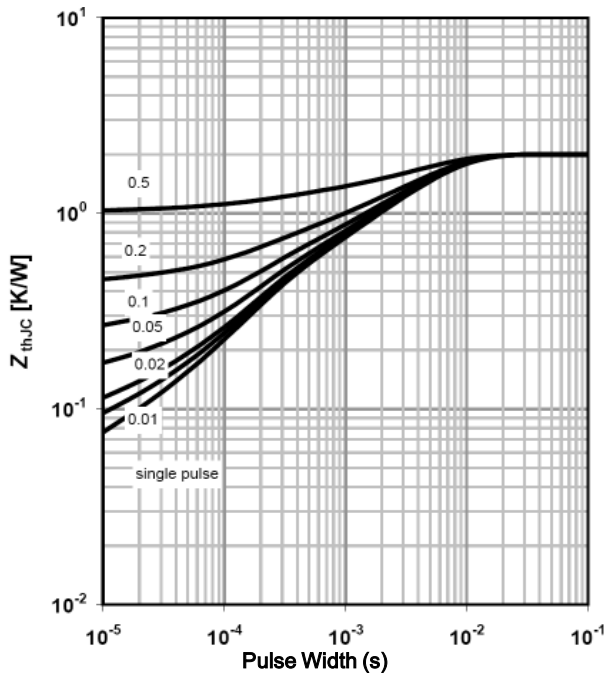


Figure 15: Maximum Transient Thermal Impedance  
TO-220, TO-252, TO-251

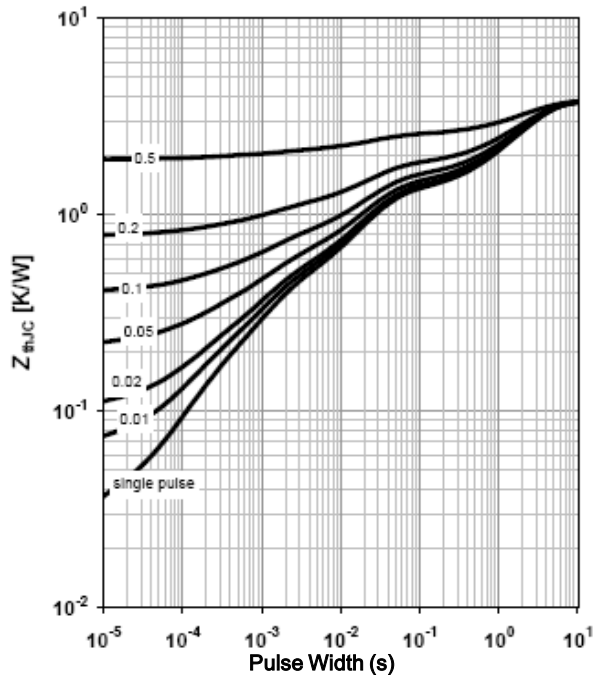


Figure 16: Maximum Transient Thermal Impedance  
TO-220 FULLPAK

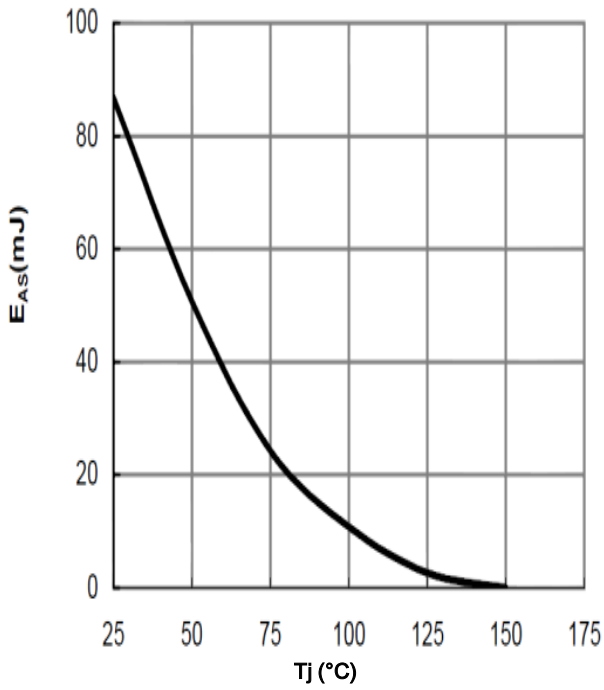
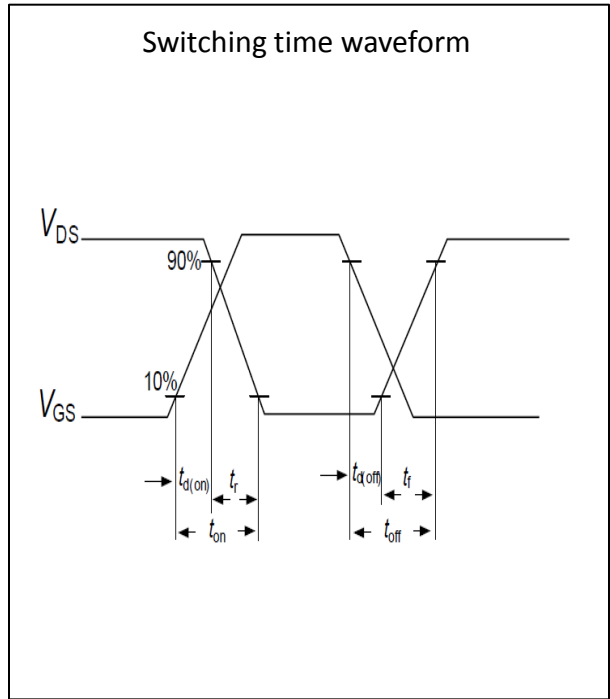
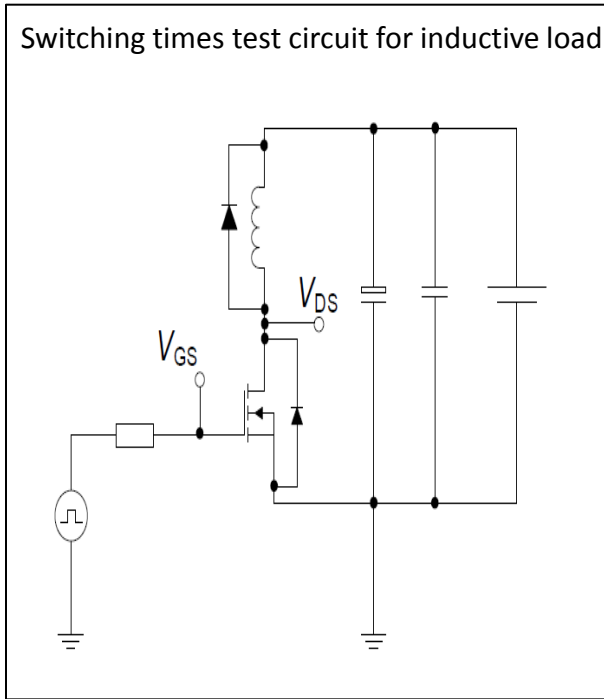


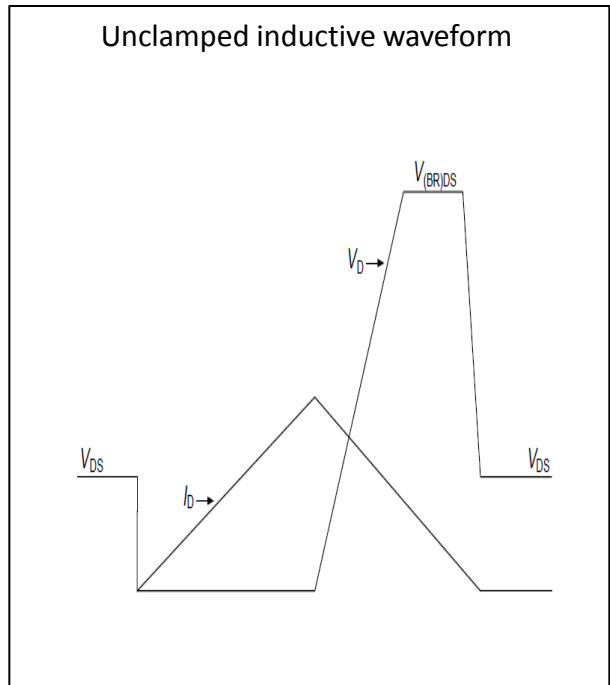
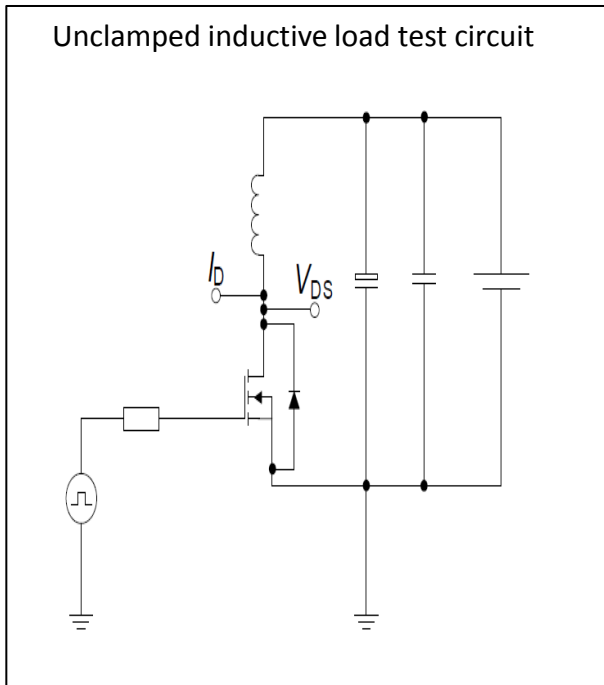
Figure 17: Avalanche energy



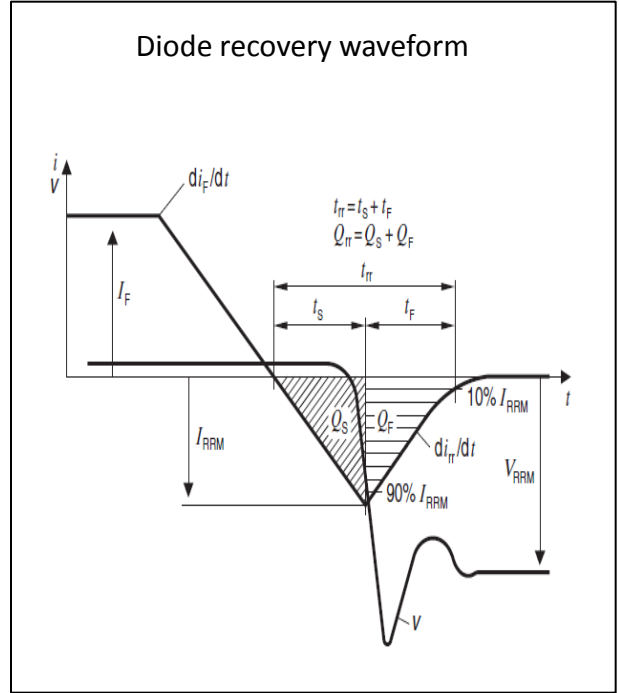
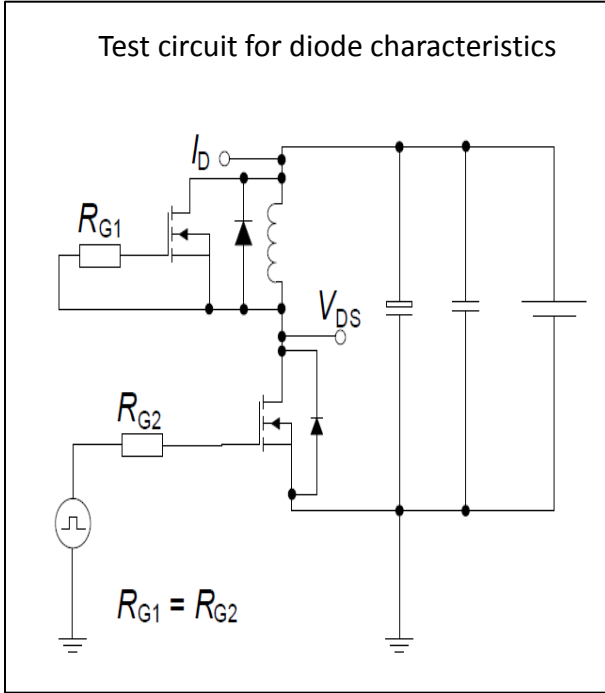
Switching times test circuit and waveform for inductive load

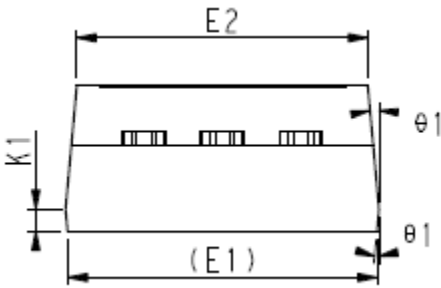
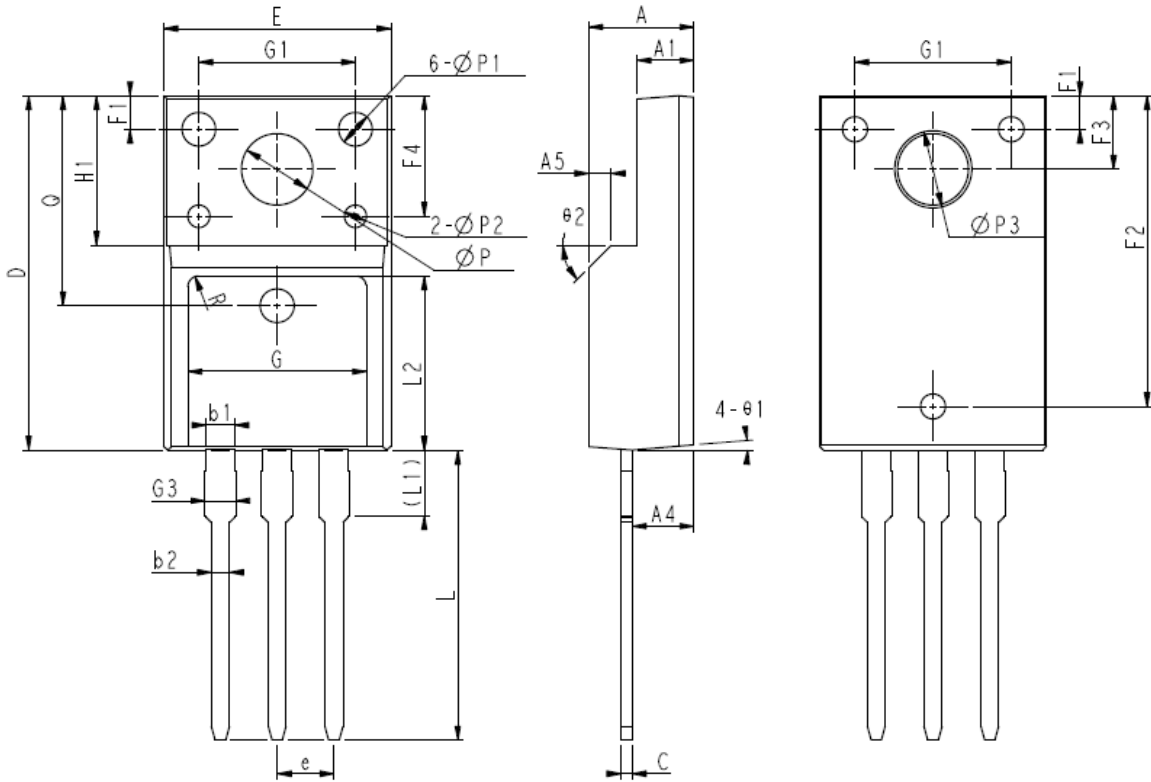


Unclamped inductive load test circuit and waveform



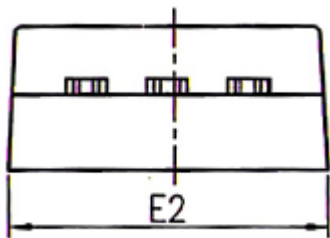
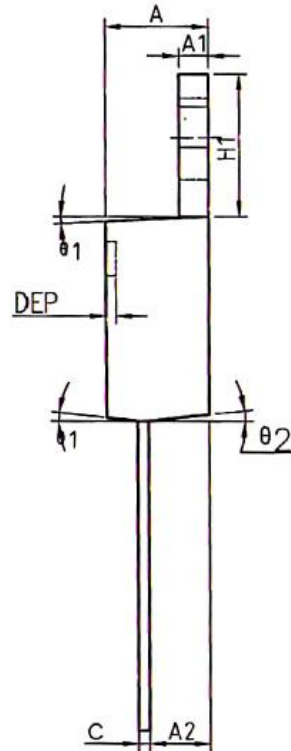
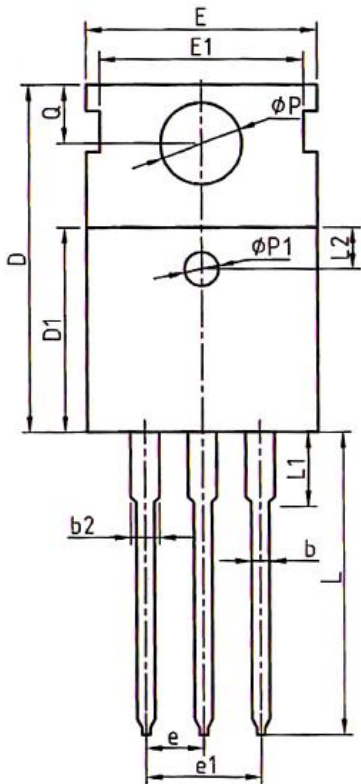
Test circuit and waveform for diode characteristics





COMMON DIMENSIONS

SYMBOL	MM		
	MIN	NOM	MAX
E	10.00	10.16	10.32
E1	9.94	10.04	10.14
E2	9.36	9.46	9.56
A	4.50	4.70	4.90
A1	2.34	2.54	2.74
A4	2.66	2.76	2.86
A5		1.00REF	
c	0.45	0.50	0.60
D	15.67	15.87	16.07
Q		9.40REF	
H1		6.70REF	
e		2.54BSC	
$\Phi$ P		3.18REF	
L	12.78	12.98	13.18
L1	2.83	2.93	3.03
L2	7.70	7.80	7.90
$\Phi$ P1	1.40	1.50	1.60
$\Phi$ P2	0.95	1.00	1.05
$\Phi$ P3		3.45REF	
$\theta$ 1	3°	5°	7°
$\theta$ 2	-	45°	-
F1	1.00	1.50	2.00
F2	13.80	13.90	14.00
F3	3.20	3.30	3.40
F4	5.30	5.40	5.50
G	7.80	8.00	8.20
G1	6.90	7.00	7.10
G3	1.25	1.35	1.45
b1	1.23	1.28	1.38
b2	0.75	0.80	0.90
K1	0.65	0.70	0.75
R		0.50REF	



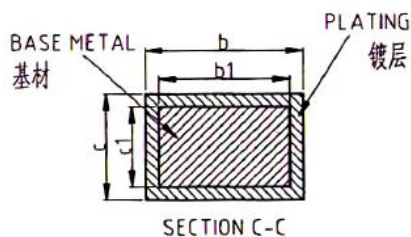
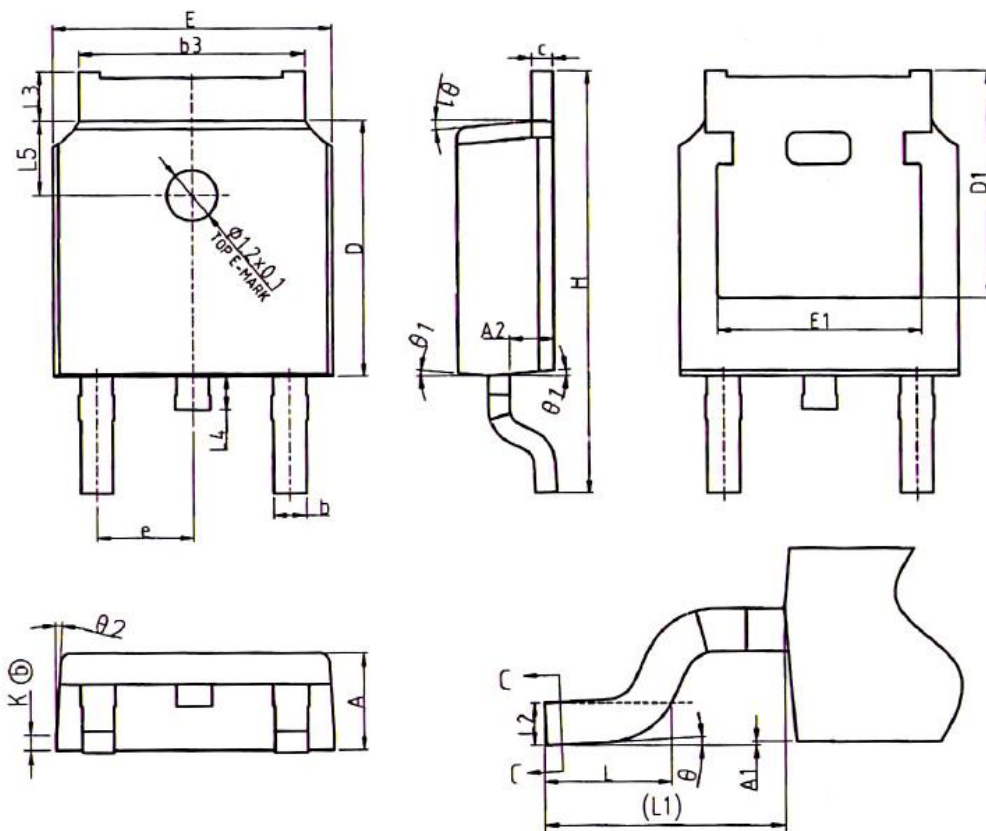
COMMON DIMENSIONS

SYMBOL	MM		
	MIN	NDM	MAX
A	4.40	4.57	4.70
A1	1.27	1.30	1.37
A2	2.35	2.40	2.50
b	0.77	0.80	0.90
b2	1.17	1.27	1.36
c	0.48	0.50	0.56
D	15.40	15.60	15.80
D1	9.00	9.10	9.20
DEP	0.05	0.10	0.20
E	9.80	10.00	10.20
E1	-	8.70	-
E2	9.80	10.00	10.20
phi P1	1.40	1.50	1.60
e	2.54BSC		
e1	5.08BSC		
H1	6.40	6.50	6.60
L	12.75	13.50	13.65
L1	-	3.10	3.30
L2	2.50REF		
phi P	3.50	3.60	3.63
Q	2.73	2.80	2.87
theta 1	5°	7°	9°
theta 2	1°	3°	5°
theta 3	1°	3°	5°



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# Package Outline TO-252



COMMON DIMENSIONS

SYMBOL	MM		
	MIN	NOM	MAX
A	2.20	2.30	2.38
A1	0.00	-	0.10
A2	0.97	1.07	1.17
b	0.72	0.78	0.85
b1	0.71	0.76	0.81
b3	5.23	5.33	5.46
c	0.47	0.53	0.58
c1	0.46	0.51	0.56
D	6.00	6.10	6.20
D1	5.30REF		
E	6.50	6.60	6.70
E1	4.70	4.83	4.92
e	2.286BSC		
H	9.90	10.10	10.30
L	1.40	1.50	1.70
L1	2.90REF		
L2	0.51BSC		
L3	0.90	-	1.25
L4	0.60	0.80	1.00
L5	1.70	1.80	1.90
$\theta$	0°	-	8°
$\theta 1$	5°	7°	9°
$\theta 2$	5°	7°	9°
K	0.40REF		

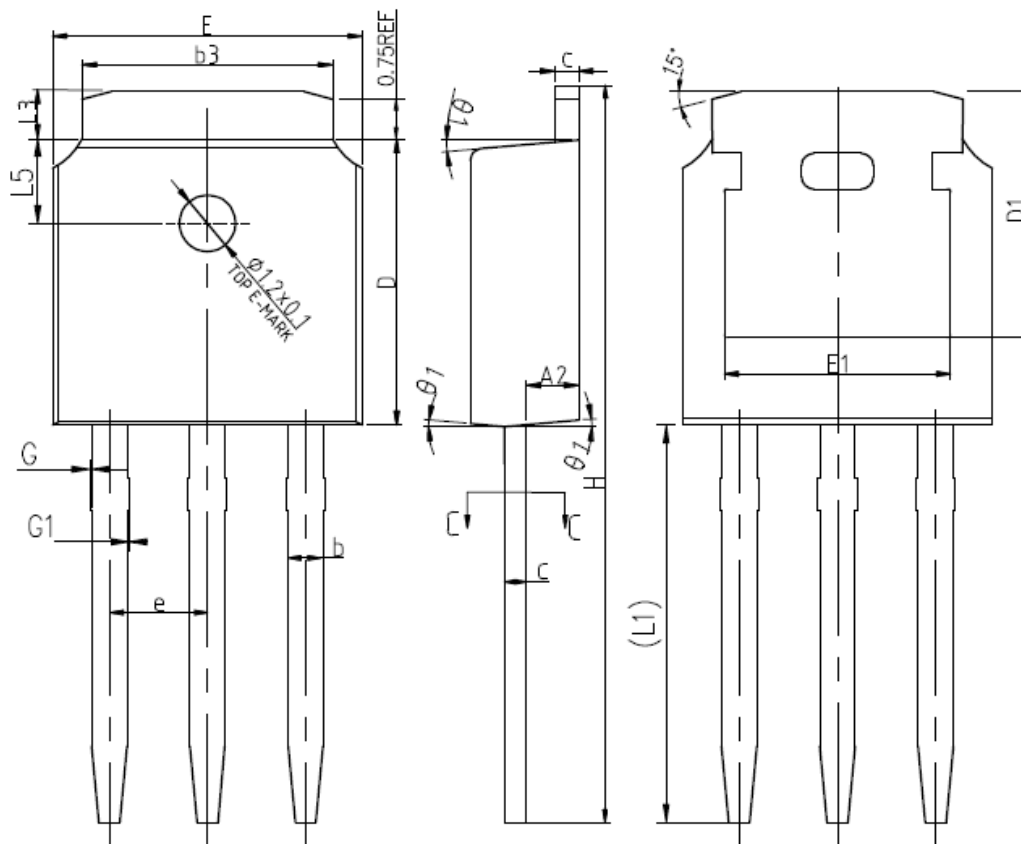
SSF80R850S/SSP80R850S/SST80R850S/SSU80R850S 800V N-Channel MOSFET



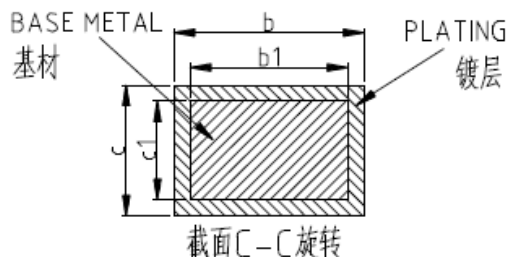
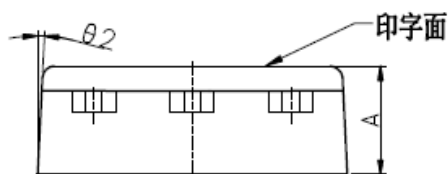
# Package Outline

TO-251

**SUPER**



COMMON DIMENSIONS



SYMBOL	MM		
	MIN	NOM	MAX
A	2.20	2.30	2.38
A2	0.97	1.07	1.17
b	0.72	0.78	0.85
b1	0.71	0.76	0.81
b3	5.23	5.33	5.46
c	0.47	0.53	0.58
c1	0.46	0.51	0.56
D	6.00	6.10	6.20
D1	5.30REF		
E	6.50	6.60	6.70
E1	4.70	4.83	4.92
e	2.286BSC		
H	16.10	16.40	16.60
L1	9.20	9.40	9.60
L3	0.90	1.02	1.25
L5	1.70	1.80	1.90
theta 1	5°	7°	9°
theta 2	5°	7°	9°

SSF80R850S/SSP80R850S/SST80R850S/SSU80R850S 800V N-Channel MOSFET



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[IPS70R2K0CEAKMA1](#) [RJK60S3DPP-E0#T2](#) [RJK60S5DPK-M0#T0](#) [APT5010JVFR](#) [APT12031JFLL](#) [APT12040JVR](#) [DMN3404LQ-7](#)  
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