

Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- ► Integral source-drain diode
- ► High input impedance and high gain
- Complementary N- and P-Channel devices

Applications

- Motor controls
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

General Description

The Supertex 2N7008 is an enhancement-mode (normally-off) transistor that utilizes a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors, and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Ordering Information

Device	Device Package Option		$R_{DS(ON)} \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ $	l _{D(ON)} (min) (mA)	
2N7008-G	TO-92	60	7.5	500	





Absolute Maximum Ratings

Parameter	Value			
Drain-to-source voltage	BV _{DSS}			
Drain-to-gate voltage	BV_{DGS}			
Gate-to-source voltage	±30V			
Operating and storage temperature	-55°C to +150°C			
Soldering temperature*	+300°C			

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Pin Configuration



Product Marking



YY = Year Sealed
WW = Week Sealed
_____ = "Green" Packaging

TO-92

⁻G indicates package is RoHS compliant ('Green')

Distance of 1.6mm from case for 10 seconds.

Thermal Characteristics

Package	I _D (continuous) [†] (mA)	I _D (pulsed) (A)	Power Dissipation @T _c = 25°C (W)	θ _{jc} (°C/W)	θ _{ja} (°C/W)	l _{DR} [†] (mA)	DRM (A)
TO-92	230	1.3	1.0	125	170	230	1.3

Note:

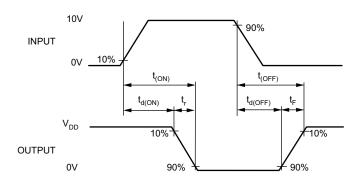
Electrical Characteristics (T_A = 25°C unless otherwise specified)

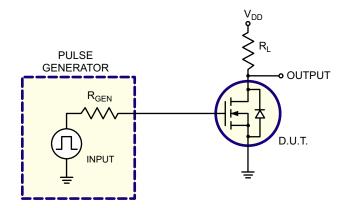
Sym	Parameter		Тур	Max	Units	Conditions	
BV _{DSS}	Drain-to-source breakdown voltage	60	-	-	V	$V_{GS} = 0V, I_{D} = -10\mu A$	
$V_{GS(th)}$	Gate threshold voltage	1.0	-	2.5	V	$V_{GS} = V_{DS}$, $I_{D} = 250 \mu A$	
I _{GSS}	Gate body leakage current	-	-	100	nA	$V_{GS} = \pm 30V, V_{DS} = 0V$	
		-	-	1.0		$V_{GS} = 0V, V_{DS} = 50V$	
I _{DSS}	Zero gate voltage drain current	-	-	500	μA	$V_{GS} = 0V, V_{DS} = 50V,$ $T_{A} = 125^{\circ}C$	
I _{D(ON)}	On-state drain current	500	-	-	mA	$V_{GS} = 10V, V_{DS} \ge 2.0V_{DS(ON)}$	
В	Static drain-to-source	-	-	7.5	Ω	$V_{GS} = 5.0V, I_{D} = 50mA$	
R _{DS(ON)}	on-state resistance	-	-	7.5	1 12	V _{GS} = 10V, I _D = 500mA	
G _{FS}	Forward transconductance	80	-	-	mmho	V _{DS} = 10V, I _D = 200mA	
C _{iss}	Input capacitance	-	-	50			
C _{oss}	Common source output capacitance	-	-	25	pF	$V_{GS} = 0V, V_{DS} = 25V,$ f = 1.0MHz	
C _{RSS}	Reverse transfer capacitance	-	-	5.0			
t _(ON)	Turn-on time	-	-	20	no	V _{DD} = 30V, I _D = 200mA,	
t _(OFF)	Turn-off time	-	-	20	ns	$R_{GEN}^{BB} = 25\Omega$	
V _{SD}	Diode forward voltage drop	-	-	1.5	V	V _{GS} = 0V, I _{SD} = 150mA	

Notes:

- All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
 All A.C. parameters sample tested.

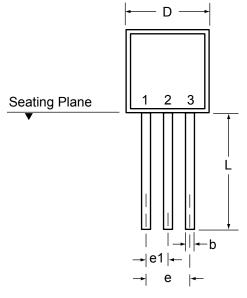
Switching Waveforms and Test Circuit

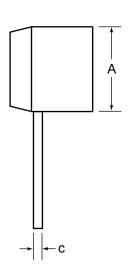




[†] I_D (continuous) is limited by max rated T_L

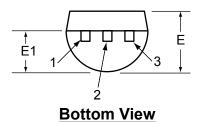
3-Lead TO-92 Package Outline (N3)





Front View

Side View



Symbol		Α	b	С	D	E	E1	е	e1	L
Dimensions (inches)	MIN	.170	.014 [†]	.014 [†]	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022 [†]	.022 [†]	.205	.165	.105	.105	.055	.610*

JEDEC Registration TO-92.

Drawings not to scale.

Supertex Doc.#: DSPD-3TO92N3, Version D080408.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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^{*} This dimension is not specified in the original JEDEC drawing. The value listed is for reference only.

[†] This dimension is a non-JEDEC dimension.

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