# N-Channel Depletion-Mode Vertical DMOS FETs

## Features

▶ High input impedance
▶ Low input capacitance
▶ Fast switching speeds
▶ Low on-resistance
▶ Free from secondary breakdown
▶ Low input and output leakage

## Applications

▶ Normally-on switches
▶ Solid state relays
▶ Converters
▶ Constant current sources
▶ Power supply circuits
▶ Telecom

## General Description

The Supertex DN3145 is a depletion-mode (normally-on) transistor utilizing an advanced vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

## Ordering Information

| Device | Package Option TO-243AA (SOT-89) | $BV_{DSX}/BV_{DGX}$ (V) | $R_{DS(ON)}$ (max) ($\Omega$) | $I_{DSS}$ (min) (mA) |
|---|---|---|---|---|
| DN3145 | DN3145N8-G | 450 | 60 | 120 |

*-G indicates package is RoHS compliant ('Green')*

## Absolute Maximum Ratings

| Parameter | Value |
|---|---|
| Drain-to-source voltage | $BV_{DSX}$ |
| Drain-to-gate voltage | $BV_{DGX}$ |
| Gate-to-source voltage | ±20V |
| Operating and storage temperature | -55°C to +150°C |
| Soldering temperature* | 300°C |

*Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.*

\*  *Distance of 1.6mm from case for 10 seconds.*

## Pin Configuration



**TO-243AA (SOT-89) (N8)**

DRAIN

SOURCE
DRAIN
GATE
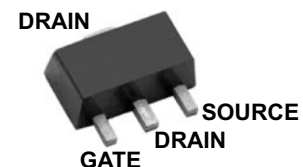
## Product Marking

**DN1MW**

W = Code for week sealed
_____ = "Green" Packaging

**TO-243AA (SOT-89) (N8)**

## Thermal Characteristics

| Package | $I_D$ (continuous)† (mA) | $I_D$ (pulsed) (mA) | Power Dissipation @$T_A$ = 25°C (W) | $\theta_{jc}$ (°C/W) | $\theta_{ja}$ (°C/W) | $I_{DR}$† (mA) | $I_{DRM}$ (mA) |
|---|---|---|---|---|---|---|---|
| TO-243AA | 100 | 300 | 1.3‡ | 34 | 97‡ | 100 | 300 |

*Notes:*

† $I_D$ (continuous) is limited by max rated $T_J$.
‡ Mounted on FR4 board, 25mm x 25mm x 1.57mm.

## Electrical Characteristics *($T_A$ = 25°C unless otherwise specified)*

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $BV_{DSX}$ | Drain-to-source breakdown voltage | 450 | - | - | V | $V_{GS}$ = -5.0V, $I_D$ = 100µA |
| $V_{GS(OFF)}$ | Gate-to-source off voltage | -1.5 | - | -3.5 | V | $V_{DS}$ = 15V, $I_D$ = 10µA |
| $\Delta V_{GS(OFF)}$ | Change in $V_{GS(OFF)}$ with temperature | - | - | -4.5 | mV/°C | $V_{DS}$ = 15V, $I_D$ = 10µA |
| $I_{GSS}$ | Gate body leakage current | - | - | 100 | nA | $V_{GS}$ = ±20V, $V_{DS}$ = 0V |
| $I_{D(OFF)}$ | Drain-to-source leakage current | - | - | 1.0 | µA | $V_{DS}$ = Max rating, $V_{GS}$ = -5.0V |
| | | - | - | 1.0 | mA | $V_{DS}$ = 0.8 Max Rating, $V_{GS}$ = -5.0V, $T_A$ = 125°C |
| $I_{DSS}$ | Saturated drain-to-source current | 120 | - | - | mA | $V_{GS}$ = 0V, $V_{DS}$ = 15V |
| $R_{DS(ON)}$ | Static drain-to-source on-state resistance | - | - | 60 | Ω | $V_{GS}$ = 0V, $I_D$ = 100mA |
| $\Delta R_{DS(ON)}$ | Change in $R_{DS(ON)}$ with temperature | - | - | 1.1 | %/°C | $V_{GS}$ = 0V, $I_D$ = 100mA |
| $G_{FS}$ | Forward transconductance | 140 | - | - | mmho | $V_{DS}$ = 10V, $I_D$ = 100mA |
| $C_{ISS}$ | Input capacitance | - | - | 120 | pF | $V_{GS}$ = -5.0V, $V_{DS}$ = 25V, f = 1.0MHz |
| $C_{OSS}$ | Common source output capacitance | - | - | 15 | | |
| $C_{RSS}$ | Reverse transfer capacitance | - | - | 10 | | |
| $t_{d(ON)}$ | Turn-on delay time | - | - | 10 | ns | $V_{DD}$ = 25V, $I_D$ = 100mA, $R_{GEN}$ = 25Ω, |
| $t_r$ | Rise time | - | - | 15 | | |
| $t_{d(OFF)}$ | Turn-off delay time | - | - | 20 | | |
| $t_f$ | Fall time | - | - | 35 | | |
| $V_{SD}$ | Diode forward voltage drop | - | - | 1.8 | V | $V_{GS}$ = -5.0V, $I_{SD}$ = 100mA |
| $t_{rr}$ | Reverse recovery time | - | 800 | - | ns | $V_{GS}$ = -5.0V, $I_{SD}$ = 100mA |

*Notes:*

1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

## Switching Waveforms and Test Circuit
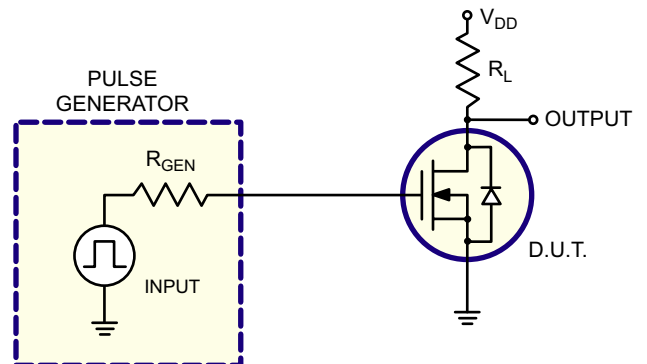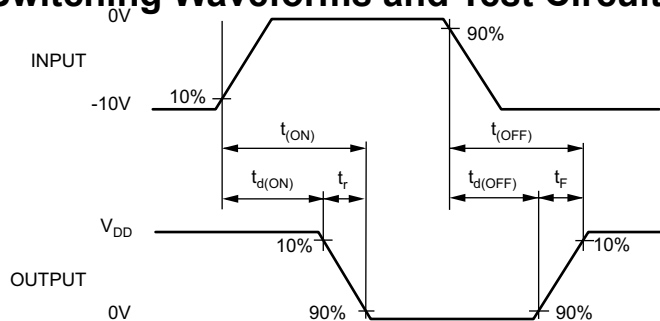
## 3-Lead TO-243AA (SOT-89) Package Outline (N8)
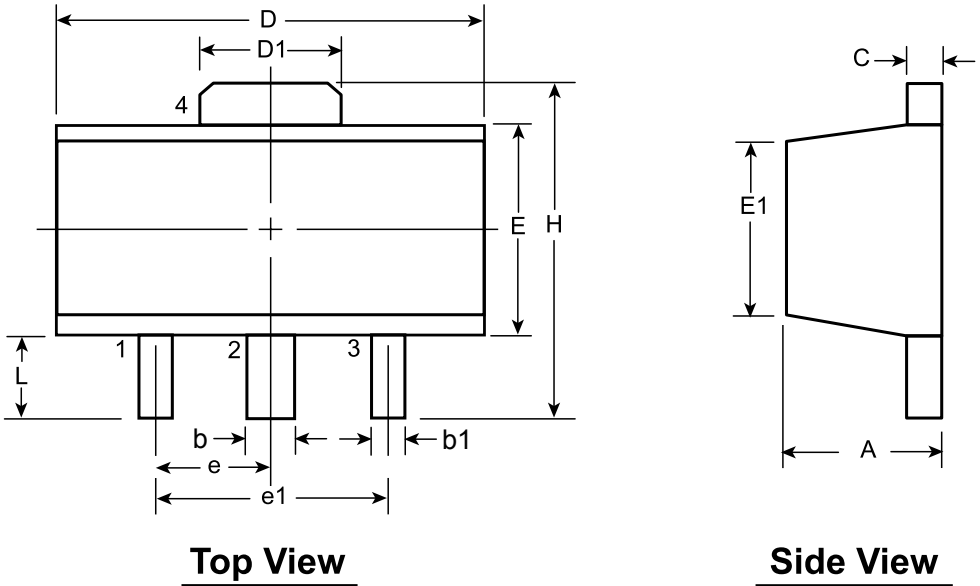


**Top View**

**Side View**

| Symbol | | A | b | b1 | C | D | D1 | E | E1 | e | e1 | H | L |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Dimensions (mm) | MIN | 1.40 | 0.44 | 0.36 | 0.35 | 4.40 | 1.62 | 2.29 | 2.13 | 1.50 BSC | 3.00 BSC | 3.94 | 0.89 |
| | NOM | - | - | - | - | - | - | - | - | | | - | - |
| | MAX | 1.60 | 0.56 | 0.48 | 0.44 | 4.60 | 1.83 | 2.60 | 2.29 | | | 4.25 | 1.20 |

*JEDEC Registration TO-243, Variation AA, Issue C, July 1986.*
***Drawings not to scale**.*
***Supertex Doc. #:** DSPD-3TO243AAN8, Version D070908.*

*(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)*

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