HV7022

34-Channel Symmetric Row Driver

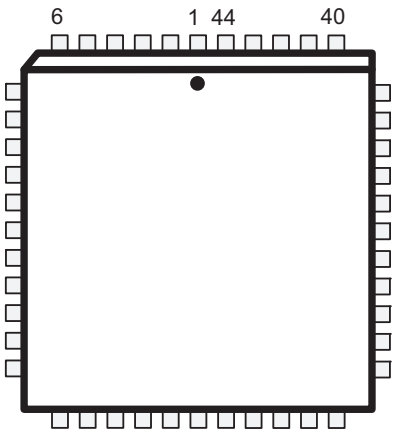
Features

- High-Voltage CMOS technology
- Symmetric row drive (reduces latent imaging in ACTFEL displays)
- Output voltage up to +230V
- Low power level shifting
- Source/sink current minimum 70 mA
- Shift register speed 4.0 MHz
- Pin-programmable shift direction

Description

HV7022 is a low-voltage serial to high-voltage parallel converter with push-pull outputs. It is especially suited for use as a symmetric row driver in AC thin-film electroluminescent (ACTFEL) displays. HV7022 offers 34 output lines, a direction (DIR) pin to give CW or CCW shift register loading, output enable (OE), and polarity (POL) control. After data is entered on the falling edge of CLK, a logic high will cause the output to swing to V_{PP} if POL is high, or to GND if POL is low.

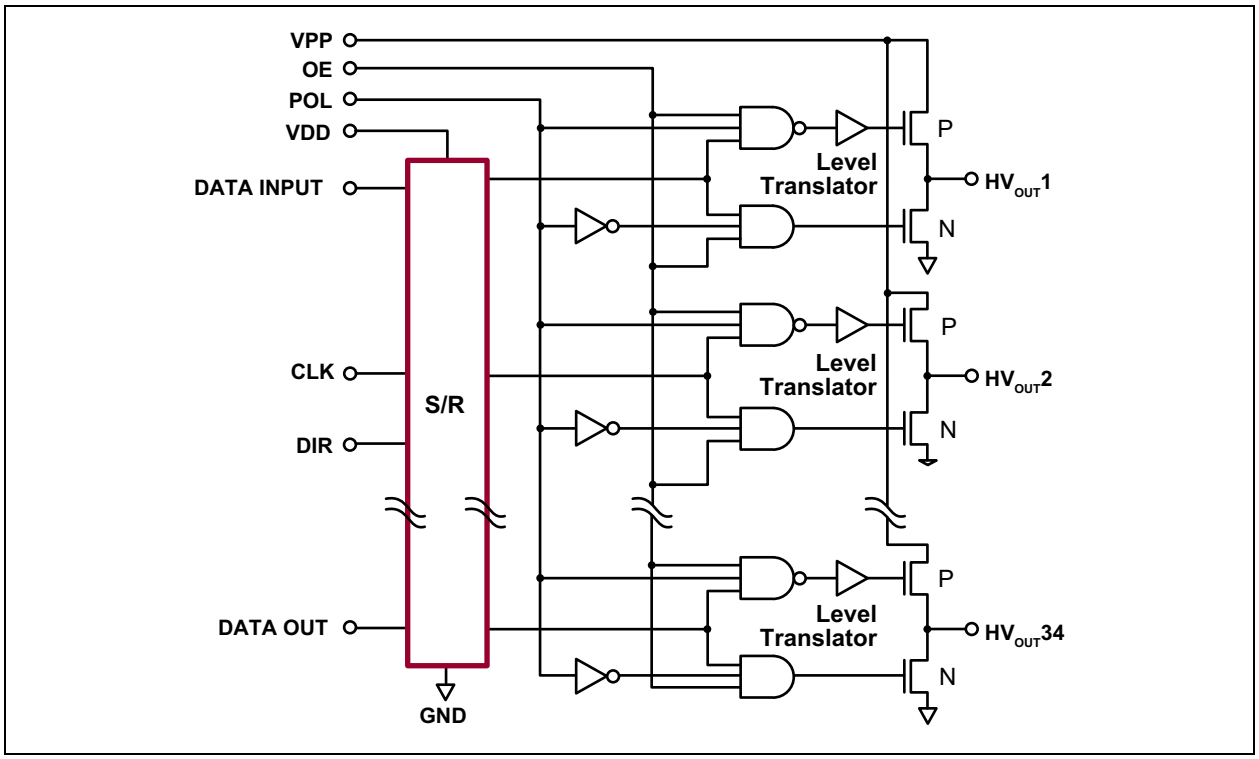
Package Type



44-Lead PLCC

See Table 2-1 for pin information

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS†

Supply voltage, V_{DD} ..... -0.3V to +15V
Supply voltage, V_{PP} ..... -0.3V to +250V
Logic input levels ..... -0.3V to V_{DD}+0.3V
Ground current[1] 1.5A
Continuous total power dissipation[2] 1200mW
Operating temperature range ..... -40°C to +85°C
Storage temperature range ..... -65°C to +150°C

† Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

1: Duty cycle is limited by the total power dissipated in the package.

2: For operation above 25°C ambient derate linearly to maximum operating temperature at 25 mW/°C.

ELECTRICAL CHARACTERISTICS

Recommended Operating Conditions: V_{PP} = 230V, V_{DD} = 12V, T_A = 25°C, unless otherwise noted

Symbol	Parameter		Min	Max	Units	Conditions
DC Characteristics						
I_{DD}	V_{DD} supply current		-	10	mA	f_{CLK}= 4.0MHz, V_{DD}=13.2V
I_{PP}	V_{PP} supply current		-	4.0	mA	One output high (**Note 1**)
			-	100	µA	All outputs low or High-Z
			-	750		All outputs low or High-Z (125°C)
I_{DDQ}	Quiescent V_{DD} supply current		-	100	µA	All V_{IN}= GND or V_{DD}
V_{OH}	High-level output	HV_{OUT}	195	-	V	I_O= -70mA
		DATA OUT	11	-	V	I_O= -500µA
V_{OL}	Low-level output	HV_{OUT}	-	30	V	I_O= +70mA
		DATA OUT	-	1.0	V	I_O= +500µA
I_{IH}	High-level logic input current		-	1.0	µA	V_{IH}= 12V
I_{IL}	Low-level logic input current		-	-1.0	µA	V_{IL}= 0V
AC Characteristics						
f_{CLK}	Clock frequency		-	4.0	MHz	–
t_{WH},t_{WL}	Pulse duration clock width high or low		125	-	ns	–
t_{SUD}	Data set-up time before falling clock		100	-	ns	–
t_{HD}	Data hold time after falling clock		100	-	ns	–
t_{SUC}	Setup time clock low before V_{PP}↑ or GND↓		300	-	ns	–
t_{SUE}	Setup time enable high before V_{PP}↑ or GND↓		300	-	ns	–
t_{SUP}	Setup time polarity high or low before V_{PP}↑ or GND↓		300	-	ns	–
t_{HC}	Hold time clock high after V_{PP}↑ or GND↓		500	-	ns	–
t_{HE}	Hold time enable high after V_{PP}↑ or GND↓		300	-	ns	–
t_{HP}	Hold time polarity high or low after V_{PP}↑ or GND↓		300	-	ns	–

ELECTRICAL CHARACTERISTICS (CONTINUED)

Recommended Operating Conditions: V_{PP} = 230V, V_{DD} = 12V, T_A = 25°C, unless otherwise noted					
Symbol	**Parameter**	**Min**	**Max**	**Units**	**Conditions**
t_{DHL}	Delay time high to low-level output from clock	-	150	ns	C_L= 10pF
t_{DLH}	Delay time low to high-level output from clock	-	200	ns	C_L = 10pF
t_{THL}	Transition time high to low-level serial output	-	200	ns	C_L= 15pF
t_{TLH}	Transition time low to high-level serial output	-	100	ns	C_L= 15pF
t_{ONH}	High-level turn-on time HV_{OUT} from enable	-	500	ns	V_{OH}= 195V, R_L= 2.0kΩ to 95V
t_{ONL}	Low-level turn-on time HV_{OUT} from enable	-	500	ns	V_{OH}= 130V, R_L= 2.0kΩ to 30V
t_{OFFH}	High-level turn-off time HV_{OUT} from enable	-	1000	ns	V_{OH}= 195V, R_L= 2.0kΩ to 95V
t_{OFFL}	Low-level turn-off time HV_{OUT} from enable	-	500	ns	V_{OH}= 130V, R_L= 2.0kΩ to 30V
SR	Slew rate, V_{PP} or GND	-	45	V/µs	One active output driving 4.7nF load to V_{PP} or GND

Note 1: The total number of ON outputs times the duty cycle must not exceed the allowable package power dissipation.

TEMPERATURE SPECIFICATIONS

Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Operating Temperature	–	-40	–	85	°C	–
Storage Temperature	–	-65	–	150	°C	–
Package Thermal Resistances						
Thermal Resistance, 44-Lead PLCC	θ_{ja}	–	37	–	°C/W	–

1.1 Power up and Recommended Operating Conditions

To power-up HV7022, perform the following power-up sequence:

1. Connect ground
2. Apply V_{DD}
3. Set all inputs (Data, CLK, Enable, etc) to a known state.
4. Apply V_{PP} (V_{PP} should not drop below V_{DD} or float during operation).

To power-down the device, reverse the steps above.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Units
V_{DD}	Logic supply voltage		10.8	13.2	V
V_{PP}	High voltage supply		–	230	V
V_{IH}	High-level input voltage	V_{DD} = 10.8	8.1	–	V
		V_{DD} = 13.2	9.9	–	
V_{IL}	Low-level input voltage	V_{DD} = 10.8	-	2.7	V
		V_{DD} = 13.2	-	3.3	
f_{CLK}	Clock frequency		-	4.0	MHz
T_A	Operating free-air temperature		-40	+85	°C
I_{OD}	Allowable pulsed current through output diode.		–	±300	mA

2.0 PIN DESCRIPTION

The locations of the pins are listed in Package Type.

TABLE 2-1: PIN DESCRIPTION

Pin #	HV7022	Description
1	HV_{OUT}18/17	High voltage outputs.
2	HV_{OUT}17/18	
3	HV_{OUT}16/19	
4	HV_{OUT}15/20	
5	HV_{OUT}14/21	
6	HV_{OUT}13/22	
7	HV_{OUT}12/23	
8	HV_{OUT}11/24	
9	HV_{OUT}10/25	
10	HV_{OUT}9/26	
11	HV_{OUT}8/27	
12	HV_{OUT}7/28	
13	HV_{OUT}6/29	
14	HV_{OUT}5/30	
15	HV_{OUT}4/31	
16	HV_{OUT}3/32	
17	HV_{OUT}2/33	
18	HV_{OUT}1/34	
19	Data OUT	Serial data output. Data output for cascading to the data input of the next device.
20	OE	Output enable input. When OE is Low, all HV outputs are forced into a High-Z state, regardless of data in each channel. When OE is High, all HV outputs reflect data latched.
21	CLK	Data shift register clock Input are shifted into the shift register on the negative edge of the clock.
22	GND	Logic and high voltage ground.
23	DIR	Direction.
24	VDD	Low voltage logic power rail.
25	POL	Polarity.
26	DATA INPUT	Serial data input. Data needs to be present before each falling edge of the clock.
27	VPP	High voltage power rail.
28	NC	No Connect.
29	HV_{OUT}34/1	High voltage outputs
30	HV_{OUT}33/2	
31	HV_{OUT}32/3	
32	HV_{OUT}31/4	
33	HV_{OUT}30/5	
34	HV_{OUT}29/6	

TABLE 2-1: PIN DESCRIPTION

Pin #	HV7022	Description
35	$HV_{OUT}28/7$	High voltage outputs.
36	$HV_{OUT}27/8$	
37	$HV_{OUT}26/9$	
38	$HV_{OUT}25/10$	
39	$HV_{OUT}24/11$	
40	$HV_{OUT}23/12$	
41	$HV_{OUT}22/13$	
42	$HV_{OUT}21/14$	
43	$HV_{OUT}20/15$	
44	$HV_{OUT}19/16$	

Note 1: Pin designation for DIR H/L
Example: for DIR = H, pin 1 is $HV_{OUT}18$
for DIR = L, pin 1 is $HV_{OUT}17$

3.0 FUNCTIONAL DESCRIPTION

Table 3-1 provides functional information about HV7022.

TABLE 3-1: FUNCTIONAL TABLE CLK

I/O Relations	Inputs					Outputs		
	CLK	DIR	DATA	POL	OE	Shift Reg	HV_{OUT}	DATA OUT
O/P HIGH	X	X	H	H	H	*	H	*
O/P OFF	X	X	L	H	H	*	HIGH-Z	*
O/P LOW	X	X	H	L	H	*	L	*
O/P OFF	X	X	L	L	H	*	HIGH-Z	*
O/P OFF	X	X	X	X	L	*	All O/P HIGH-Z	*
Load S/R, set DIR	↓	L	X	X	X	Qn→Qn+1	*	Q_{34}
	↓	H	X	X	X	Qn→Qn-1	*	Q_1
	No ↓	X	X	X	X	*	No Change	No Change

Note 1: H = logic high level, L = logic low level, X = irrelevant, ↓ = high-to-low transition
Q1 = $HV_{OUT}1$, Qn = $HV_{OUT}n$, etc.
* = dependent on previous state and whether an O/P or S/R command occurred.

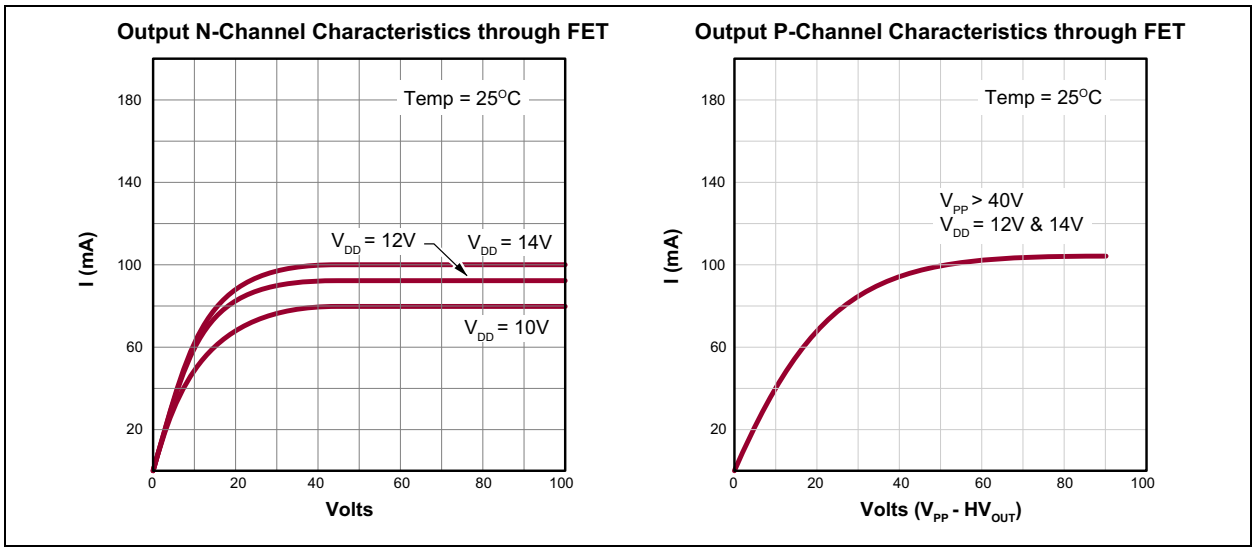


FIGURE 3-1: *HV_{OUT} Characteristics*

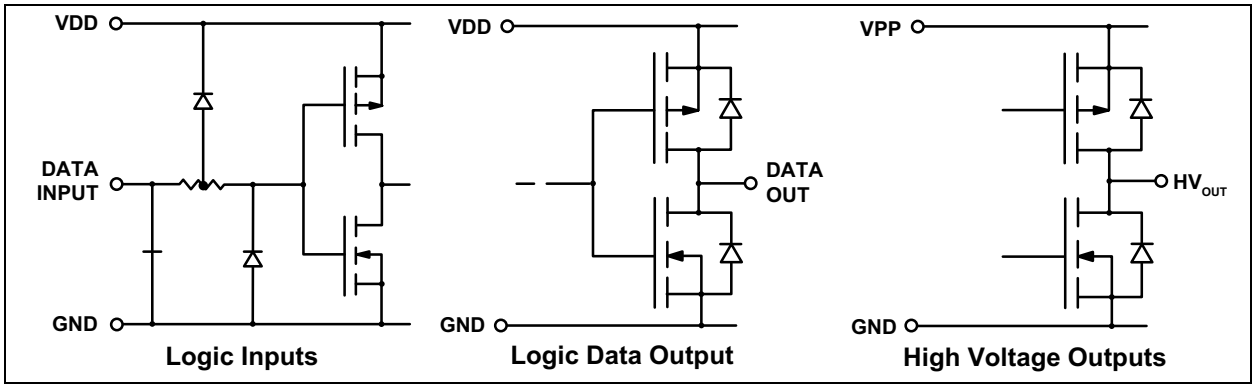


FIGURE 3-2: *Input and Output Equivalent Circuits*

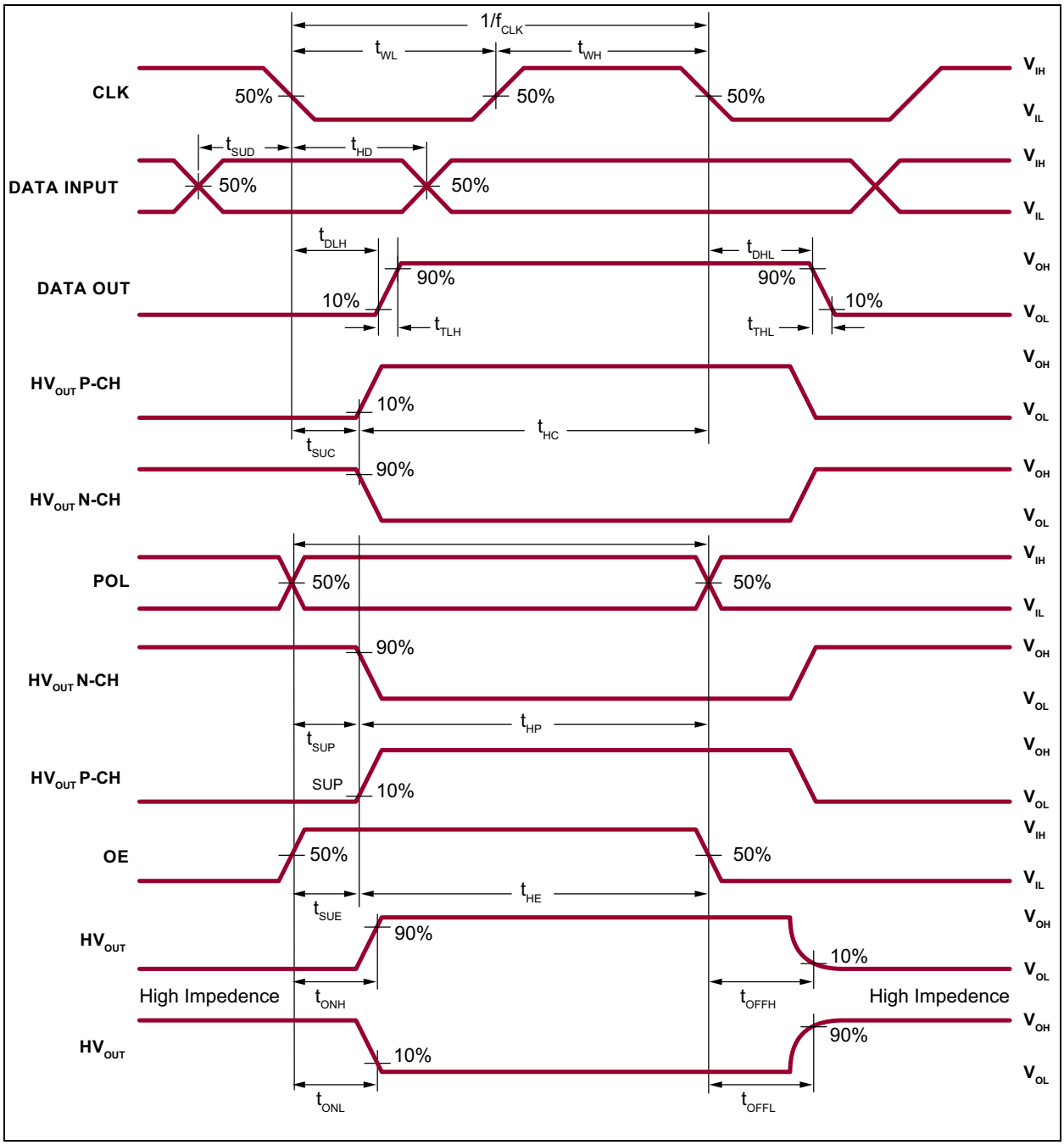
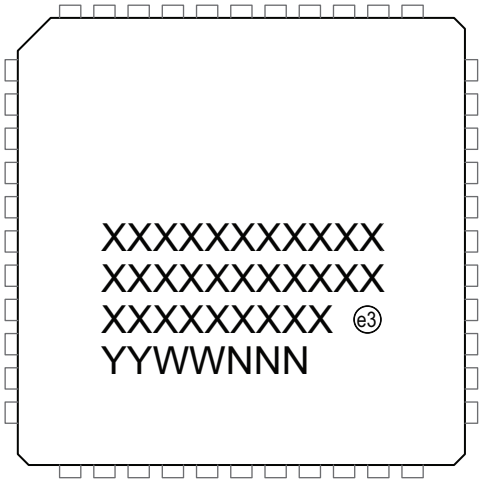


FIGURE 3-3: *Switching Waveforms*

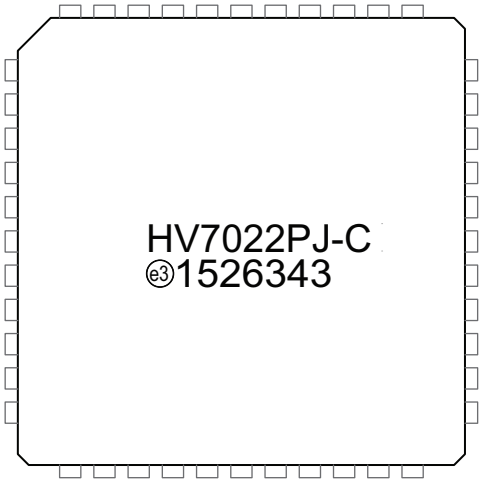
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

44-lead PLCC



Example

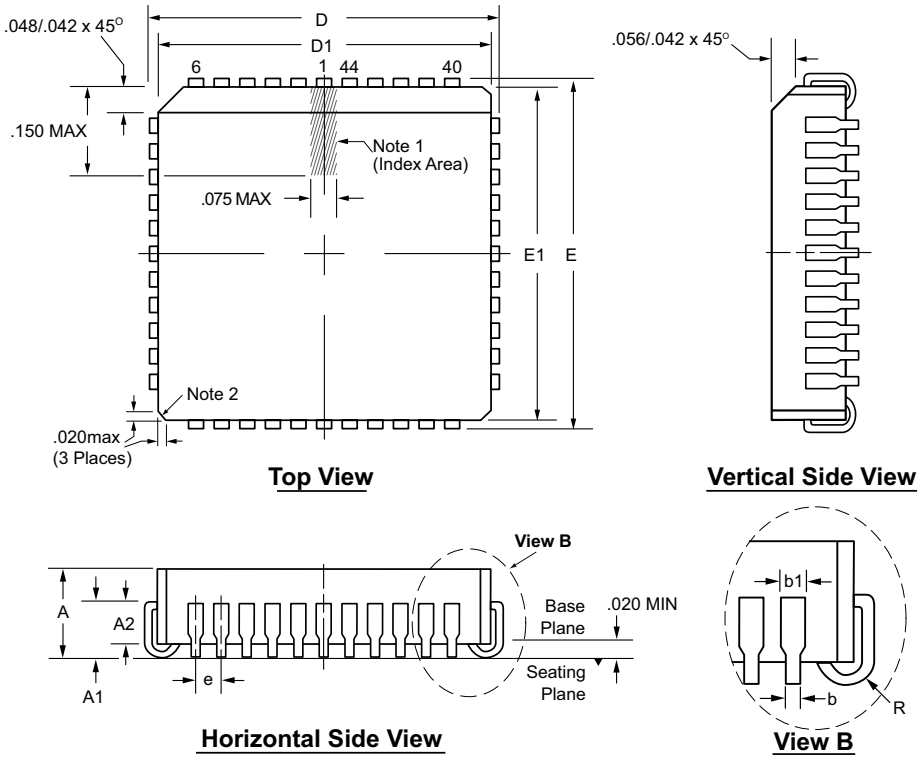


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

44-Lead PLCC Package Outline (PJ)

.653x.653in body, .180in height (max), .050in pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Actual shape of this feature may vary.*

Symbol		A	A1	A2	b	b1	D	D1	E	E1	e	R
Dimension (inches)	MIN	.165	.090	.062	.013	.026	.685	.650	.685	.650	.050 BSC	.025
	NOM	.172	.105	-	-	-	.690	.653	.690	.653		.035
	MAX	.180	.120	.083	.021	.036†	.695	.656	.695	.656		.045

JEDEC Registration MS-018, Variation AC, Issue A, June, 1993.
† This dimension differs from the JEDEC drawing.
Drawings not to scale.

APPENDIX A: REVISION HISTORY

Revision A (February 2016)

- Updated Supertex Doc.# DSFP-HV7022C to Microchip DS20005428A.
- Changed part number from HV7022C to HV7022.
- Removed 44-Lead Quad Cerpac package.
- Minor text changes throughout.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	XX	-	X	-	X	-	X
Device	Package Options		Version		Environmental		Media Type

Device:	HV7022	= 34-Channel Symmetric Row Driver
Package:	PJ	= 44-Lead PLCC
Version	C	= Revision C
Environmental	G	= Lead (Pb)-free/ROHS-compliant package
Media Type:	(blank)	= 27/Tube for PJ package

Examples:

a) HV7022PJ-C-G — 44-Lead PLCC package, 27/Tube

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