HV9925

Programmable Current LED Lamp Driver IC with PWM Dimming

Features

- Programmable Output Current up to 50 mA
- Pulse-Width Modulation (PWM) Dimming/Enable
- Universal 85 VAC to 264 VAC Operation
- Fixed Off-Time Buck Converter
- Internal 475V Power MOSFET
- Overtemperature Protection with Hysteresis

Applications

- Decorative Lighting
- Low-Power Lighting Fixtures

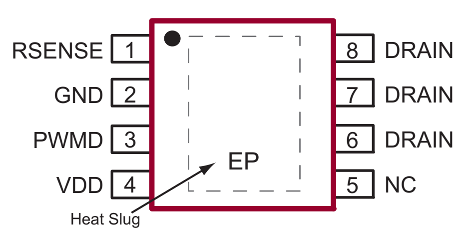
General Description

The HV9925 is a pulse-width modulated high-efficiency LED driver control IC with PWM dimming capabilities. It allows efficient operation of high-brightness LED strings from voltage sources ranging up to 400 VDC. The HV9925 includes an internal high-voltage switching MOSFET controlled with a fixed off-time of approximately 10.5 µs. The LED string is driven at constant current, thus providing constant light output and enhanced reliability. Selecting a current sense resistor value can externally program the output LED current of the HV9925.

The peak current control scheme provides good regulation of the output current throughout the universal AC line voltage range of 85 VAC to 264 VAC or DC input voltage of 20V to 400V. The HV9925 is designed with a built-in thermal shutdown to prevent excessive power dissipation in the IC.

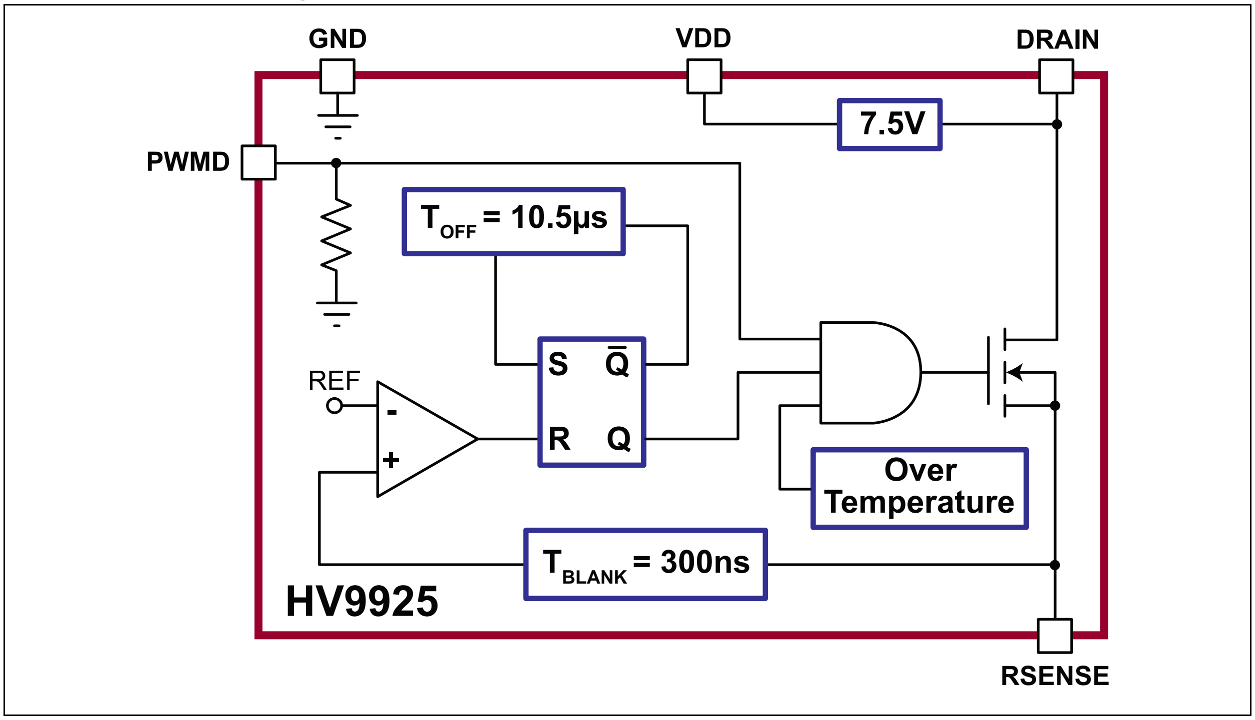
Package Type

8-lead SOIC
(Top view)

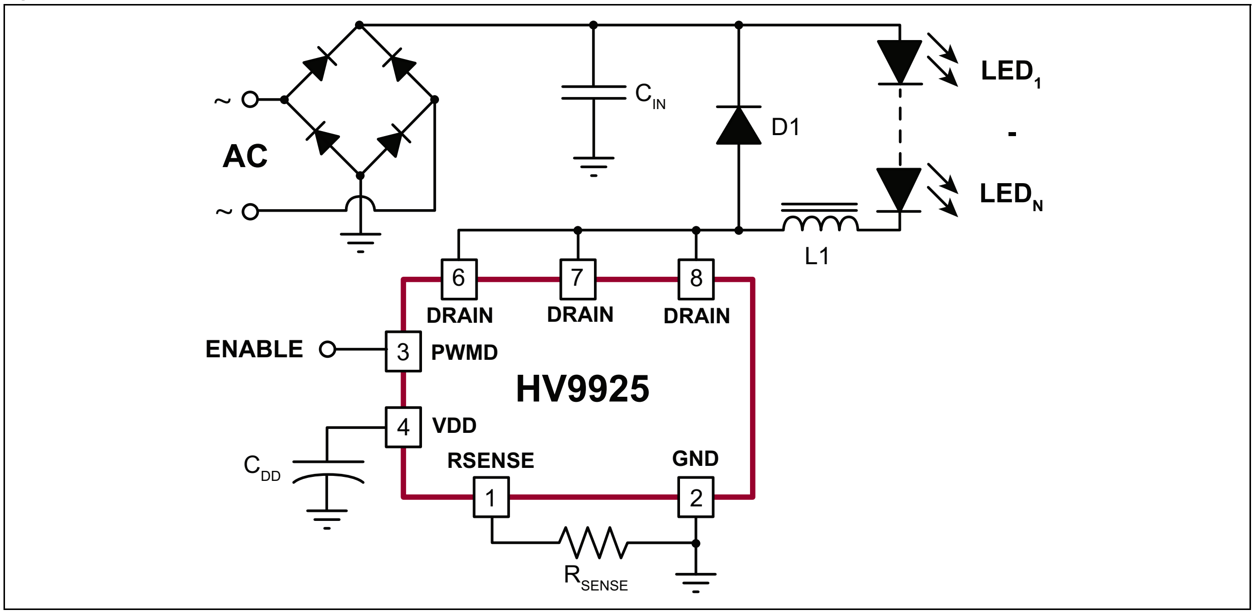


Heat slug (exposed thermal pad) is at ground potential. See Table 3-1 for pin information.

Functional Block Diagram



Typical Application Circuit



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

DRAIN-to-Source Breakdown Voltage, $V_{DS(BR)}$ .... +475V
Supply Voltage, V_{DD} .... –0.3V to +10V
PWMD, RSENSE Voltage .... –0.3V to +10V
Supply Current, I_{DD} .... +5 mA
Junction Temperature, T_J .... –40°C to +150°C
Storage Temperature, T_S .... –65°C to +150°C
Power Dissipation at 25°C (Note 1) .... 800 mW

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: The power dissipation is given for the standard minimum pad for 8-lead SOIC package without a heat slug, and based on $R_{\theta JA}$ = 125°C/W. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the latter is determined by the user’s board design. The junction-to-ambient thermal resistance is $R_{\theta JA}$ = 105°C/W when the part is mounted on a 0.04-square-inch pad of 1 oz copper, and $R_{\theta JA}$ = 60°C/W when mounted on a one-square-inch pad of 1 oz copper.

ELECTRICAL CHARACTERISTICS

Electrical Specifications: The specifications are at T_A = 25°C and V_{DRAIN} = 50V unless otherwise noted.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
V_{DD} Regulator Output	V_{DD}	—	7.5	—	V	
V_{DD} Undervoltage Upper Threshold	$V_{UVLO,R}$	4.8	—	—	V	V_{DD} Rising
V_{DD} Undervoltage Lockout Hysteresis	ΔV_{UVLO}	—	200	—	mV	
Operating Supply Current	I_{DD}	—	300	500	µA	$V_{DD(EXT)}$ = 8.5V
Output (DRAIN)						
V_{DRAIN} Supply Voltage	V_{DRAIN}	20	—	400	V	
On-Resistance	R_{ON}	—	100	200	Ω	I_{DRAIN} = 50 mA
Output Capacitance	C_{DRAIN}	—	1	5	pF	V_{DRAIN} = 400V (Note 2)
DRAIN Saturation Current	I_{SAT}	100	150	—	mA	
CURRENT SENSE COMPARATOR						
Threshold Voltage	V_{TH}	0.435	0.47	0.525	V	
Leading Edge Blanking Delay	T_{BLANK}	200	300	400	ns	Note 2
Minimum On-Time	$T_{ON(MIN)}$	—	—	650	ns	
OFF-TIME GENERATOR						
Off-Time	T_{OFF}	8	10.5	13	µs	
PWM DIMMING						
PWMD Input High Voltage	$V_{PWMD,HI}$	2	—	—	V	
PWMD Input Low Voltage	$V_{PWMD,LO}$	—	—	0.8	V	
PWMD Pull-Down Resistance	R_{PWMD}	100	200	300	kΩ	V_{PWMD} = 5V
THERMAL SHUTDOWN						
Overtemperature Trip Limit	T_{OT}	—	140	—	°C	Note 2
Temperature Hysteresis	T_{OTHYS}	—	60	—	°C	Note 2

Note 1: Denotes the specifications which apply over the full operating ambient temperature range of –40°C < T_A < +85°C.

2: Denotes guarantee by design.

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Ambient Temperature	T_A	–40	—	+85	°C	
Operating Junction Temperature	T_J	–40	—	+125	°C	
Storage Temperature	T_S	–65	—	+150	°C	
Maximum Junction Temperature	$T_{J(ABSMAX)}$	—	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
8-lead SOIC with Heat Slug	θ_{JA}	—	84	—	°C/W	**Note 1**
8-lead SOIC with Heat Slug	θ_{JA}	—	125	—	°C/W	**Note 2**
8-lead SOIC with Heat Slug	θ_{JA}	—	105	—	°C/W	**Note 3**
8-lead SOIC with Heat Slug	θ_{JA}	—	60	—	°C/W	**Note 4**

Note 1: Mounted on JEDEC 2s2p test PCB.

2: Mounted on standard minimum pad.

3: Mounted on a 0.04 square inch pad of 1 oz copper.

4: Mounted on a 1 square inch pad of 1 oz copper.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g. outside specified power supply range) and therefore outside the warranted range.

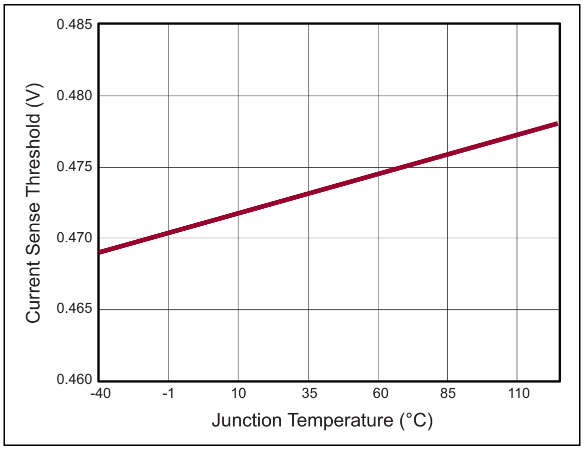


FIGURE 2-1: *Threshold Voltage V_{TH} vs. Junction Temperature T_J.*

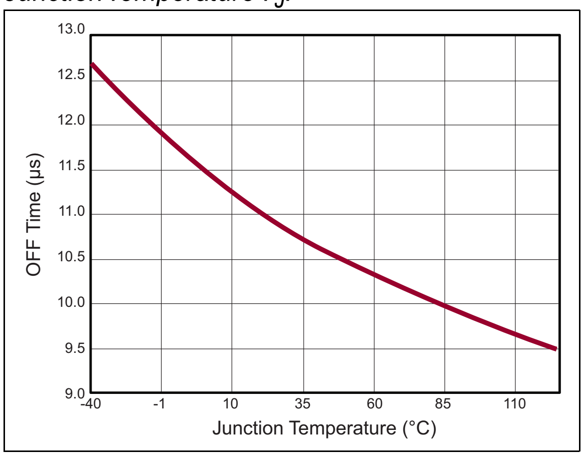


FIGURE 2-2: *Off-Time T_{OFF} vs. Junction Temperature T_J.*

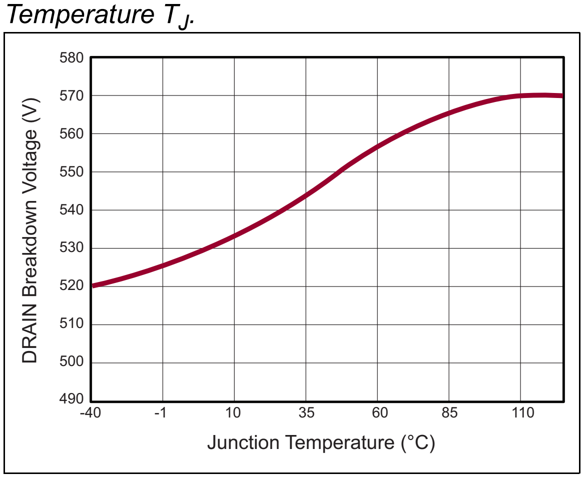


FIGURE 2-3: *DRAIN Breakdown Voltage V_{BR} vs. Junction Temperature T_J.*

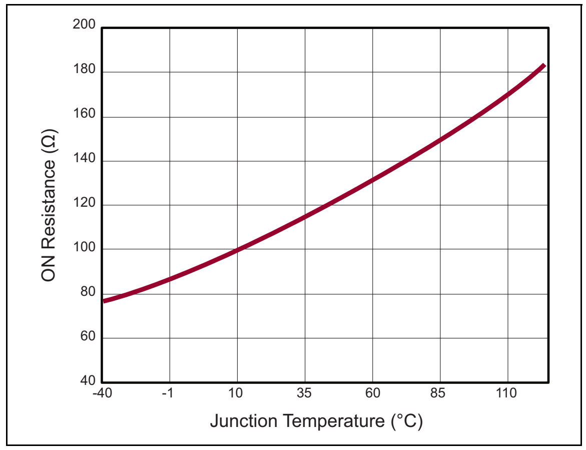


FIGURE 2-4: *ON Resistance R_{ON} vs. Junction Temperature T_J.*

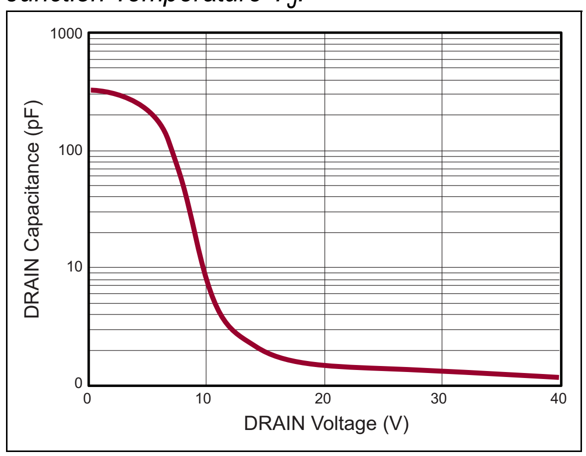


FIGURE 2-5: *DRAIN Capacitance C_{DRAIN} vs. V_{DRAIN}.*

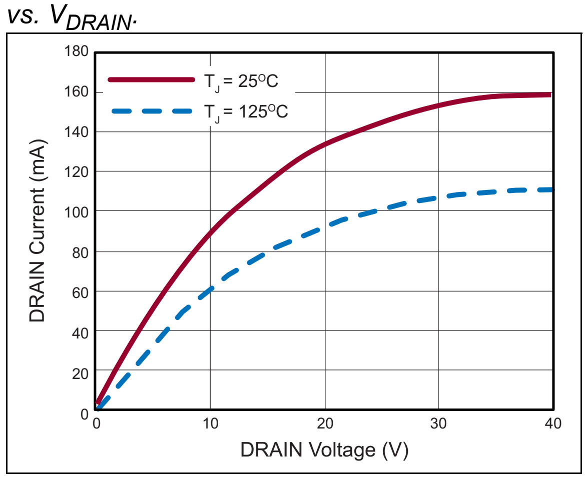


FIGURE 2-6: *Output Characteristics I_{DRAIN} vs V_{DRAIN}.*

3.0 PIN DESCRIPTION

The details on the pins of HV9925 are listed in Table 3-1. Refer to **Package Type** for the location of pins.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	RSENSE	Source terminal of the output switching MOSFET provided for current sense resistor connection
2	GND	Common connection for all circuits
3	PWMD	PWM Dimming input to the IC
4	VDD	Power supply pin for internal control circuits. Bypass this pin with a 0.1 µF low-impedance capacitor.
5	NC	No connection
6	DRAIN	Drain terminal of the output switching MOSFET and a linear regulator input
7		
8		
EP	GND	Exposed backside pad. It must be connected to pin 2 and GND plane on PCB to maximize thermal performance of the package.

4.0 FUNCTIONAL DESCRIPTION

The HV9925 is a PWM peak current control IC for driving a buck converter topology in Continuous Conduction Mode (CCM). The HV9925 controls the output current (rather than output voltage) of the converter that can be programmed by a single external resistor (R_{SENSE}) for driving a string of light-emitting diodes (LEDs). An external enable input (PWMD) that can be used for PWM dimming of an LED string is provided. The typical rising and falling edge transitions of the LED current when using the PWM dimming feature of the HV9925 are shown in Figure 5-6 and Figure 5-7.

When the input voltage of 20V to 400V appears at the DRAIN pin, the internal linear regulator attempts to maintain a voltage of 7.5 VDC at the V_{DD} pin. Until this voltage exceeds the internally programmed undervoltage upper threshold, no output switching occurs. When the threshold is exceeded, the integrated high-voltage switch turns on, pulling the DRAIN low. A 200 mV hysteresis is incorporated with the undervoltage comparator to prevent oscillation.

When the voltage at RSENSE exceeds 0.47V, the switch turns off and the DRAIN output becomes high impedance. At the same time, a one-shot circuit that determines the off-time of the switch (10.5 µs typical) is activated.

A “blanking” delay of 300 ns is provided upon the turn-on of the switch that prevents false triggering of the current sense comparator due to leading edge spike caused by circuit parasitics.

5.0 APPLICATION INFORMATION

5.1 Selecting L1 and D1

The required value of L1 is inversely proportional to the ripple current ΔI_O in it. Setting the relative peak-to-peak ripple current to 20%–30% of average output current in the LED string is a good practice to ensure noise immunity of the current sense comparator. See Equation 5-1.

EQUATION 5-1:

$$L1 = \frac{(V_O \times T_{OFF})}{\Delta I_O}$$

Where:

V_O = Forward voltage of the LED string
T_{OFF} = Off-time of the HV9925
ΔI_O = Peak-to-peak ripple current in the LED string

The output current in the LED string can be calculated as illustrated in Equation 5-2.

EQUATION 5-2:

$$I_O = \left(\frac{V_{TH}}{R_{SENSE}}\right) - \left(\frac{\Delta I_O}{2}\right)$$

Where:

V_{TH} = Current sense comparator threshold
R_{SENSE} = Current sense resistor

The ripple current introduces a peak-to-average error in the output current setting that needs to be accounted for. Due to the constant off-time control technique used in the HV9925, the ripple current is nearly independent of the input AC or DC voltage variation. Therefore, the output current will remain unaffected by the varying input voltage.

Adding a filter capacitor across the LED string can reduce the output current ripple even further, thus permitting a reduced value of L1. However, one must keep in mind that the peak-to-average current error is affected by the variation of T_{OFF}. Therefore, the initial output current accuracy might be sacrificed at large ripple current in L1.

Another important aspect of designing an LED driver with HV9925 is related to certain parasitic elements of the circuit, including distributed coil capacitance of L1, junction capacitance C_J and reverse recovery time t_{rr} of the rectifier diode D1, capacitance of the printed circuit board traces C_{PCB} and output capacitance C_{DRAIN} of the controller itself. These parasitic elements affect the efficiency of the switching converter and could potentially cause false triggering of the current sense comparator if not properly managed. Minimizing these parasitics is essential for efficient and reliable operation of HV9925.

Coil capacitance of inductors is typically provided in the manufacturer's data books either directly or in terms of the self-resonant frequency (SRF). Refer to Equation 5-3.

EQUATION 5-3:

$$SRF = \frac{1}{(2\Pi\sqrt{(L \times C_L)})}$$

Where:

L = Inductance value
C_L = Coil capacitance

Charging and discharging this capacitance every switching cycle causes high-current spikes in the LED string. Therefore, connecting a small capacitor C_O (~10 nF) is recommended to bypass these spikes.

Using an ultra-fast rectifier diode for D1 is recommended to achieve high efficiency and reduce the risk of false triggering of the current sense comparator. Using diodes with shorter reverse recovery time t_{rr} and lower junction capacitance C_J achieves better performance. The reverse voltage rating V_R of the diode must be greater than the maximum input voltage of the LED lamp.

The total parasitic capacitance present at the DRAIN output of the HV9925 can be calculated as shown in Equation 5-4.

EQUATION 5-4:

$$C_P = C_{DRAIN} + C_{PCB} + C_L + C_J$$

When the switch turns on, the capacitance C_P is discharged into the DRAIN output of the IC. The discharge current is typically limited to about 150 mA. However, it may become lower at increased junction temperature. The duration of the leading edge current spike can be estimated as show in Equation 5-5.

EQUATION 5-5:

$$T_{SPIKE} = \left(\frac{V_{IN} \times C_P}{I_{SAT}}\right) + t_{rr}$$

To avoid false triggering of the current sense comparator, C_P must be minimized in accordance with Equation 5-6.

EQUATION 5-6:

$$C_P < \frac{I_{SAT} \times (T_{BLANK(MIN)} - t_{rr})}{V_{IN(MAX)}}$$

Where:

$T_{BLANK(MIN)}$ = Minimum blanking time of 200 ns

$V_{IN(MAX)}$ = Maximum instantaneous input voltage

The typical DRAIN and RSENSE voltage waveforms are shown in Figure 5-4 and Figure 5-5.

5.2 Estimating Power Loss

Discharging the parasitic capacitance C_P into the DRAIN output of the HV9925 is responsible for the bulk of the switching power loss. It can be estimated using Equation 5-7.

EQUATION 5-7:

$$P_{SWITCH} = \left(\frac{C_P \times V_{IN}^2}{2} + V_{IN} \times I_{SAT} \times t_{rr}\right) \times F_S$$

Where:

F_S = Switching frequency

I_{SAT} = Saturated DRAIN current

Disregarding the voltage drop at HV9925 and D1, the switching frequency is derived using Equation 5-8.

EQUATION 5-8:

$$F_S = \frac{V_{IN} - V_O}{V_{IN} \times T_{OFF}}$$

When the HV9925 LED driver is powered from the full-wave rectified AC input, the switching power loss can be estimated as illustrated in Equation 5-9.

EQUATION 5-9:

$$P_{SWITCH} \approx \frac{1}{2 \times T_{OFF}}(V_{AC} \times C_P + 21_{SAT} \times t_{rr})(V_{AC} - V_O)$$

V_{AC} is the input AC line RMS voltage.

The switching power loss associated with turn-off transitions of the DRAIN output can be disregarded. Due to the large amount of parasitic capacitance connected to this switching node, the turn-off transition occurs essentially at zero voltage.

When the HV9925 LED driver is powered from DC input voltages, the conduction power loss can be calculated using the following equation: Equation 5-10.

EQUATION 5-10:

$$P_{COND} = (D \times I_O^2 \times R_{ON}) + I_{DD} \times V_{IN} \times (1 - D)$$

Where:

$D = V_O/V_{IN}$ is the duty ratio

R_{ON} = On resistance of internal MOSFET switch

I_{DD} = Internal linear regulator current

When the LED driver is powered from the full-wave rectified AC line input, the exact equation for calculating the conduction loss is more complicated. However, it can be estimated using the following equation.

EQUATION 5-11:

$$P_{COND} = (K_C \times I_O^2 \times R_{ON}) + (K_D \times I_{DD} \times V_{AC})$$

Where V_{AC} is the input AC line voltage. The coefficients K_C and K_D can be determined from the minimum duty ratio $D_M = 0.71V_O/(V_{AC})$.

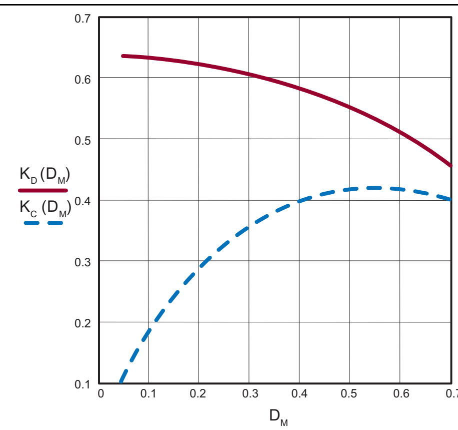


***FIGURE 5-1:** Conduction Loss Coefficients K_C and K_D.*

5.3 EMI Filter

As with all off-line converters, selecting an input filter is critical to obtaining good EMI. A switching side capacitor, albeit of small value, is necessary in order to ensure low impedance to the high frequency switching currents of the converter. As a rule of thumb, this capacitor should be approximately 0.1 µF/W to 0.2 µF/W of LED output power. A recommended input filter is shown in Figure 5-2 for the following design example:

5.4 Design Example 1

Let us design an HV9925 LED lamp driver meeting the following specifications:

Input: Universal AC, 85–264 VAC

Output Current: 20 mA

Load: String of 10 LED
(V_F = 4.1V, maximum each)

The schematic diagram of the LED driver is shown in Figure 5-2.

5.4.1 STEP 1: CALCULATE L1

The output voltage $V_O = 10 \times V_F \approx 41V$ (maximum). Use Equation 5-1 assuming a 30% peak-to-peak ripple current relative to average output current in the LED string. See Equation 5-12.

EQUATION 5-12:

$$L1 = \frac{(41V \times 10.5\mu s)}{(0.3 \times 20mA)} = 72mH$$

Select L1 = 68 mH, I = 30 mA. Typical SRF = 170 kHz. Calculate the coil capacitance. Refer to Equation 5-13.

EQUATION 5-13:

$$C_L = \frac{1}{L1 \times (2\Pi \times SRF)^2} = \frac{1}{68mH \times (2\Pi \times 170kHz)^2} \approx 13pF$$

5.4.2 STEP 2: SELECT D1

Usually the reverse recovery characteristics of ultra-fast rectifiers at I_F = 20 mA to 50 mA are not provided in the manufacturer's data books. The designer may need to experiment with different diodes to achieve the best result.

Select D1 with V_R = 600V, $t_{rr} \approx$ 20 ns, (I_F = 20 mA, I_{RR} = 100 mA) and $C_J \approx$ 8 pF (V_F > 50V).

5.4.3 STEP 3: CALCULATE TOTAL PARASITIC CAPACITANCE

Using Equation 5-4, C_{DRAIN} = 5 pF (maximum), PCB traces capacitance C_{PCB} = 5 pF (typical), and the above derived C_L and C_J values, the total parasitic capacitance is calculated in Equation 5-14.

EQUATION 5-14:

$$C_P = 5pF + 5pF + 13pF + 8pF = 31pF$$

5.4.4 STEP 4. CALCULATE THE LEADING EDGE SPIKE DURATION

Use Equation 5-5 and Equation 5-6, and take DRAIN saturation current I_{SAT} = 100 mA (minimum) and $V_{IN} = V_{AC(MAX)}$ = 264V. The leading edge spike duration is computed from Equation 5-15.

EQUATION 5-15:

$$T_{SPIKE} = \frac{264V \times \sqrt{2} \times 31pF}{100mA} + 20ns \approx 136ns < T_{BLANK(MIN)}$$

5.4.5 STEP 5: ESTIMATE THE POWER DISSIPATION IN HV9925 AT 264 VAC

Use Equation 5-9 and Equation 5-11 to calculate the power dissipation.

1. Switching Power Loss (See Equation 5-16.)

EQUATION 5-16:

$$P_{SWITCH} \approx \frac{1}{2 \times 10.5\mu s}(264V \times 31pF + 2 \times 100mA \times 20ns)(264V - 41V)$$

$$P_{SWITCH} \approx 130mW$$

2. Minimum Duty Ratio (See Equation 5-17.)

EQUATION 5-17:

$$D_M = \frac{(0.71 \times 41V)}{264V} \approx 0.11$$

3. Conduction Power Loss (See Equation 5-18.) K_C = 0.2 and K_D = 0.63 for D_M = 0.11 from the conduction loss coefficient curves in Figure 5-1.

EQUATION 5-18:

$$P_{COND} = 0.20 \times (20mA)^2 \times 200\Omega + 0.63 \times 200\mu A \times 264V \approx 50mW$$

4. Total Power Dissipation at $V_{AC(MAX)}$ (See Equation 5-19.)

EQUATION 5-19:

$$P_{D(TOTAL)} = P_{COND} + P_{SWITCH} = 130mW + 50mW = 180mW$$

5.4.6 STEP 6: SELECT INPUT CAPACITOR C_{IN}

The output power is calculated with Equation 5-20.

EQUATION 5-20:

$$P_{OUT} = 41V \times 20mA = 820mW$$

Select 0.1 µF, 400V metalized polyester film capacitor as C_{IN}.

5.5 Design Example 2

Let us now design a PWM-dimmable LED lamp driver using the HV9925:

Input: Universal AC, 85VAC to 135 VAC

Output Current: 50 mA

Load: String of 12 LED (V_F = 2.5V maximum each)

The schematic diagram of the LED driver is shown in Figure 5-3. We will use an aluminum electrolytic capacitor for C_{IN} to prevent interruptions of the LED current at zero crossings of the input voltage. As a rule of thumb, 2 µF to 3 µF per each watt of the input power is required for C_{IN} in this case.

5.5.1 STEP 1: CALCULATE L1.

The output voltage V_O = 12 x V_F = 30V (maximum). Use Equation 5-1 assuming a 30% peak-to-peak ripple current relative to average output current in the LED string. See Equation 5-21.

EQUATION 5-21:

$$L1 = \frac{(30V \times 10.5\mu s)}{(0.3 \times 50mA)} = 21mH$$

Select L1= 22 mH, I = 60 mA. Typical SRF = 270 kHz. Calculate the coil capacitance. See Equation 5-22.

EQUATION 5-22:

$$C_L = \frac{1}{L1 \times (2\Pi \times SRF)^2} = \frac{1}{22mH \times (2\Pi \times 270KHz)^2} \approx 15pF$$

5.5.2 STEP 2: SELECT D1

Select D1 with V_R = 400V, $t_{rr} \approx$ 35 ns and $C_J \leq$ 8 pF.

5.5.3 STEP 3: CALCULATE THE TOTAL PARASITIC CAPACITANCE

Use Equation 5-4. Take C_{DRAIN} = 5 pF (maximum), C_{PCB} = 5 pF (typical), and the above derived C_L and C_J values. The total parasitic capacitance is calculated from Equation 5-23.

EQUATION 5-23:

$$C_P = 5pF + 5pF + 15pF + 8pF = 33pF$$

5.5.4 STEP 4: CALCULATE THE LEADING EDGE SPIKE DURATION

Use Equation 5-5 and Equation 5-6, and take I_{SAT} = 100 mA (minimum) and $V_{IN} = V_{AC(MAX)}$ = 135V. The leading edge spike duration is computed from Equation 5-24.

EQUATION 5-24:

$$T_{SPIKE} = \frac{135V \times \sqrt{2} \times 33pF}{100mA} + 35ns \approx 98ns < T_{BLANK(MIN)}$$

5.5.5 STEP 5: ESTIMATE THE POWER DISSIPATION IN HV9925 AT 135 VAC

Perform the estimation using Equation 5-7, Equation 5-8, and Equation 5-11.

1. Switching Power Loss (See Equation 5-25 and Equation 5-26)

EQUATION 5-25:

$$F_s = \frac{135V - 30V}{135V \times 10.5\mu s} = 74kHz$$

EQUATION 5-26:

$$P_{SWITCH} = \frac{(33pF \times (135V)^2 + 135V \times 2 \times 100mA \times 35ns)}{2} \times 74kHz$$

$$P_{SWITCH} \approx 57mW$$

2. Minimum Duty Ratio (See Equation 5-27.)

EQUATION 5-27:

$$D_M = \frac{30V}{(135 \times \sqrt{2})} \approx 0.16$$

3. Conduction Power Loss (See Equation 5-28.)

K_C = 0.25 and K_D = 0.62 for D_M = 0.16 from the conduction loss coefficient curves in Figure 5-1.

EQUATION 5-28:

$$P_{COND} = 0.25 \times (50mA)^2 \times 200\Omega + 0.62 \times 0.5mA \times 135V$$

$$P_{COND} = 167mW$$

4. Total Power Dissipation in HV9925 (See Equation 5-29.)

EQUATION 5-29:

$$P_{D(TOTAL)} = 57mW + 167mW = 224mW$$

5.5.6 STEP 6: SELECT INPUT CAPACITOR C_{IN}

The output power is calculated from Equation 5-30.

EQUATION 5-30:

$$P_{OUT} = 30V \times 50mA = 1.5W$$

Select 3.3 µF, 250V aluminum electrolytic capacitor as C_{IN}.

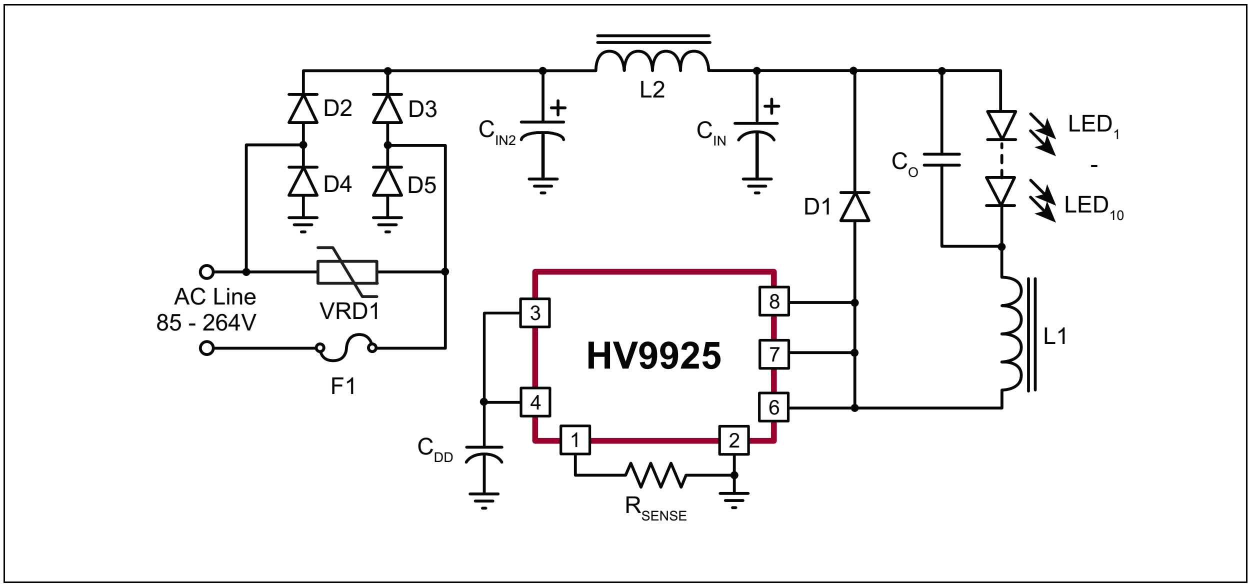


FIGURE 5-2: *Universal 85 VAC to 264 VAC LED Lamp Driver. (I_O = 20 mA, V_O = 41V from Example 1)*

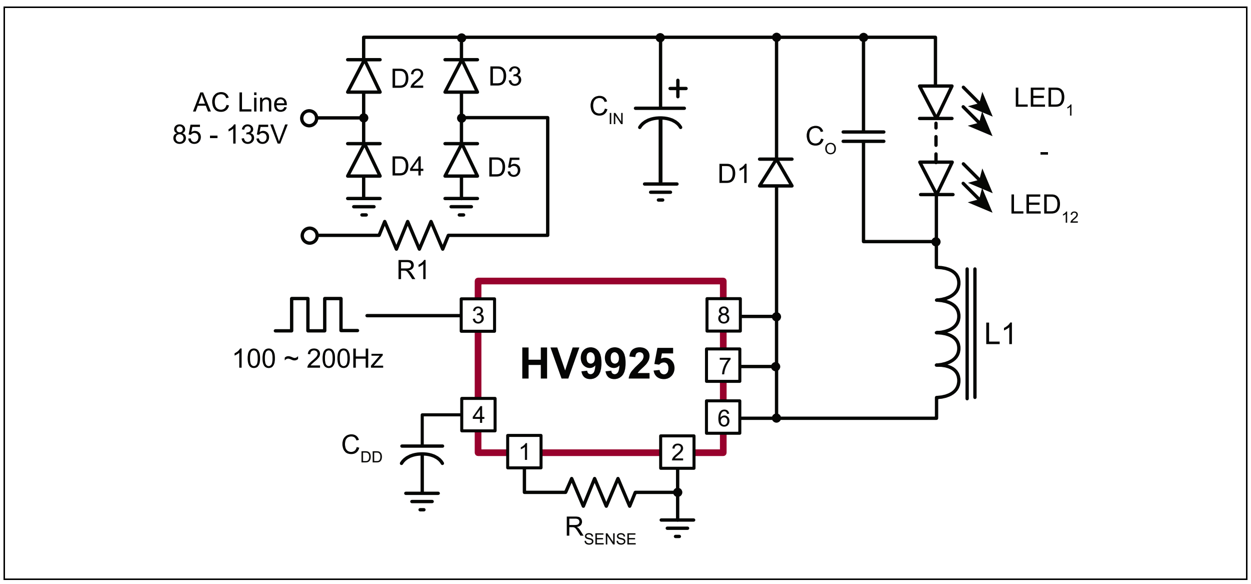


FIGURE 5-3: *85 VAC to 135 VAC LED Lamp Driver with PWM Dimming. (I_O = 50 mA, V_O = 30V from Example 2)*

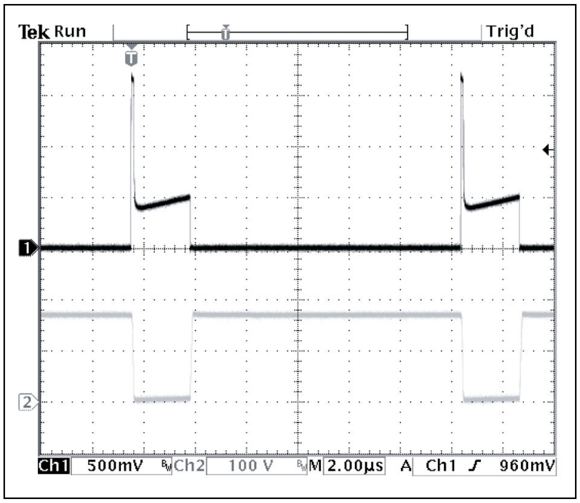


FIGURE 5-4: *Switching Waveforms. CH1: V_{RSENSE}, CH2: V_{DRAIN}.*

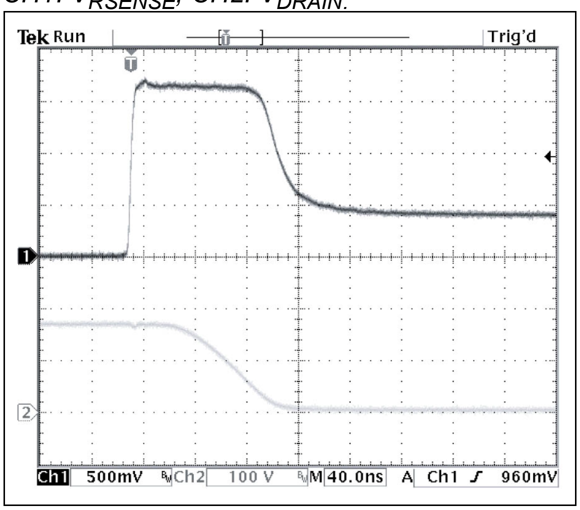


FIGURE 5-5: *Switch-On Transition–Leading Edge Spike. CH1: V_{RSENSE}, CH2: V_{DRAIN}.*

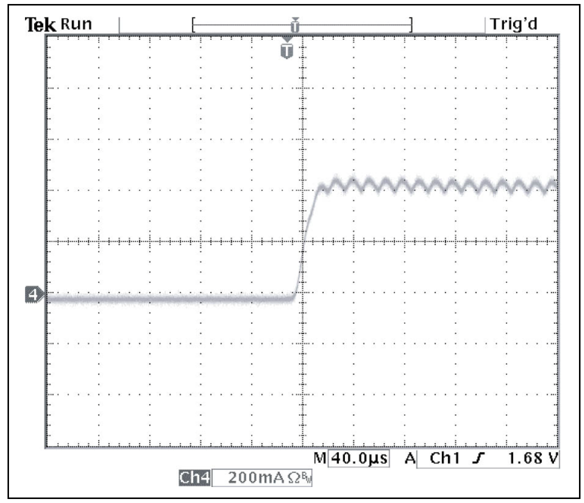


FIGURE 5-6: *PWM Dimming–Rising Edge. CH4: 10 × I_{OUT}.*

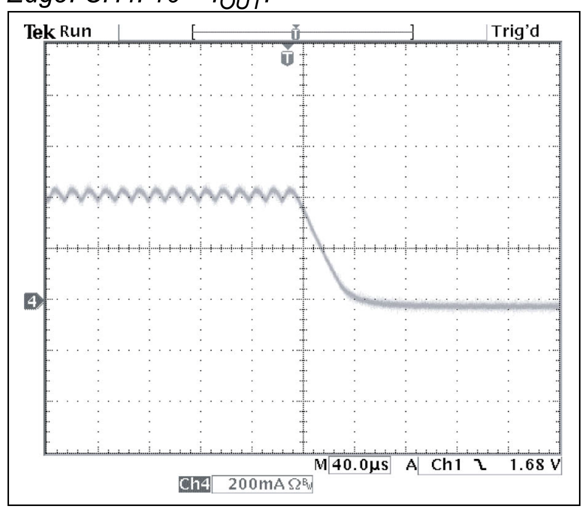
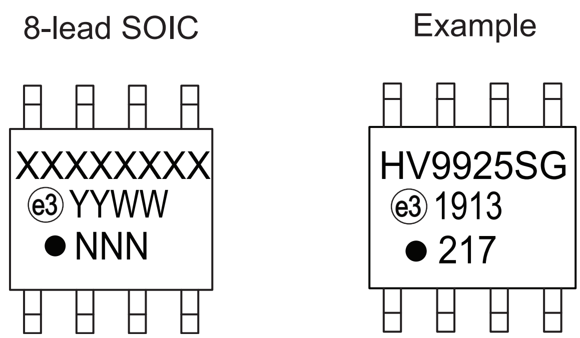


FIGURE 5-7: *PWM Dimming–Falling Edge. CH4: 10 × I_{OUT}.*

6.0 PACKAGING INFORMATION

6.1 Package Marking Information

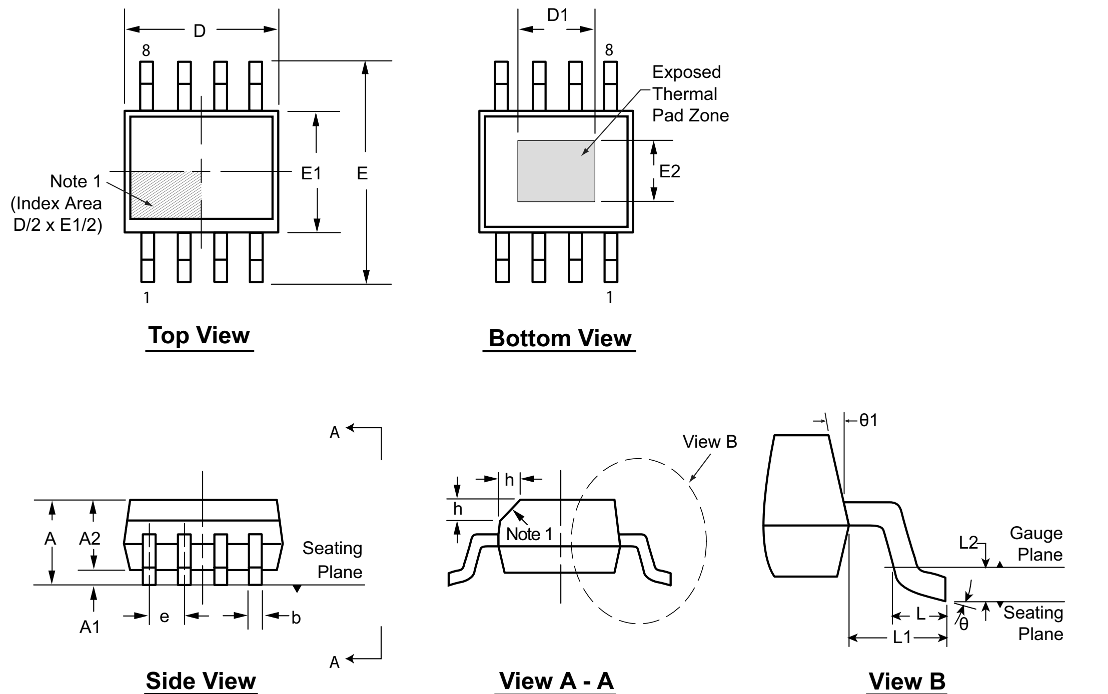


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

8-Lead SOIC (Narrow Body w/Heat Slug) Package Outline (SG)

4.90x3.90mm body, 1.70mm height (max), 1.27mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

1. *If optional chamfer feature is not present, a Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/ identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	D1	E	E1	E2	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.25*	0.00	1.25	0.31	4.80*	3.30†	5.80*	3.80*	2.29†	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	4.90	-	6.00	3.90	-		-	-			-	-
	MAX	1.70	0.15	1.55*	0.51	5.00*	3.81†	6.20*	4.00*	2.79†		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation BA, Issue E, Sept. 2005.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings not to scale.

APPENDIX A: REVISION HISTORY

Revision A (December 2019)

- Converted Supertex Doc# DSFP-HV9925 to Microchip
- Updated the quantity of the 8-lead SOIC (with heat slug) SG package from 2500/Reel to 3300/Reel to align it with the actual BQM
- Made minor text changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	HV9925	=	Programmable Current LED Lamp Driver IC with PWM Dimming
Packages:	SG	=	8-lead SOIC with Heat Slug
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Type:	(Blank)	=	3300/Reel for an SG Package

Examples:

a) HV9925SG-G: Programmable Current LED Lamp Driver IC with PWM Dimming, 8-lead SOIC w/Heat Slug Package, 3300/Reel

Note the following details of the code protection feature on Microchip devices:

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