LND01

Lateral N-Channel Depletion-Mode MOSFET

Features

- Bi-directional
- Low On-resistance
- Low Input Capacitance
- Fast Switching Speeds
- High Input Impedance and High Gain
- Low Power Drive Requirement
- Ease of Paralleling

Applications

- Normally-on Switches
- Solid-state Relays
- Converters
- Constant Current Sources
- Analog Switches

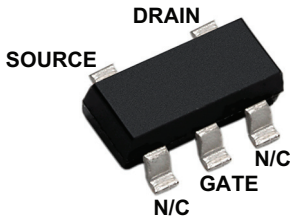
General Description

The LND01 is a low-threshold, Depletion-mode (normally-on) transistor that uses an advanced lateral DMOS structure and a well-proven silicon gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors as well as the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally induced secondary breakdown.

The body of the transistor is connected to the gate pin. The channel is therefore being pinched off by both the gate and body. The gate pin has a diode connected to the drain terminal and another diode connected to the source terminal.

Package Type

5-lead SOT-23



See Table 2-1 for pin information.

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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Drain-to-source Voltage ..... BV_{DSX}
Source-to-drain Voltage..... BV_{SDX}
Gate-to-source Voltage ..... –12V to +0.6V
Gate-to-drain Voltage ..... –12V to +0.6V
Operating Ambient Temperature, T_A ..... –25°C to +125°C

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: T_A = 25°C unless otherwise specified. (**Note 1**)

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Drain-to-source Breakdown Voltage	BV_{DSX}	9	—	—	V	V_{GS} = –3V, I_{DS} = 10 µA
Source-to-drain Breakdown Voltage	BV_{SDX}	9	—	—	V	V_{GD} = –3V, I_{SD} = 10 µA
Gate-to-source Off Voltage	$V_{GS(OFF)}$	–0.8	—	–3	V	V_{DS} = 9V, I_{DS} = 1 µA
Source-to-gate Off Voltage	$V_{SG(OFF)}$	–0.8	—	–3	V	V_{SD} = 9V, I_{SD} = 1 µA
Gate-to-source Diode	V_{GS}	–12	—	0.6	V	I_{GS} = ±1 µA
Gate-to-drain Diode	V_{GD}	–12	—	0.6	V	I_{GD} = ±1 µA
Drain-to-source Leakage Current	$I_{DS(OFF)}$	—	—	1	µA	V_{GS} = –3V, V_{DS} = 9V
Source-to-drain Leakage Current	$I_{SD(OFF)}$	—	—	1	µA	V_{GD} = –3V, V_{SD} = 9V
Saturated Drain-to-source Current	I_{DSS}	300	—	—	mA	V_{GS} = 0V, V_{DS} = 9V
Saturated Source-to-drain Current	I_{SDD}	300	—	—	mA	V_{GD} = 0V, V_{SD} = 9V
Static Drain-to-source On-state Resistance	$R_{DS(ON)}$	—	0.9	1.4	Ω	V_{GS} = 0V, I_{DS} = 100 mA
Static Source-to-drain On-state Resistance	$R_{SD(ON)}$	—	0.9	1.4	Ω	V_{GD} = 0V, I_{SD} = 100 mA

Note 1: All DC parameters are 100% tested at 25°C unless otherwise stated. (Pulse test: 300 µs pulse, 2% duty cycle)
2: Specification is obtained by characterization and is not 100% tested.

AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: T_A = 25°C unless otherwise specified. (**Note 2**)

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Forward Transconductance	G_{FS}	200	—	—	mmho	V_{DS} = 9V, I_{DS} = 50 mA
Input Capacitance	C_{ISS}	—	46	—	pF	V_{GS} = –3V, V_{DS} = 5V, f = 1 MHz
Common Source Output Capacitance	C_{OSS}	—	32	—	pF	
Reverse Transfer Capacitance	C_{RSS}	—	23	—	pF	
Turn-on Delay Time	$t_{d(ON)}$	—	3.8	—	ns	V_{DD} = 9V, I_{DS} = 100 mA, R_{GEN} = 25Ω
Rise Time	t_r	—	11	—	ns	
Turn-off Delay Time	$t_{d(OFF)}$	—	1	—	ns	
Fall Time	t_f	—	6.4	—	ns	

Note 1: All DC parameters are 100% tested at 25°C unless otherwise stated. (Pulse test: 300 µs pulse, 2% duty cycle)
2: Specification is obtained by characterization and is not 100% tested.

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TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise specified, for all specifications $T_A = T_J$ = +25°C.						
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
TEMPERATURE RANGE						
Operating Ambient Temperature	T_A	–25	—	+125	°C	
PACKAGE THERMAL RESISTANCE						
5-lead SOT-23	θ_{JA}	—	253	—	°C/W	

THERMAL CHARACTERISTICS

Package	**I_D (1) (Continuous) (mA)**	**I_D (Pulsed) (mA)**	**Power Dissipation at T_C = 25°C (W)**
5-lead SOT-23	330	600	0.36

Note 1: I_D (continuous) is limited by maximum T_J.

2.0 PIN DESCRIPTION

Table 2-1 shows the description of pins in LND01.
Refer to **Package Type** for the location of pins.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	N/C	Not connected
2	Gate	Gate
3	N/C	Not connected
4	Drain	Drain
5	Source	Source

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3.0 FUNCTIONAL DESCRIPTION

Figure 3-1 illustrates the switching waveforms and test circuit for LND01.

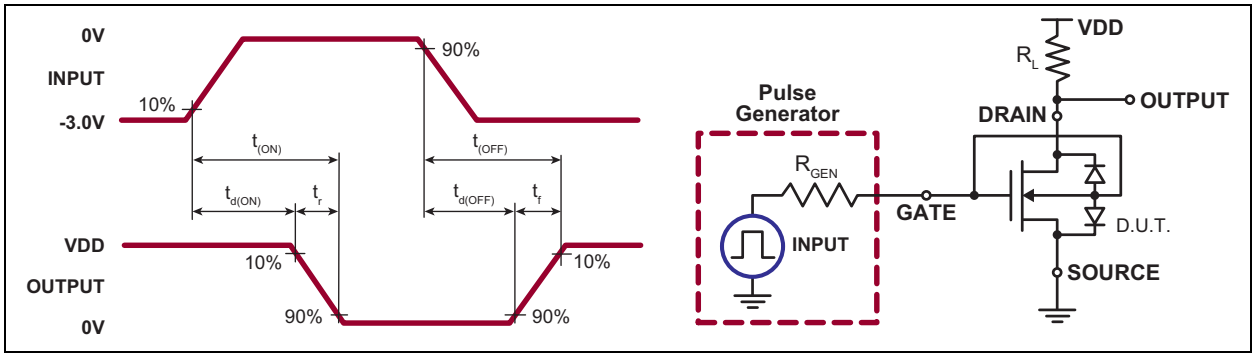


FIGURE 3-1: *Switching Waveforms and Test Circuit.*

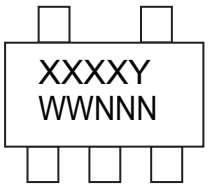
TABLE 3-1: PRODUCT SUMMARY

BV_{DSX}/BV_{SDX} (V)	$R_{DS(ON)}/R_{SD(ON)}$ (Maximum) (Ω)	I_{DSS}/I_{SSD} (Maximum) (mA)
9	1.4	300

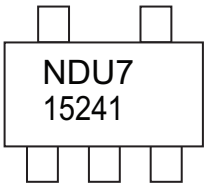
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

5-lead SOT-23



Example



Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	(e4)	Pre-plated

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

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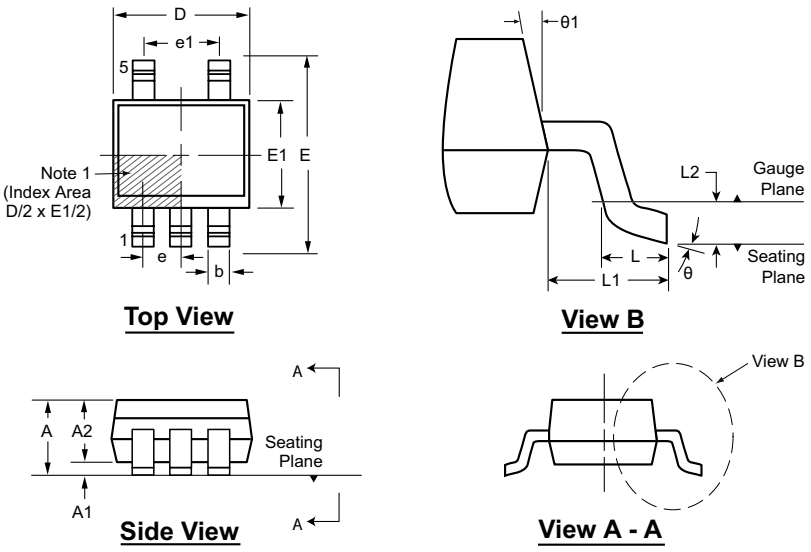
5-Lead SOT-23 Package Outline (K1)

2.90x1.60mm body, 1.45mm height (max), 0.95mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	e1	L	L1	L2	θ	θ1
Dimension (mm)	MIN	0.90*	0.00	0.90	0.30	2.75*	2.60*	1.45*	0.95 BSC	1.90 BSC	0.30	0.60 REF	0.25 BSC	0°	5°
	NOM	-	-	1.15	-	2.90	2.80	1.60			0.45			4°	10°
	MAX	1.45	0.15	1.30	0.50	3.05*	3.00*	1.75*			0.60			8°	15°

JEDEC Registration MO-178, Variation AA, Issue C, Feb. 2000.
** This dimension is not specified in the JEDEC drawing.*
Drawings not to scale.

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NOTES:

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APPENDIX A: REVISION HISTORY

Revision A (June 2017)

- Converted Supertex Doc# DSFP-LND01 to Microchip DS20005696A
- Changed the package marking format
- Changed the quantity of the 5-lead SOT-23 K1 package from 2500/Reel to 3000/Reel
- Made minor text changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	LND01	=	Lateral N-Channel Depletion-Mode MOSFET
Package:	K1	=	5-lead SOT-23
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Type:	(blank)	=	3000/Reel for a K1 Package

Example:

a) LND01K1-G: Lateral N-Channel Depletion-Mode MOSFET, 5-lead SOT-23, 3000/Reel

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