



FEATURES

- 3.3V power supply
- 620ps propagation delay
- Fully differential design
- Supports low voltage operation
- Available in 20-pin SOIC package

DESCRIPTION

The SY100EL91L is a triple LVPECL-to-ECL or LVPECL-to-LVECL translator.

A V_{BB} output is provided for interfacing with single ended PECL signals at the input. If a single ended input is to be used, the V_{BB} output should be connected to the \bar{D} input. The active signal would then drive the D input. When used, the V_{BB} output should be bypassed to ground via a $0.01\mu\text{F}$ capacitor. The V_{BB} output is designed to act as the switching reference for the EL91L under single ended input switching conditions. As a result this pin can only source/sink up to 0.5mA of current.

To accomplish the level translation the EL91L requires three power rails. The V_{CC} supply should be connected to the positive supply, and the V_{EE} pin should be connected to the negative power supply. The GND pins as expected are connected to the system ground plane. Both V_{EE} and V_{CC} should be bypassed to ground via $0.01\mu\text{F}$ capacitors.

Under open input conditions, the \bar{D} input will be biased at $V_{CC}/2$ and the D input will be pulled to GND. This condition will force the Q output to a LOW, ensuring stability.

FUNCTION TABLE

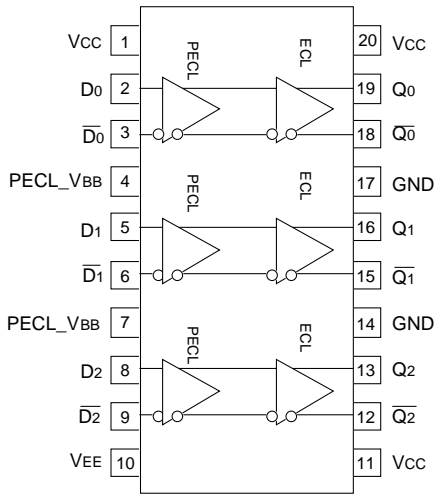
Function	Vcc	VEE
LVPECL-to-ECL	3.3V	-5.0V
LVPECL-to-LVECL	3.3V	-3.3V

PIN NAMES

Pin	Function
Dn	PECL Inputs
Qn	ECL Outputs
PECL_VBB	PECL Reference Voltage Output

PACKAGE/ORDERING INFORMATION

Ordering Information⁽¹⁾



Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100EL91LZC	Z20-1	Commercial	SY100EL91LZC	Sn-Pb
SY100EL91LZCTR ⁽²⁾	Z20-1	Commercial	SY100EL91LZC	Sn-Pb
SY100EL91LZI	Z20-1	Industrial	SY100EL91LZI	Sn-Pb
SY100EL91LZITR ⁽²⁾	Z20-1	Industrial	SY100EL91LZI	Sn-Pb
SY100EL91LZG ⁽³⁾	Z20-1	Industrial	SY100EL91LZG with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY100EL91LZGTR ^(2, 3)	Z20-1	Industrial	SY100EL91LZG with Pb-Free bar-line indicator	Pb-Free NiPdAu

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

20-Pin Wide SOIC (Z20-1)

3.3V LVPECL INPUT DC ELECTRICAL CHARACTERISTICS⁽¹⁾

Symbol	Parameter	TA = -40°C			TA = 0°C			TA = +25°C			TA = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
VCC	Power Supply Voltage	3.0	—	3.8	3.0	—	3.8	3.0	3.3	3.8	3.0	—	3.8	V
V _{IH}	Input HIGH Voltage ⁽²⁾	2.135	—	2.420	2.135	—	2.420	2.135	2.350	2.420	2.135	—	2.420	V
V _{IL}	Input LOW Voltage ⁽²⁾	1.490	—	1.825	1.490	—	1.825	1.490	—	1.825	1.490	—	1.825	V
I _{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	—	—	150	μA
I _{IL}	Input LOW Current $\frac{Dn}{Dn}$	0.5 -600	— —	— —	0.5 -600	— —	— —	0.5 -600	— —	— —	0.5 -600	— —	— —	μA
V _{BB}	Output Reference ⁽²⁾	1.920	—	2.040	1.920	—	2.040	1.920	—	2.040	1.920	—	2.040	V
I _{CC}	Power Supply Current	—	—	10	—	—	10	—	6.0	10	—	—	10	mA

Notes:

1. Parametric values specified at: 3 volt Power Supply Range 100EL91L Series -3.0V to -3.8V.
2. These levels are for V_{CC} = 3.3V. Level specifications will vary 1:1 with V_{CC}.

ECL/LVECL OUTPUT DC ELECTRICAL CHARACTERISTICS⁽¹⁾

Symbol	Parameter	TA = -40°C			TA = 0°C			TA = +25°C			TA = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V _{EE}	Power Supply Voltage $\frac{ECL}{LVECL}$	-4.2	—	-5.5	-4.2	—	-5.5	-4.2	—	-5.5	-4.2	—	-5.5	V
		-3.0	—	-3.8	-3.0	—	-3.8	-3.0	—	-3.8	-3.0	—	-3.8	
V _{OH}	Output HIGH Voltage	-1085	—	-880	-1025	—	-880	-1025	-955	-880	-1025	—	-880	mV
V _{OL}	Output LOW Voltage	-1830	—	-1555	-1810	—	-1620	-1810	-1705	-1620	-1810	—	-1620	mV
I _{EE}	Power Supply Current	—	—	28	—	—	28	—	22	28	—	—	30	mA

Note:

1. Parametric values specified at: 3 volt Power Supply Range 100EL91L Series -3.0V to -3.8V.

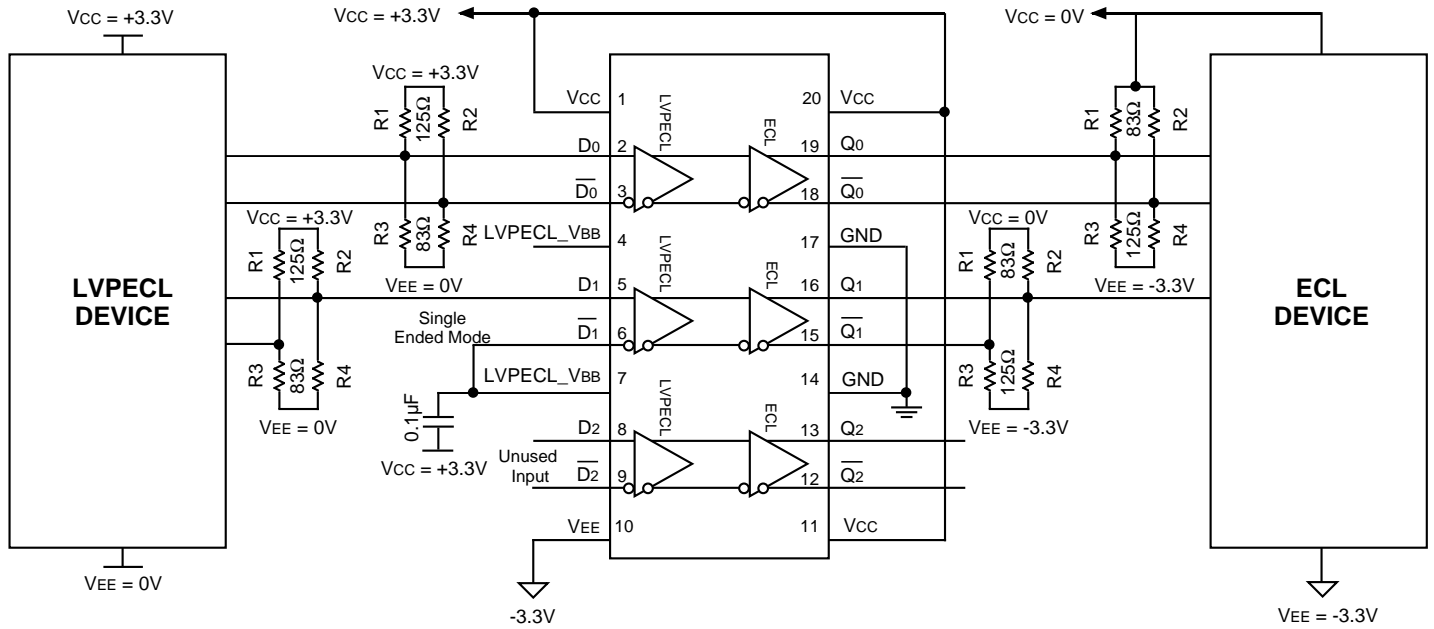
AC ELECTRICAL CHARACTERISTICS⁽⁴⁾LVPECL: $V_{CC} = +3.0V$ to $+3.8V$, ECL: $V_{EE} = -4.2V$ to $-5.5V$, LVECL: $V_{EE} = -3.0V$ to $-3.8V$

Symbol	Parameter	TA = -40°C			TA = 0°C			TA = +25°C			TA = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t _{PD}	Propagation Delay D to Q	490	590	690	510	610	710	520	620	720	560	660	760	ps
	Diff. S.E.	440	590	740	460	610	760	470	620	770	510	660	810	
t _{skew}	Within-Device Skew ⁽¹⁾	—	40	100	—	40	100	—	40	100	—	40	100	ps
	Output-to-Output	—	—	200	—	—	200	—	—	200	—	—	200	
	Part-to-Part (Diff.) Duty Cycle (Diff.)	—	25	—	—	25	—	—	25	—	—	25	—	
V _{PP}	Minimum Input Swing ⁽²⁾	150	—	—	150	—	—	150	—	—	150	—	—	mV
V _{CMR}	Common Mode Range ⁽³⁾	1.3	—	V _{CC} -0.2	1.2	—	V _{CC} -0.2	1.2	—	V _{CC} -0.2	1.2	—	V _{CC} -0.2	V
	V _{PP} < 500mV	1.5	—	V _{CC} -0.2	1.4	—	V _{CC} -0.2	1.4	—	V _{CC} -0.2	1.4	—	V _{CC} -0.2	
	V _{PP} > 500mV	1.5	—	V _{CC} -0.2	1.4	—	V _{CC} -0.2	1.4	—	V _{CC} -0.2	1.4	—	V _{CC} -0.2	
t _r t _f	Output Rise/Fall Times Q (20% to 80%)	320	400	580	320	400	580	320	400	580	320	400	580	ps

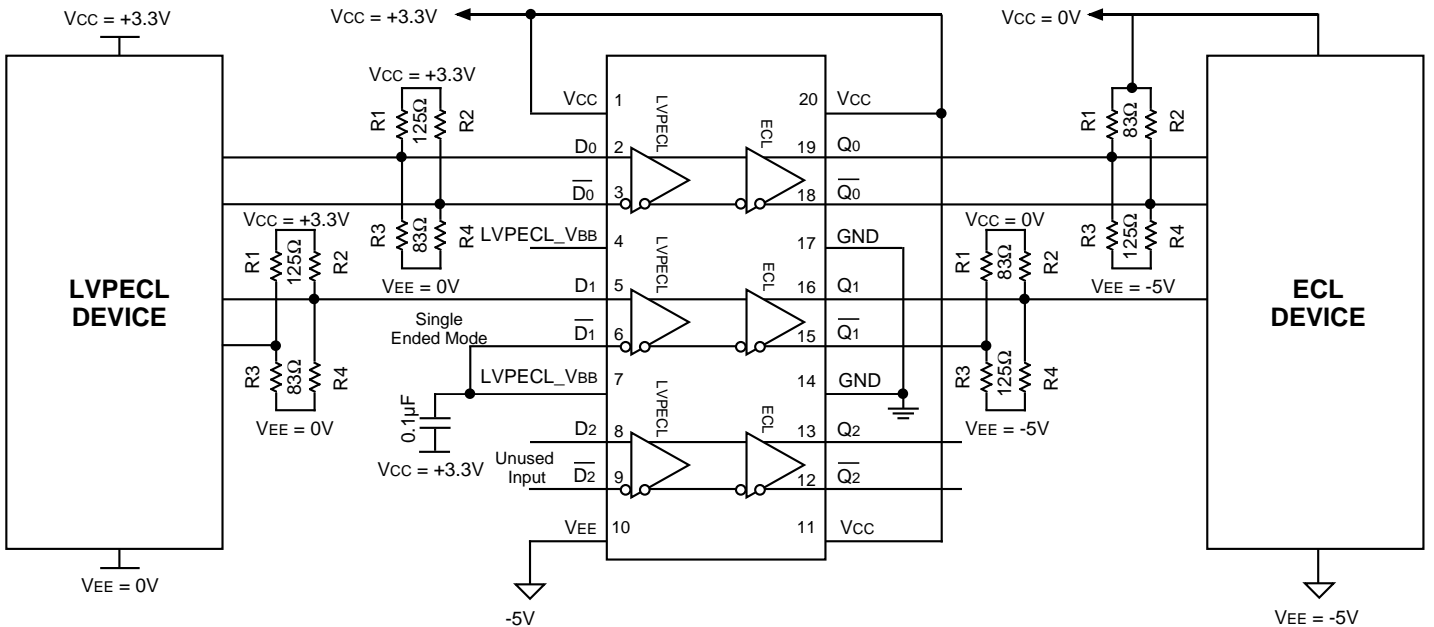
Notes:

- Skew is measured between outputs under identical transitions.
- Minimum input swing for which AC parameters are guaranteed. The device has a DC gain of ~40.
- The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP} min. and 1V.
- Parametric values specified at: 3 volt Power Supply Range 100EL91L Series -3.0V to -3.8V.

LVPECL-TO-ECL MODE CONFIGURATION



3.3V Configuration

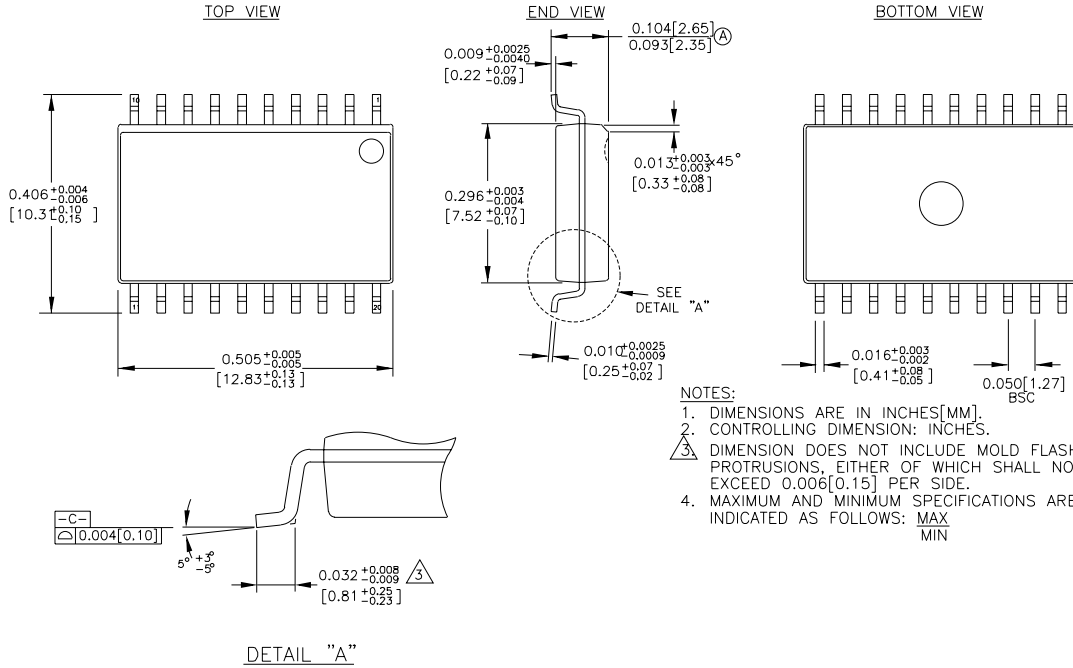


5.0V Configuration

Notes:

1. The schematic above demonstrates three different ways that all or any inputs of SY100EL91L can be used. The three modes or operation are: Differential LVPECL, Single-Ended LVPECL, and/or Open.
2. If D2 and $\overline{D2}$ are used in differential mode, then the same scheme of D0 and $\overline{D0}$ applies. If used in single-ended mode, then use the same scheme of D1 and $\overline{D1}$.

20-PIN SOIC .300" WIDE (Z20-1)



Rev. 03

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