

Specification for Approval

Date: 2022/02/25

Customer : 天河星

TAI-TECH P/N: DFP252012BF-R24M

CUSTOMER P/N: _____

DESCRIPTION: _____

QUANTITY: _____ pcs

REMARK:		
Customer Approval Feedback		

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Power Inductor

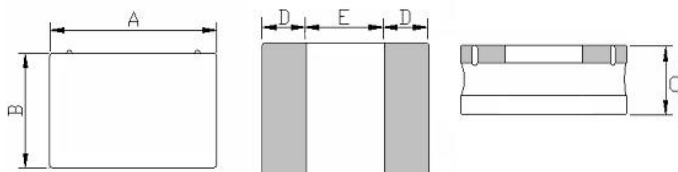
DFP252012BF-R24M

1. Features

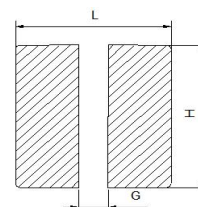
1. This specification applies Low Profile Power Inductors.
2. 100% Lead(Pb) & Halogen-Free and RoHS compliant.
3. Operating temperature : -40~+125°C (Including self - temperature rise)



2. Dimension



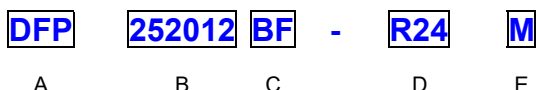
Recommended PC Board Pattern



Series	A(mm)	B(mm)	C(mm)	D(mm)	E(mm)
DFP252012BF	2.5 -0.1/+0.2	2.0 -0.1/+0.2	1.2Max	0.85 ref	0.80 ref

L(mm)	G(mm)	H(mm)
2.9	0.8	2.4

3. Part Numbering



- A: Series
- B: Dimension
- C: Lead Free Material
- D: Inductance R24=0.24uH
- E: Inductance Tolerance K=±10%, L=±15%,M=±20%,Y=±30%.

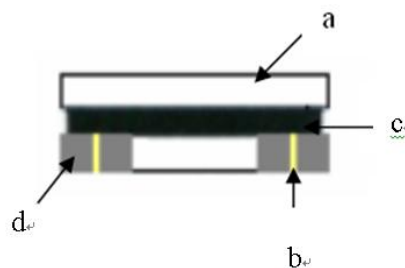
4. Specification

TAI-TECH Part Number	Inductance (uH)	Test Frequency (Hz)	DCR (Ω)		I sat (A)		I rms (A)	
			typ	Max	typ	Max	typ	Max
DFP252012BF-R24M	0.24	0.1V/1M	0.024	0.028	8.00	6.50	4.70	4.20

Note:
 Isat : Saturation Current (Isat) will cause L0 to drop approximately 30%.
 Irms : Heat Rated Current (Irms) will cause the coil temperature rise approximately ΔT of 40°C
 Rated DC current: The lower value of Irms and Isat.

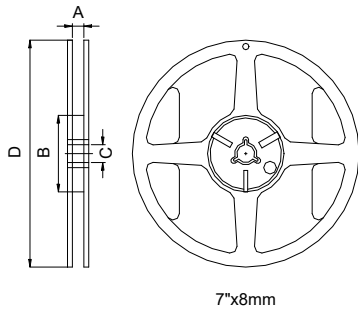
5. Material List

No.	Description	Specification
a.	Core	Ferrite Core
b.	Wire	Enameled Copper Wire
c.	Glue	Epoxy with magnetic powder
d.	Terminal	Ag/Ni/Sn



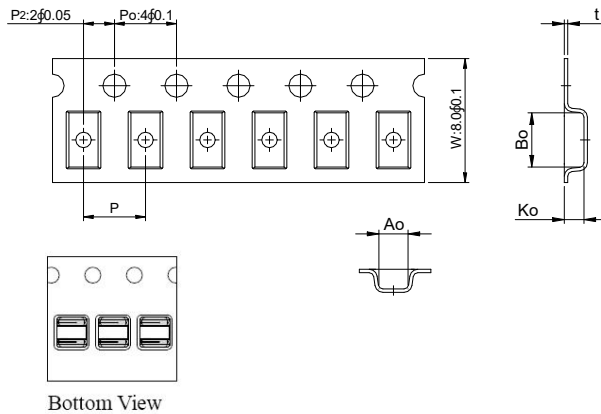
6. Packaging Information

6-1. Reel Dimension



Type	A(mm)	B(mm)	C(mm)	D(mm)
7"x8mm	8.4±1.0	50 min	13±0.8	178±2

6-2. Tape Dimension

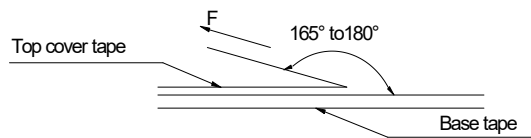


Series	Size	Bo(mm)	Ao(mm)	Ko(mm)	P(mm)	t(mm)
DFP	252012	3.10±0.1	2.45±0.1	1.40±0.1	4.0±0.1	0.23±0.05

6-3. Packaging Quantity

Chip size	252012
Chip / Reel	2000

6-4. Tearing Off Force

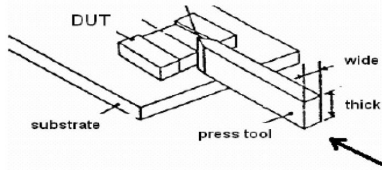


The force for tearing off cover tape is 10 to 130 grams in the arrow direction under the following conditions(referenced ANSI/EIA-481-D-2008 of 4.11 standard).

Tearing Speed mm	Room Temp. (°C)	Room Humidity (%)	Room atm (hPa)
300±10%	5~35	45~85	860~1060

7. Reliability and Test Condition

Item	Performance	Test Condition
Operating temperature	-40~+125℃ (Including self - temperature rise)	
Storage temperature	1. -10~+40℃, 50~60%RH (Product with taping) 2. -40~+125℃ (on board)	
Electrical Performance Test		
Inductance	Refer to standard electrical characteristics list.	HP4284A, CH11025, CH3302, CH1320, CH1320S LCR Meter.
DCR		CH16502, Agilent33420A Micro-Ohm Meter.
Saturation Current (Isat)	Approximately ΔL 30%.	Saturation DC Current (Isat) will cause L0 to drop ΔL (%)
Heat Rated Current (Irms)	Approximately ΔT 40℃	Heat Rated Current (Irms) will cause the coil temperature rise ΔT (℃) without core loss. 1. Applied the allowed DC current 2. Temperature measured by digital surface thermometer
Reliability Test		
Life Test	Appearance: No damage. Inductance: within $\pm 10\%$ of initial value Q: Shall not exceed the specification value. RDC: within $\pm 15\%$ of initial value and shall not exceed the specification value.	Preconditioning: Run through IR reflow for 3 times. (IPC/JEDEC J-STD-020E Classification Reflow Profiles) Temperature: 125 ± 2 ℃ (Inductor + ambient + temp rise) Applied current: rated current Duration: 1000 ± 12 hrs Measured at room temperature after placing for 24 ± 2 hrs
Load Humidity		Preconditioning: Run through IR reflow for 3 times. (IPC/JEDEC J-STD-020E Classification Reflow Profiles) Humidity: 85 $\pm 2\%$ R.H. Temperature: 85 ± 2 ℃ Duration: 1000hrs Min. Bead: with 100% rated current, Inductance: with 100% rated current Measured at room temperature after placing for 24 ± 2 hrs.
Moisture Resistance		Preconditioning: Run through IR reflow for 3 times. (IPC/JEDEC J-STD-020E Classification Reflow Profiles) 1. Baked at 50℃ for 25hrs, measured at room temperature after placing for 4 hrs. 2. Raise temperature to 65 ± 2 ℃ 90-100%RH in 2.5hrs, and keep 3 hours, cool down to 25℃ in 2.5hrs. 3. Raise temperature to 65 ± 2 ℃ 90-100%RH in 2.5hrs, and keep 3 hours, cool down to 25℃ in 2.5hrs, keep at 25℃ for 2 hrs then keep at -10℃ for 3 hrs 4. Keep at 25℃ 80-100%RH for 15min and vibrate at the frequency of 10 to 55 Hz to 10 Hz, measure at room temperature after placing for 1~2 hrs.
Thermal shock		Preconditioning: Run through IR reflow for 3 times. (IPC/JEDEC J-STD-020E Classification Reflow Profiles) Condition for 1 cycle Step1: -40 ± 2 ℃ 30 ± 5 min Step2: 125 ± 2 ℃ ≤ 0.5 min Step3: 125 ± 2 ℃ 30 ± 5 min Number of cycles: 500 Measured at room fempraturc after placing for 24 ± 2 hrs.
Vibration		Preconditioning: Run through IR reflow for 3 times. (IPC/JEDEC J-STD-020E Classification Reflow Profiles) Oscillation Frequency: 10Hz~2KHz~10Hz for 20 minutes Equipment: Vibration checker Total Amplitude: 10g Testing Time: 12 hours(20 minutes, 12 cycles each of 3 orientations).

Item	Performance	Test Condition															
Bending	Appearance : No damage.	Shall be mounted on a FR4 substrate of the following dimensions: >=0805 inch(2012mm):40x100x1.2mm <0805 inch(2012mm):40x100x0.8mm Bending depth: >=0805 inch(2012mm):1.2mm <0805 inch(2012mm):0.8mm duration of 10 sec.															
Shock	Inductance : within±10% of initial value Q : Shall not exceed the specification value. RDC : within ±15% of initial value and shall not exceed the specification value	<table border="1" data-bbox="1018 376 1447 510"> <thead> <tr> <th>Type</th> <th>Peak value (g's)</th> <th>Normal duration (D) (ms)</th> <th>Wave form</th> <th>Velocity change (V)ft/sec</th> </tr> </thead> <tbody> <tr> <td>SMD</td> <td>50</td> <td>11</td> <td>Half-sine</td> <td>11.3</td> </tr> <tr> <td>Lead</td> <td>50</td> <td>11</td> <td>Half-sine</td> <td>11.3</td> </tr> </tbody> </table> shocks in each direction along 3 perpendicular axes(18 shocks).	Type	Peak value (g's)	Normal duration (D) (ms)	Wave form	Velocity change (V)ft/sec	SMD	50	11	Half-sine	11.3	Lead	50	11	Half-sine	11.3
Type	Peak value (g's)	Normal duration (D) (ms)	Wave form	Velocity change (V)ft/sec													
SMD	50	11	Half-sine	11.3													
Lead	50	11	Half-sine	11.3													
Solder ability	More than 95% of the terminal electrode should be covered with solder .	a. Method B1, 4 hrs @155°C dry heat @235°C±5°C Test time:5 +0/-0.5 seconds. b. Method D category 3. (steam aging 8hours ± 15 min)@ 260°C±5°C Test time: 30 +0/-0.5 seconds.															
Resistance to Soldering Heat		Depth: completely cover the termination <table border="1" data-bbox="1007 741 1433 857"> <thead> <tr> <th>Temperature(°C)</th> <th>Time(s)</th> <th>Temperature ramp/immersion and emersion rate</th> <th>Number of heat cycles</th> </tr> </thead> <tbody> <tr> <td>260 ±5 (solder temp)</td> <td>10 ±1</td> <td>25mm/s ±6 mm/s</td> <td>1</td> </tr> </tbody> </table>	Temperature(°C)	Time(s)	Temperature ramp/immersion and emersion rate	Number of heat cycles	260 ±5 (solder temp)	10 ±1	25mm/s ±6 mm/s	1							
Temperature(°C)	Time(s)	Temperature ramp/immersion and emersion rate	Number of heat cycles														
260 ±5 (solder temp)	10 ±1	25mm/s ±6 mm/s	1														
Terminal Strength	Appearance : No damage. Inductance : within±10% of initial value Q : Shall not exceed the specification value. RDC : within ±15% of initial value and shall not exceed the specification value e	Preconditioning: Run through IR reflow for 3 times.(IPC/JEDEC J-STD-020E Classification Reflow Profiles With the component mounted on a PCB with the device to be tested, apply a force (>0805inch(2012mm):1kg, <=0805inch(2012mm):0.5kg) to the side of a device being tested. This force shall be applied for 60 +1 seconds. Also the force shall be applied gradually as not to apply a shock to the component being tested. 															

Note : When there are questions concerning measurement result : measurement shall be made after 48 ± 2 hours of recovery under the standard condition.

8.Soldering Specifications

(1) Soldering

Mildly activated rosin fluxes are preferred. TAI-TECH terminations are suitable for re-flow soldering systems. If hand soldering cannot be avoided, the preferred technique is the utilization of hot air soldering tools.

(2) Soldering Reflow:

Recommended temperature profiles for lead free re-flow soldering in Figure 1. Table 1.1&1.2 (J-STD-020E)

(3) Iron Reflow:

Products attachment with a soldering iron is discouraged due to the inherent process control limitations. In the event that a soldering iron must be employed the following precautions are recommended.(Fig. 2)

- Preheat circuit and products to 150°C
- Never contact the ceramic with the iron tip
- Use a 20 watt soldering iron with tip diameter of 1.0mm
- 355°C tip temperature (max)
- 1.0mm tip diameter (max)
- Limit soldering time to 4~5sec.

Fig.1 Soldering Reflow

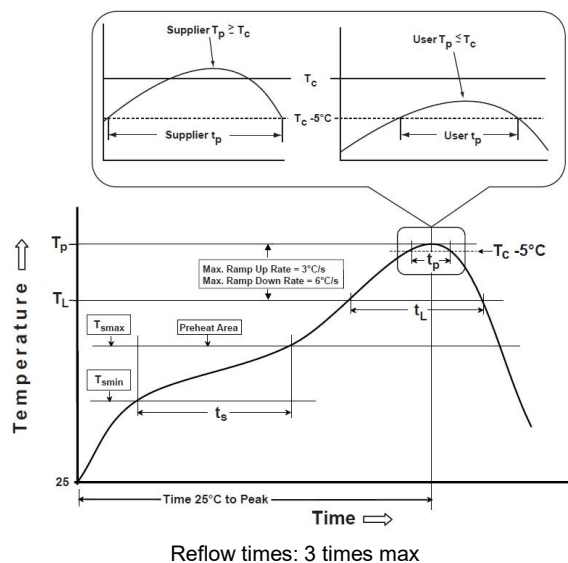


Fig.2 Iron Reflow

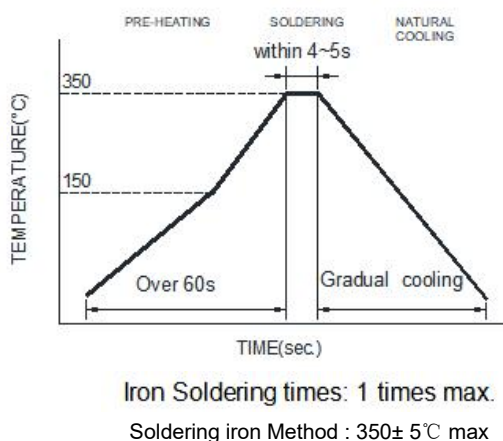


Table (1.1): Reflow Profiles

Profile Type:	Pb-Free Assembly
Preheat	
-Temperature Min(T_{smin})	150°C
-Temperature Max(T_{smax})	200°C
-Time(t_s)from(T_{smin} to T_{smax})	60-120seconds
Ramp-up rate(T_L to T_p)	3°C/second max.
Liquidus temperature(T_L)	217°C
Time(t_L)maintained above T_L	60-150 seconds
Classification temperature(T_c)	See Table (1.2)
Time(t_p) at $T_c - 5^\circ\text{C}$ (T_p should be equal to or less than T_c .)	< 30 seconds
Ramp-down rate(T_p to T_L)	6°C /second max.
Time 25°C to peak temperature	8 minutes max.

T_p : maximum peak package body temperature, T_c : the classification temperature.
For user (customer) T_p should be equal to or less than T_c .

Table (1.2) Package Thickness/Volume and Classification Temperature (T_c)

	Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
PB-Free Assembly	<1.6mm	260°C	260°C	260°C
	1.6-2.5mm	260°C	250°C	245°C
	$\geq 2.5\text{mm}$	250°C	245°C	245°C

Reflow is referred to standard IPC/JEDEC J-STD-020E ◦

9. Notes

- (1) When there are questions concerning measurement result : measurement shall be made after 48 ± 2 hours of recovery under the standard condition
- (2) This power choke coil itself does not have any protective function in abnormal condition such as overload, short-circuit and open-circuit conditions, etc. Therefore, it shall be confirmed as the end product that there is no risk of smoking, fire, dielectric withstand voltage, insulation resistance, etc. in abnormal conditions to provide protective devices and/or protection circuit in the end product.
- (3) When this power choke coil was used in a similar or new product to the original one, sometimes it might not be able to satisfy the specifications due to different condition of use.
- (4) Dielectric withstanding test with higher voltage than specific value will damage insulating material and shorten its life.
- (5) This power choke coil must not be used in wet condition by water, coffee or any liquid because insulation strength becomes very low in this condition.
- (6) Please consult our company to confirm the reliability of the process required to wash or use or exposure to a chemical solvent used in this product. PCB washing tested to MIL-STD-202 Method 1 and dry it off immediately .
- (7) The rated current as listed is either the saturation current or the heating current depending on which value is lower.
- (8) If this power choke is dipped in the cleaning agent, such as toluene, xylene, ketone, and ether system, there is a possibility that the performance decreases greatly, and marking disappears.
- (9) The high power ultrasonic washing may damage the choke body .
- (10) Before use, the user should determine whether this product is suitable for their own design. Our company only guarantees that the product meets the requirements of this specification .

Application Notice

• Storage Conditions

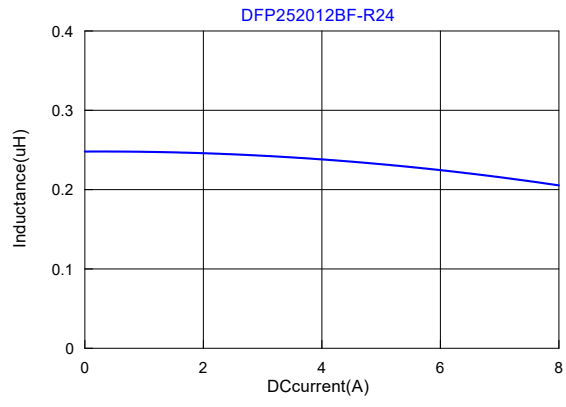
To maintain the solderability of terminal electrodes:

1. TAI-TECH products meet IPC/JEDEC J-STD-020E standard-MSL, level 1.
2. Temperature and humidity conditions: Less than 40°C and 60% RH.
3. Recommended products should be used within 12 months from the time of delivery.
4. The packaging material should be kept where no chlorine or sulfur exists in the air.

• Transportation

1. Products should be handled with care to avoid damage or contamination from perspiration and skin oils.
2. The use of tweezers or vacuum pick up is strongly recommended for individual components.
3. Bulk handling should ensure that abrasion and mechanical shock are minimized.

10. Typical Performance Curves



11 Appearance criterion

11-1 Core chipping

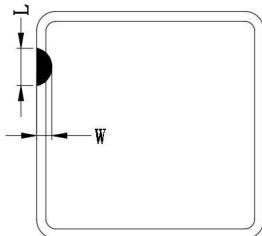
The appearance standard of the chipping size on top side, and bottom side ferrite core is listed below.

Chip off is generated during molding and manufacturing process.

Chip off acceptance limits subjected to the product size.

Our current Defect limit is based on the IPC-A-610.

Some chip off does not impact the product function, see the IPC standard 1 & 2.

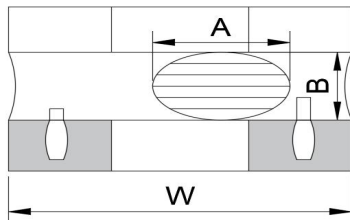


L	≤50 % of the length
W	≤25 % of the width

Defects usually occur at the corners and edges of the product, There will be a slight defect black and rough, but not exposed copper, and does not affect the product performance and reliability.

11-2 Void appearance tolerance Limit

Size of voids occurring to coating resin is specified below.



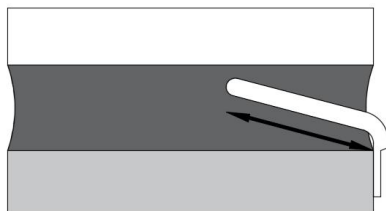
Exposed wire tolerance limit of coating resin part on product side.

Size of exposed wire occurring to coating resin is specified below.

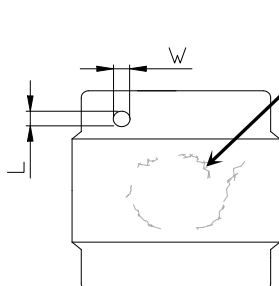
1. Width direction (dimension a) : Acceptable when $a \leq w/2$.
2. Length direction (dimension b) : Dimension b is not specified.
3. The total area of exposed wire occurring to each sides is not greater than 50% of coating resin area, and is acceptable.

11-3 External appearance criterion for exposed wire


Exposed winding wire at the secondary side is regarded as qualified product.




11-4 Electrode appearance criterion for exposed wire



Visual check on core surface with no crack means pass.


 Only top side of wire is exposed.
 (regardless of whole top side of wire exposed)

Conforming


 Wire is soldered insufficiently and less than half of outer diameter is covered with solder.
 Less than 1/2 of joint side length.
 (More than 1/2 is selected as defect)

L&w
≤20% of the area on one single pad

Foreign materials on the product body is inevitable and accepted.

Electrodes with foreign body (dirt) appearance standards

Foreign materials (dirt) will not affect the coplanarity of PAD,

below the example of foreign materials (dirt) quantity ≤2PCS on single PAD.

Dimensions range as shown in the table.

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