

- ♦ Polarity: Color band denotes cathode
- ♦ High temperature soldering guaranteed: 260°C/10 seconds/.375",(9.5mm) lead lengths at 5 lbs., (2.3kg) tension
- ♦ Weight: 1.2 grams

#### .....

# Maximum Ratings and Electrical Characteristics

Rating at 25  $^{\circ}$ C ambient temperature unless otherwise specified. Single phase, half wave, 60 Hz, resistive or inductive load. For capacitive load, derate current by 20%

Type Number	Symbol	SF 31	SF 32	SF 33	SF 34	SF 35	SF 36	SF 37	SF 38	Units
Maximum Recurrent Peak Reverse Voltage	V <sub>RRM</sub>	50	100	150	200	300	400	500	600	V
Maximum RMS Voltage	V <sub>RMS</sub>	35	70	105	140	210	280	350	420	V
Maximum DC Blocking Voltage	V <sub>DC</sub>	50	100	150	200	300	400	500	600	V
Maximum Average Forward Rectified Current .375 (9.5mm) Lead Length $@T_A = 55^{\circ}C$	I <sub>F(AV)</sub>	3								A
Peak Forward Surge Current, 8.3 ms Single Half Sine- wave Superimposed on Rated Load (JEDEC method)	I <sub>FSM</sub>	125								А
Maximum Instantaneous Forward Voltage (Note 1) @ 3 A	V <sub>F</sub>	0.95				1.3		1	.7	V
Maximum DC Reverse Current at Rated@ T $_A$ =25 °CDC Blocking Voltage@ T $_A$ =125 °C	I <sub>R</sub>	5 100								uA uA
Maximum Reverse Recovery Time (Note 2)	Trr	35								nS
Typical Junction Capacitance (Note 3)	Cj	80					70			
Typical Thermal Resistance (Note 4)	R <sub>θJA</sub>	35								°C/W
Operating Temperature Range	TJ	- 65 to + 125								°C
Storage Temperature Range	T <sub>STG</sub>	- 65 to + 150								°C

Note 1: Pulse Test with PW=300 usec, 1% Duty Cycle

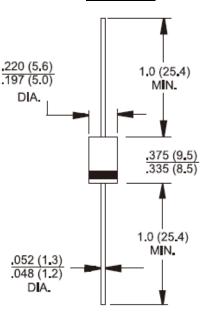
Note 2: Reverse Recovery Test Conditions: I<sub>F</sub>=0.5A, I<sub>R</sub>=1.0A, I<sub>RR</sub>=0.25A

Note 3: Measured at 1 MHz and Applied Reverse Voltage of 4.0V D.C.

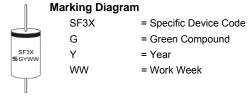
Note 4: Mount on Cu-Pad Size 16mm x 16mm on PCB.

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# SF31 - SF38 3.0AMPS. Super Fast Rectifiers DO-201AD

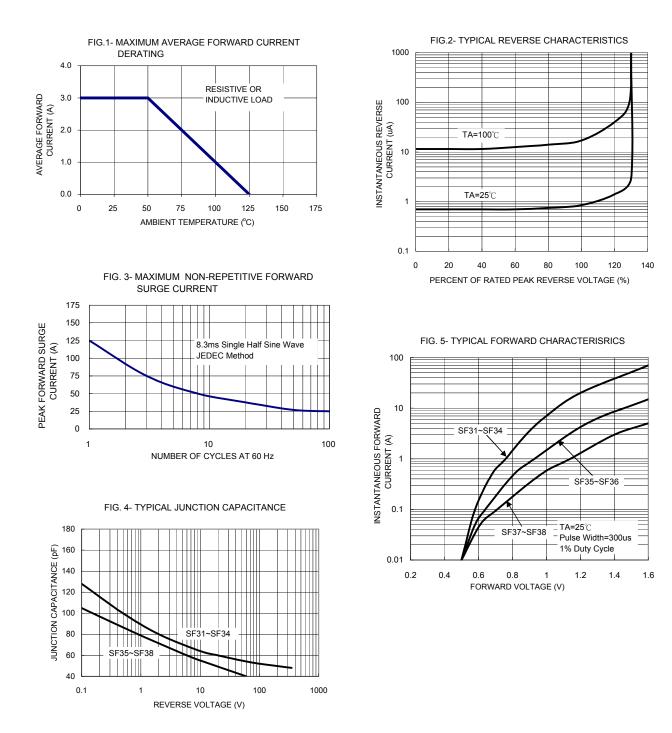


## Dimensions in inches and (millimeters)

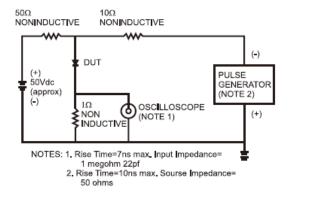


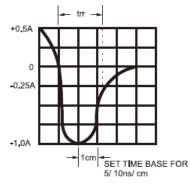


### RATINGS AND CHARACTERISTIC CURVES (SF31 THRU SF38)



#### FIG.6- REVERSE RECOVERY TIME CHARACTERISTIC AND TEST CIRCUIT DIAGRAM





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