

AUTOMOTIVE Dual N-Channel 40V 175°C MOSFET

FEATURES

- AEC-Q101 Rev-D Qualified
- 100% UIS and R_g tested
- 175°C Operating Junction Temperature
- RoHS Compliant
- Halogen-free according to IEC 61249-2-21

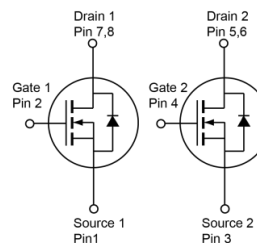
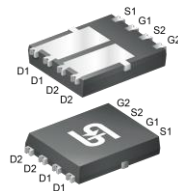
APPLICATIONS

- Power Switch for 12V Automotive Systems
- Solenoid and Motor Control
- Automotive Transmission Control
- DC-DC Converters

PRODUCT SUMMARY		
PARAMETER	VALUE	UNIT
V _{DS}	40	V
R _{DS(on)} (max)	V _{GS} = 10V	15
	V _{GS} = 7V	28.6
Q _g	18	nC



PDFN56U Dual



Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T _A = 25°C unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V _{DS}	40	V
Gate-Source Voltage	V _{GS}	±20	V
Continuous Drain Current (Note 1)	I _D	T _C = 25°C	39
		T _A = 25°C	9
Pulsed Drain Current	I _{DM}	156	A
Single Pulse Avalanche Current (Note 2)	I _{AS}	15	A
Single Pulse Avalanche Energy (Note 2)	E _{AS}	34	mJ
Total Power Dissipation	P _D	T _C = 25°C	48
		T _C = 125°C	16
Total Power Dissipation	P _D	T _A = 25°C	2.4
		T _A = 125°C	0.8
Operating Junction and Storage Temperature Range	T _J , T _{STG}	- 55 to +175	°C

THERMAL RESISTANCE			
PARAMETER	SYMBOL	MAXIMUM	UNIT
Thermal Resistance – Junction to Case	R _{θJC}	3.1	°C/W
Thermal Resistance – Junction to Ambient	R _{θJA}	61	°C/W

Thermal Performance Note: R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design. The R_{θJA} limit presented here is based on mounting on a 1 in² pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$	BV_{DSS}	40	--	--	V
Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	$V_{GS(TH)}$	1.8	2.8	4	V
Gate-Source Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$	I_{GSS}	--	--	± 100	nA
Drain-Source Leakage Current	$V_{GS} = 0\text{V}, V_{DS} = 40\text{V}$	I_{DSS}	--	--	1	μA
	$V_{GS} = 0\text{V}, V_{DS} = 40\text{V}$ $T_J = 125^\circ\text{C}$		--	--	100	
	$V_{GS} = 0\text{V}, V_{DS} = 40\text{V}$ $T_J = 175^\circ\text{C}$		--	--	500	
Drain-Source On-State Resistance (Note 3)	$V_{GS} = 10\text{V}, I_D = 9\text{A}$	$R_{DS(on)}$	--	10.3	15	m Ω
	$V_{GS} = 10\text{V}, I_D = 9\text{A}$ $T_J = 125^\circ\text{C}$		--	17.5	25.5	
	$V_{GS} = 10\text{V}, I_D = 9\text{A}$ $T_J = 175^\circ\text{C}$		--	21.6	31.5	
	$V_{GS} = 7\text{V}, I_D = 6\text{A}$		--	11.6	28.6	
Forward Transconductance (Note 3)	$V_{DS} = 10\text{V}, I_D = 9\text{A}$	g_{fs}	--	38	--	S
Dynamic (Note 4)						
Total Gate Charge	$V_{GS} = 10\text{V}, V_{DS} = 20\text{V},$ $I_D = 9\text{A}$	Q_g	--	18	--	nC
Total Gate Charge	$V_{GS} = 7\text{V}, V_{DS} = 20\text{V},$ $I_D = 6\text{A}$	Q_g	--	13	--	
Gate-Source Charge		Q_{gs}	--	6	--	
Gate-Drain Charge		Q_{gd}	--	4	--	
Input Capacitance	$V_{GS} = 0\text{V}, V_{DS} = 20\text{V},$ $f = 1.0\text{MHz}$	C_{iss}	--	1135	--	pF
Output Capacitance		C_{oss}	--	112	--	
Reverse Transfer Capacitance		C_{rss}	--	52	--	
Gate Resistance	$f = 1.0\text{MHz}$	R_g	0.8	2.5	5	Ω
Switching (Note 4)						
Turn-On Delay Time	$V_{GS} = 10\text{V}, V_{DS} = 20\text{V},$ $I_D = 9\text{A}, R_G = 2\Omega$	$t_{d(on)}$	--	7	--	ns
Rise Time		t_r	--	8	--	
Turn-Off Delay Time		$t_{d(off)}$	--	13	--	
Fall Time		t_f	--	4	--	
Source-Drain Diode						
Diode Forward Voltage (Note 3)	$V_{GS} = 0\text{V}, I_S = 9\text{A}$	V_{SD}	--	--	1.2	V
Reverse Recovery Time	$I_S = 9\text{A},$ $di/dt = 100\text{A}/\mu\text{s}$	t_{rr}	--	14	--	ns
Reverse Recovery Charge		Q_{rr}	--	7	--	nC

Notes:

- Silicon limited current only.
- $L = 0.3\text{mH}, V_{GS} = 10\text{V}, V_{DD} = 25\text{V}, R_G = 50\Omega, I_{AS} = 15\text{A},$ Starting $T_J = 25^\circ\text{C}$
- Pulse test: Pulse Width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
- Switching time is essentially independent of operating temperature.

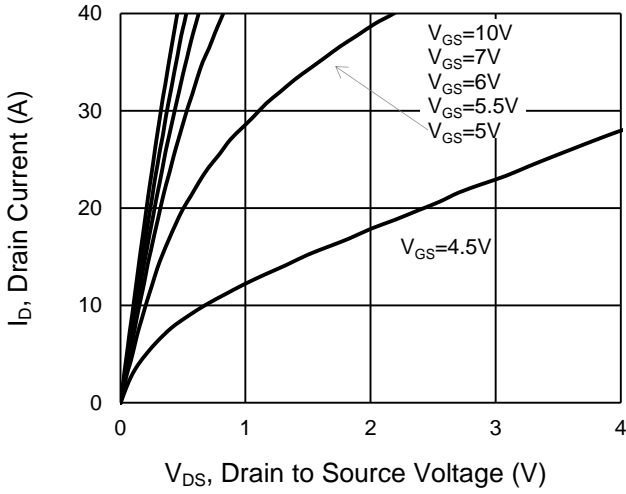
ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TQM150NB04DCR RLG	PDFN56U Dual	2,500pcs / 13" Reel

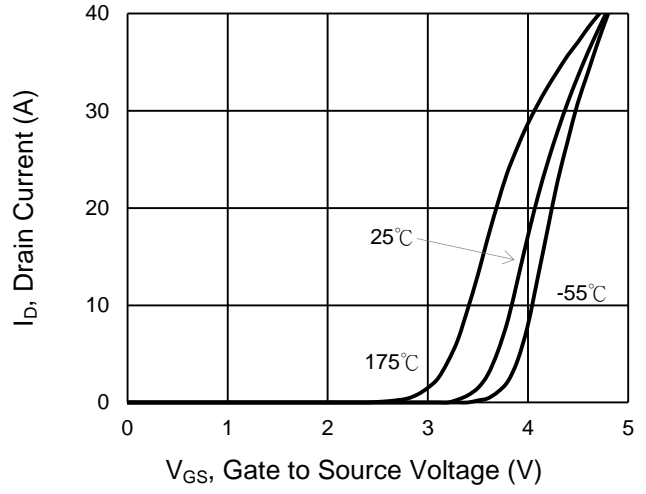
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

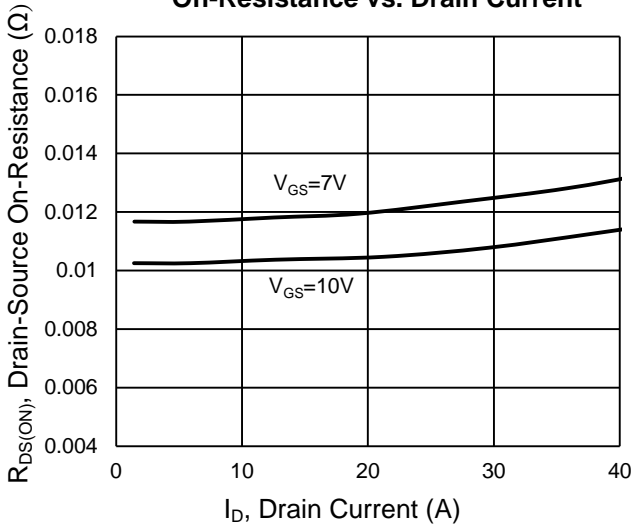
Output Characteristics



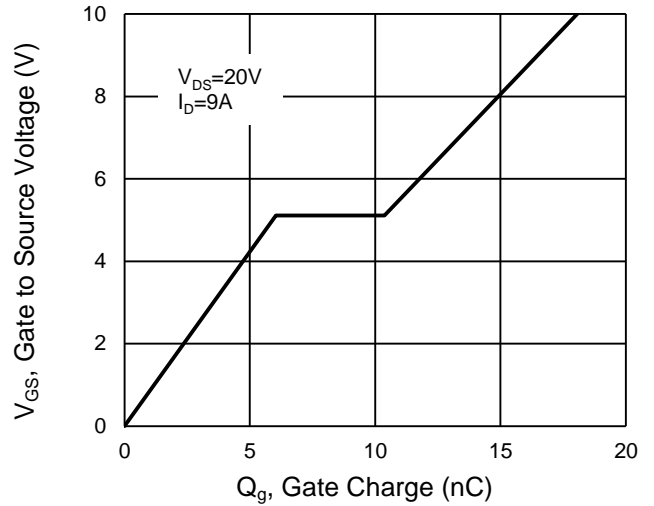
Transfer Characteristics



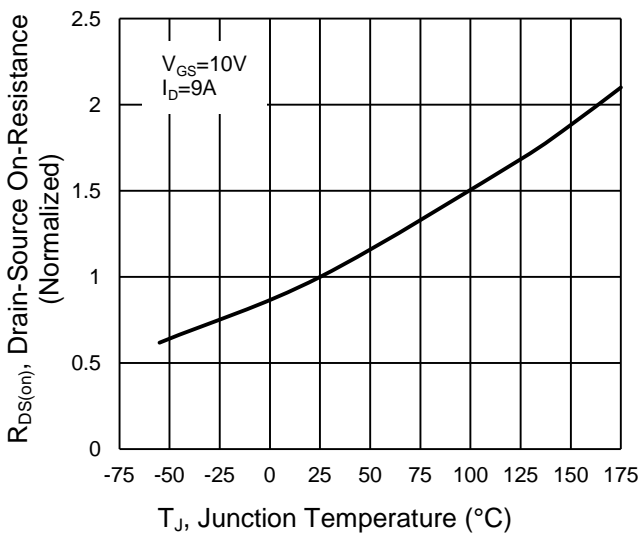
On-Resistance vs. Drain Current



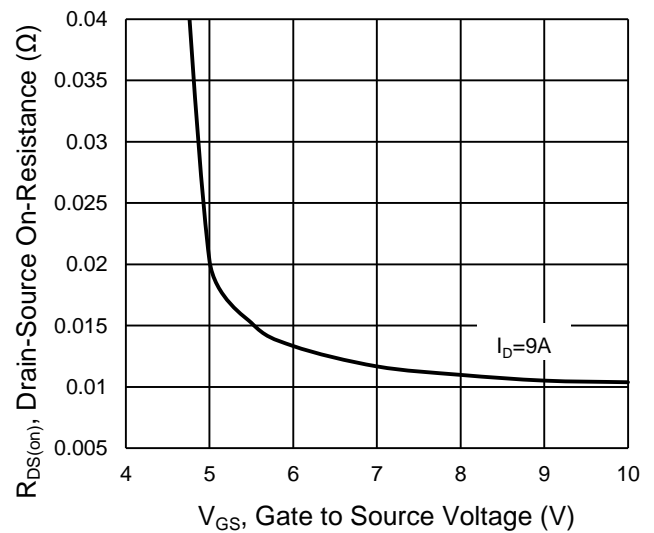
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



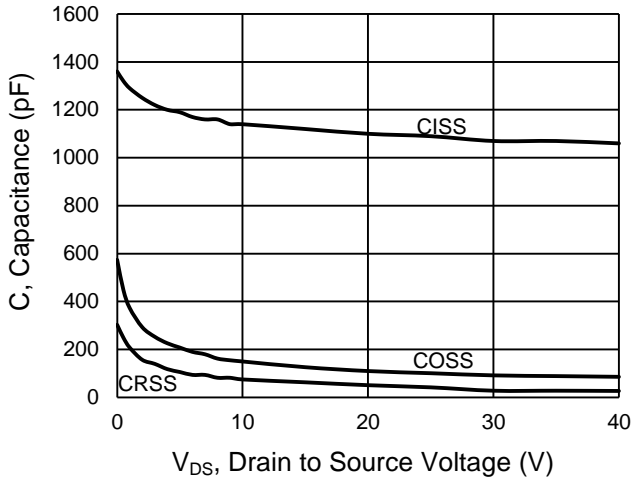
On-Resistance vs. Gate-Source Voltage



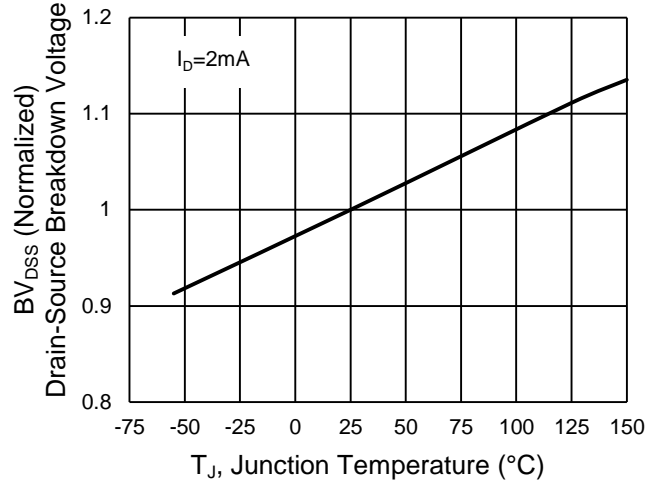
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

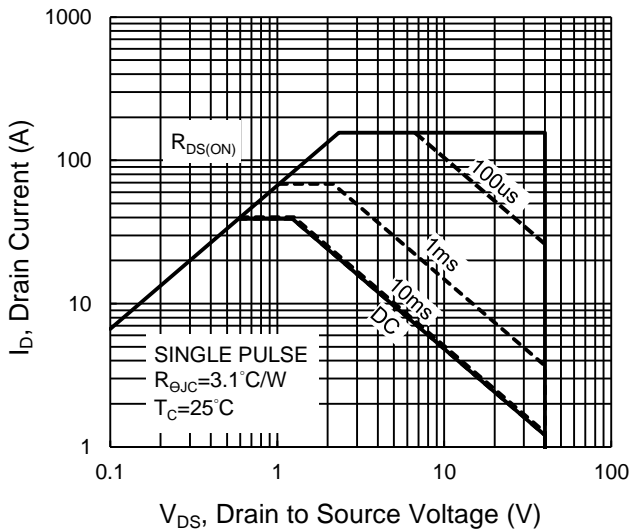
Capacitance vs. Drain-Source Voltage



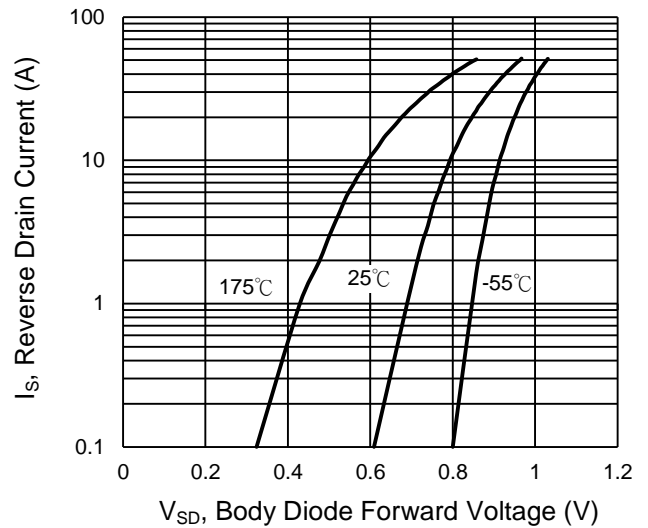
BV_{DSS} vs. Junction Temperature



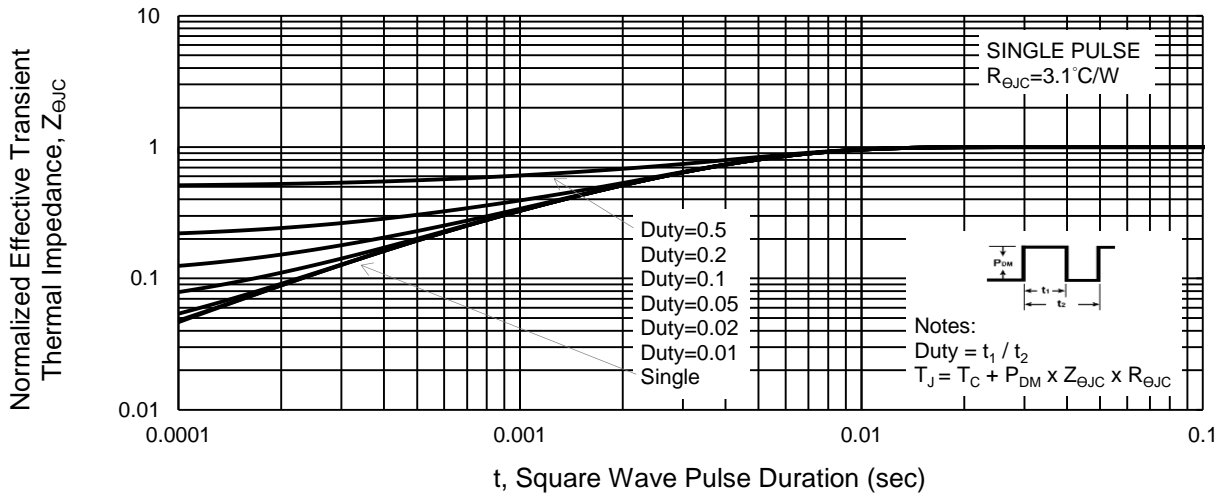
Maximum Safe Operating Area, Junction-to-Case



Source-Drain Diode Forward Current vs. Voltage

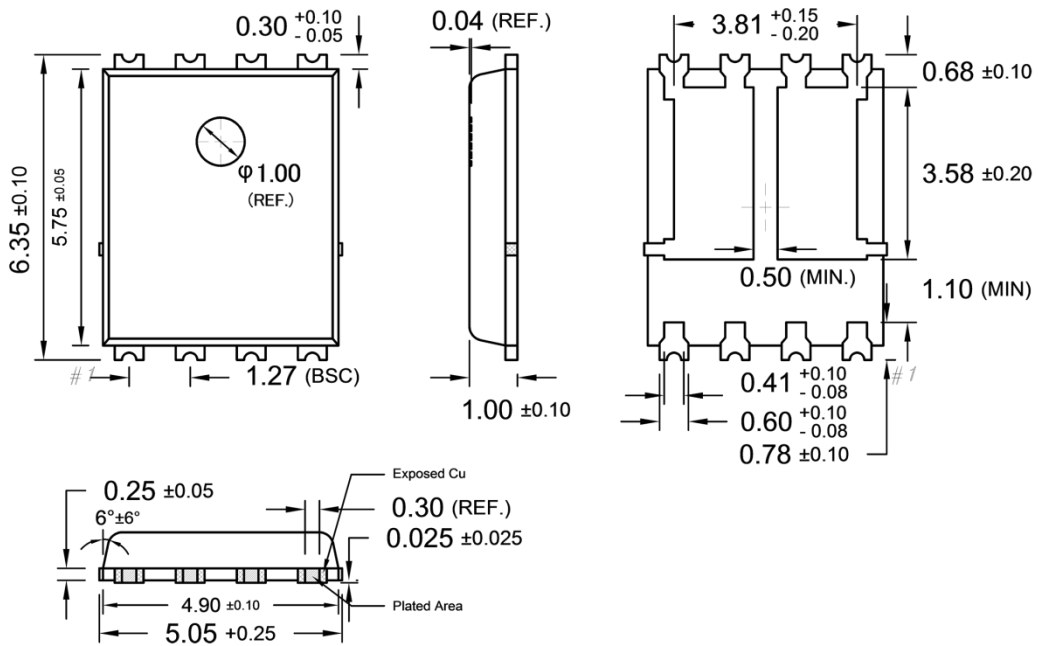


Normalized Thermal Transient Impedance, Junction-to-Case

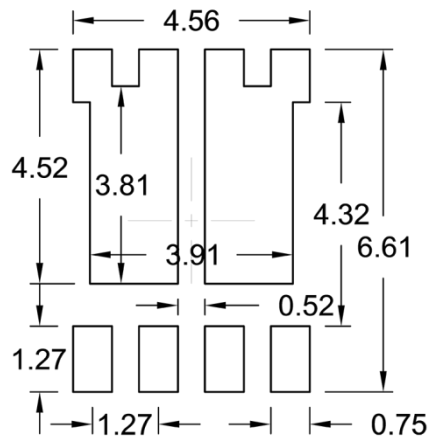


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

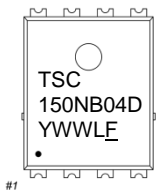
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SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



- Y** = Year Code
- WW** = Week Code (01~52)
- L** = Lot Code (1~9,A~Z)
- F** = Factory Code
- = AEC-Q101 Qualified

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