

## P-Channel Power MOSFET

-30V, -34A, 8.5mΩ

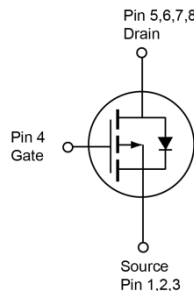
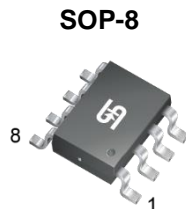
### FEATURES

- Low  $R_{DS(on)}$  to minimize conductive losses
- Low gate charge for fast power switching
- 100% UIS and  $R_g$  tested
- Compliant to RoHS directive 2011/65/EU and in accordance to WEEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21

### APPLICATIONS

- DC-DC Converters
- Battery Power Management
- Load Switch
- BLDC Motor Drives

KEY PERFORMANCE PARAMETERS		
PARAMETER	VALUE	UNIT
$V_{DS}$	-30	V
$R_{DS(on)}$ (max)	$V_{GS} = -10V$	8.5
	$V_{GS} = -4.5V$	14
$Q_g$	28	nC



Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	-30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current (Note 1)	$I_D$	$T_C = 25^\circ\text{C}$	-34
		$T_A = 25^\circ\text{C}$	-13
Pulsed Drain Current	$I_{DM}$	-136	A
Single Pulse Avalanche Current (Note 2)	$I_{AS}$	-23	A
Single Pulse Avalanche Energy (Note 2)	$E_{AS}$	79	mJ
Total Power Dissipation	$P_D$	$T_C = 25^\circ\text{C}$	14
		$T_C = 125^\circ\text{C}$	2.8
Total Power Dissipation	$P_D$	$T_A = 25^\circ\text{C}$	2.2
		$T_A = 125^\circ\text{C}$	0.4
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	- 55 to +150	$^\circ\text{C}$

THERMAL PERFORMANCE			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	9	$^\circ\text{C/W}$
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	57	$^\circ\text{C/W}$

**Thermal Performance Note:**  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins.  $R_{\theta JA}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.

<b>ELECTRICAL SPECIFICATIONS</b> ( $T_A = 25^\circ\text{C}$ unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = -250\mu A$	$BV_{DSS}$	-30	--	--	V
Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250\mu A$	$V_{GS(TH)}$	-1.2	-1.5	-2.5	V
Gate-Source Leakage Current	$V_{GS} = \pm 20V, V_{DS} = 0V$	$I_{GSS}$	--	--	$\pm 100$	nA
Drain-Source Leakage Current	$V_{GS} = 0V, V_{DS} = -30V$	$I_{DSS}$	--	--	-1	$\mu A$
	$V_{GS} = 0V, V_{DS} = -30V$ $T_J = 125^\circ\text{C}$		--	--	-100	
Drain-Source On-State Resistance (Note 3)	$V_{GS} = -10V, I_D = -13A$	$R_{DS(on)}$	--	7.7	8.5	m $\Omega$
	$V_{GS} = -4.5V, I_D = -10A$		--	11	14	
Forward Transconductance (Note 3)	$V_{DS} = -5V, I_D = -13A$	$g_{fs}$	--	35	--	S
<b>Dynamic</b> (Note 4)						
Total Gate Charge	$V_{GS} = -10V,$ $V_{DS} = -15V, I_D = -13A$	$Q_g$	--	56	--	nC
Total Gate Charge	$V_{GS} = -4.5V,$ $V_{DS} = -15V, I_D = -10A$	$Q_g$	--	28	--	
Gate-Source Charge		$Q_{gs}$	--	9	--	
Gate-Drain Charge		$Q_{gd}$	--	11	--	
Input Capacitance	$V_{GS} = 0V, V_{DS} = -15V$ $f = 1.0\text{MHz}$	$C_{iss}$	--	3216	--	pF
Output Capacitance		$C_{oss}$	--	409	--	
Reverse Transfer Capacitance		$C_{rss}$	--	277	--	
Gate Resistance	$f = 1.0\text{MHz}$	$R_g$	1.8	6	12	$\Omega$
<b>Switching</b> (Note 4)						
Turn-On Delay Time	$V_{GS} = -10V, V_{DS} = -15V,$ $I_D = -13A, R_G = 2\Omega$	$t_{d(on)}$	--	7.2	--	ns
Turn-On Rise Time		$t_r$	--	2.6	--	
Turn-Off Delay Time		$t_{d(off)}$	--	68	--	
Turn-Off Fall Time		$t_f$	--	33	--	
<b>Source-Drain Diode</b>						
Forward Voltage (Note 3)	$V_{GS} = 0V, I_S = -13A$	$V_{SD}$	--	--	-1	V
Reverse Recovery Time	$I_S = -13A,$ $di/dt = 100A/\mu s$	$t_{rr}$	--	34	--	ns
Reverse Recovery Charge		$Q_{rr}$	--	19	--	nC

**Notes:**

- Silicon limited current only.
- $L = 0.3\text{mH}, V_{GS} = -10V, V_{DD} = -25V, R_G = 25\Omega, I_{AS} = -23A,$  Starting  $T_J = 25^\circ\text{C}$
- Pulse test: Pulse Width  $\leq 300\mu s,$  duty cycle  $\leq 2\%$ .
- Switching time is essentially independent of operating temperature.

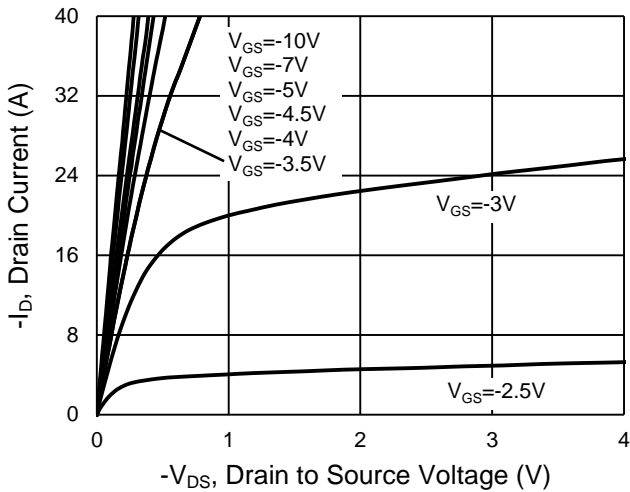
**ORDERING INFORMATION**

PART NO.	PACKAGE	PACKING
TSM085P03CS RLG	SOP-8	2,500pcs / 13" Reel

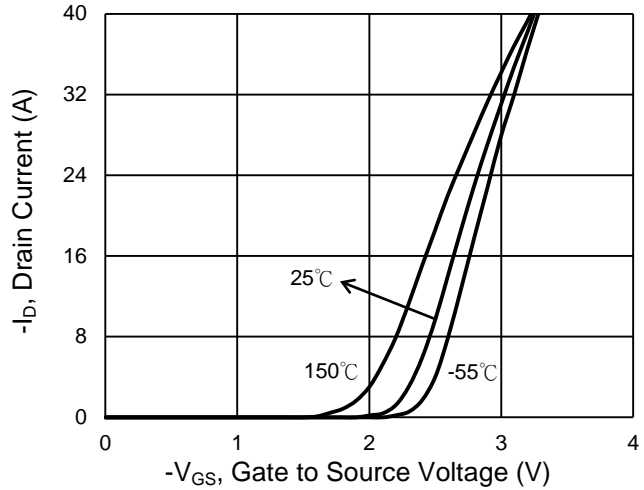
**CHARACTERISTICS CURVES**

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

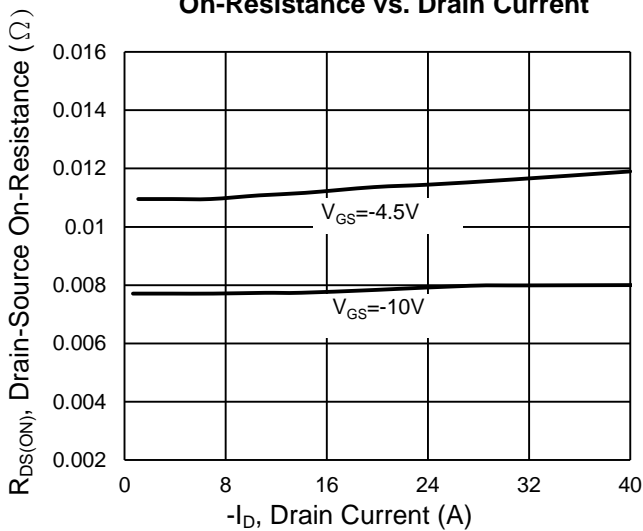
**Output Characteristics**



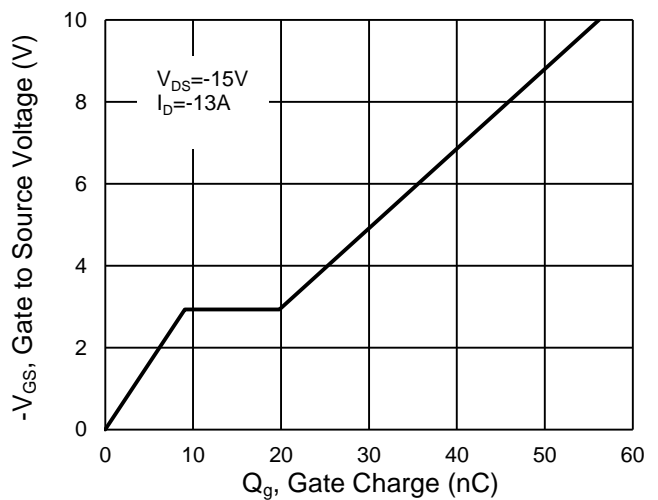
**Transfer Characteristics**



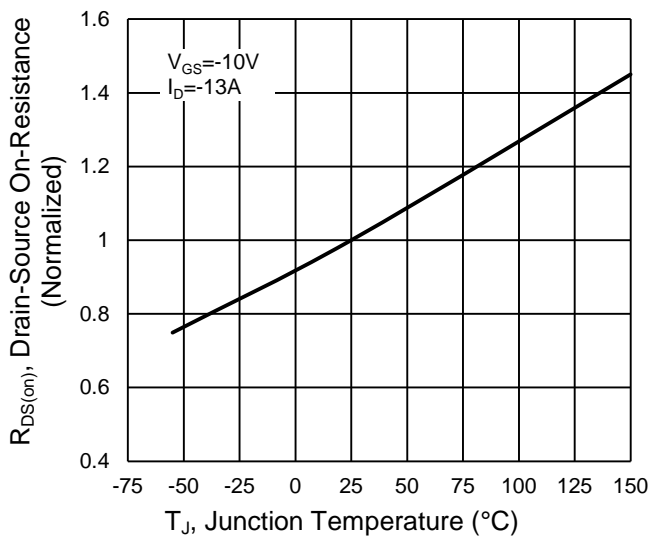
**On-Resistance vs. Drain Current**



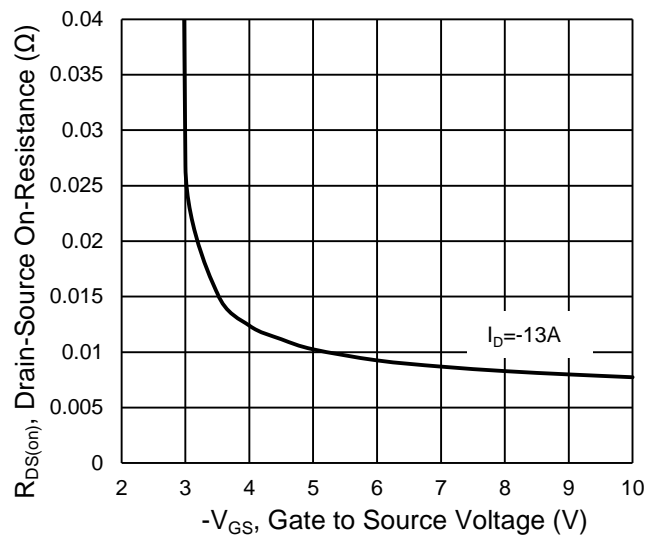
**Gate-Source Voltage vs. Gate Charge**



**On-Resistance vs. Junction Temperature**



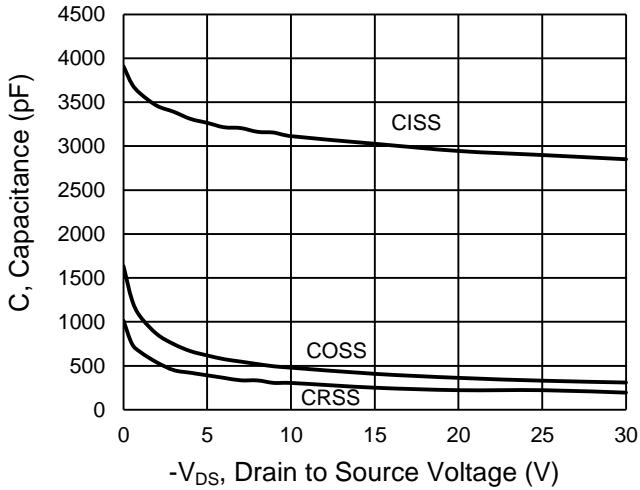
**On-Resistance vs. Gate-Source Voltage**



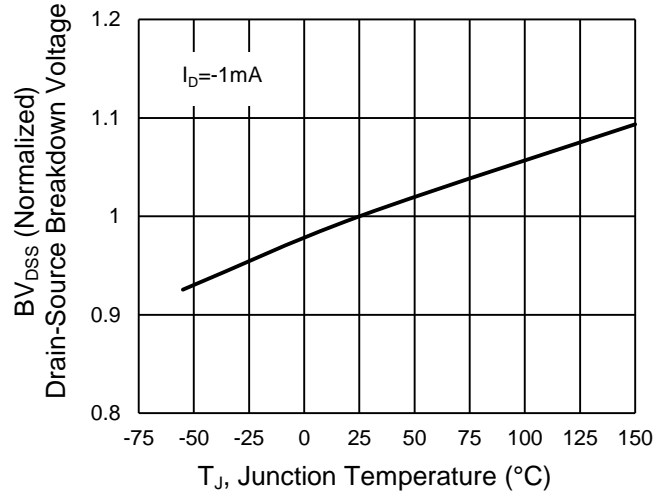
**CHARACTERISTICS CURVES**

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

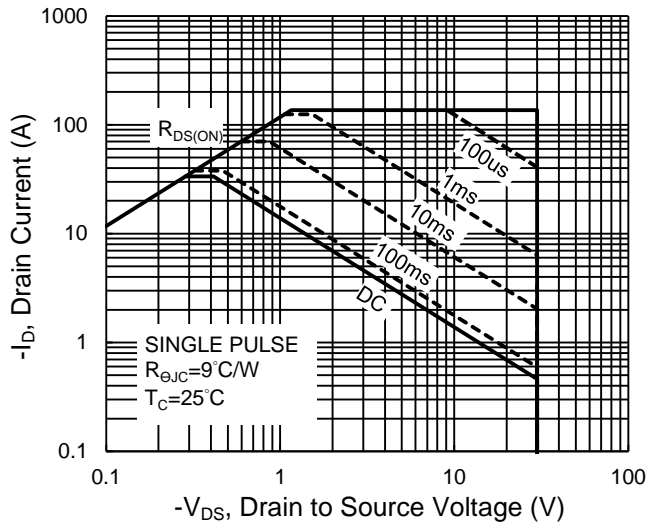
**Capacitance vs. Drain-Source Voltage**



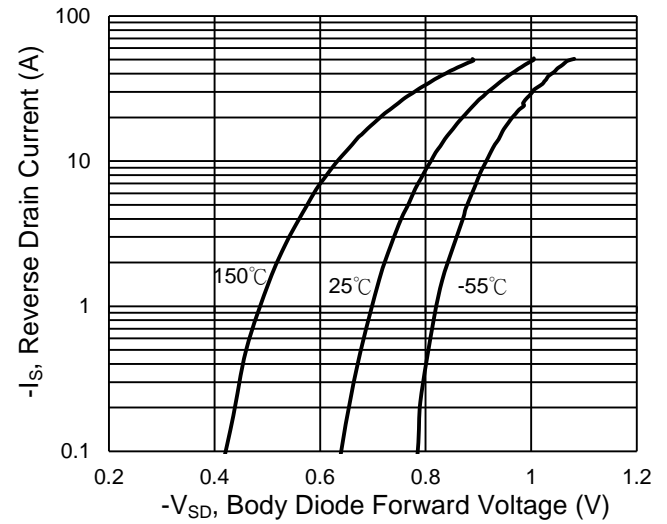
**$BV_{DSS}$  vs. Junction Temperature**



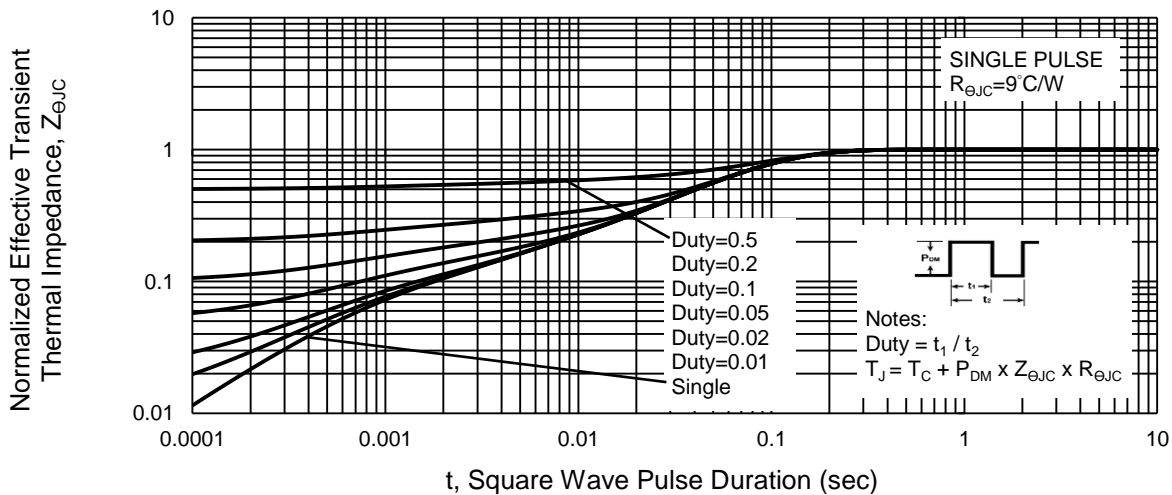
**Maximum Safe Operating Area, Junction-to-Case**



**Source-Drain Diode Forward Current vs. Voltage**

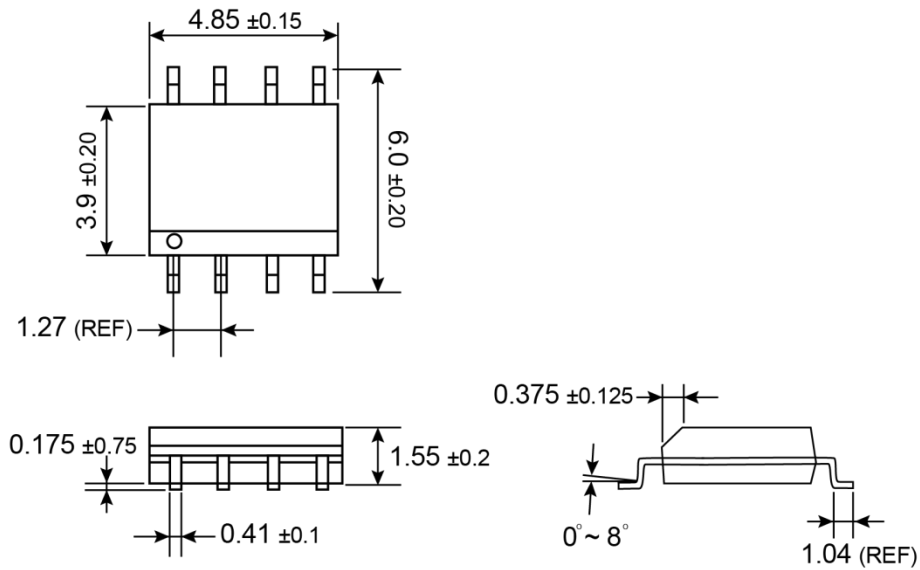


**Normalized Thermal Transient Impedance, Junction-to-Case**

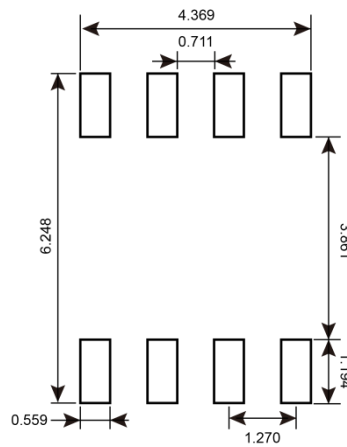


**PACKAGE OUTLINE DIMENSIONS** (Unit: Millimeters)

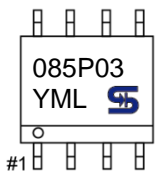
**SOP-8**



**SUGGESTED PAD LAYOUT** (Unit: Millimeters)



**MARKING DIAGRAM**



- Y = Year Code
- M = Month Code
- |        |        |        |        |
|--------|--------|--------|--------|
| O =Jan | P =Feb | Q =Mar | R =Apr |
| S =May | T =Jun | U =Jul | V =Aug |
| W =Sep | X =Oct | Y =Nov | Z =Dec |
- L = Lot Code (1~9, A~Z)

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