

## Dual N-Channel Power MOSFET

40V, 48A, 11mΩ

### FEATURES

- Low  $R_{DS(ON)}$  to minimize conductive losses
- Low gate charge for fast power switching
- 100% UIS and  $R_g$  tested
- RoHS Compliant
- Halogen-free according to IEC 61249-2-21

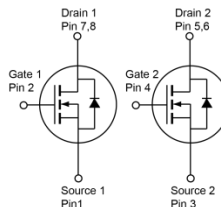
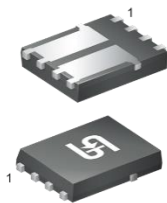
### APPLICATIONS

- BLDC Motor Control
- Battery Power Management
- DC-DC Converter
- Secondary Synchronous Rectification

KEY PERFORMANCE PARAMETERS		
PARAMETER	VALUE	UNIT
$V_{DS}$	40	V
$R_{DS(on)}$ (max)	$V_{GS} = 10V$	11
	$V_{GS} = 7V$	17.2
$Q_g$	25	nC



PDFN56 Dual



Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	40	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current (Note 1)	$I_D$	$T_C = 25^\circ\text{C}$	48
		$T_A = 25^\circ\text{C}$	10
Pulsed Drain Current	$I_{DM}$	192	A
Single Pulse Avalanche Current (Note 2)	$I_{AS}$	17	A
Single Pulse Avalanche Energy (Note 2)	$E_{AS}$	43	mJ
Total Power Dissipation	$P_D$	$T_C = 25^\circ\text{C}$	48
		$T_C = 125^\circ\text{C}$	9.6
Total Power Dissipation	$P_D$	$T_A = 25^\circ\text{C}$	2
		$T_A = 125^\circ\text{C}$	0.4
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	- 55 to +150	$^\circ\text{C}$

### THERMAL PERFORMANCE

PARAMETER	SYMBOL	MAXIMUM	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	2.6	$^\circ\text{C/W}$
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	61	$^\circ\text{C/W}$

**Thermal Performance Note:**  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design. The  $R_{\theta JA}$  limit presented here is based on mounting on a 1 in<sup>2</sup> pad of 2 oz copper.

<b>ELECTRICAL SPECIFICATIONS</b> ( $T_A = 25^\circ\text{C}$ unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$	$BV_{DSS}$	40	--	--	V
Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	$V_{GS(TH)}$	2	2.9	4	V
Gate-Source Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$	$I_{GSS}$	--	--	$\pm 100$	nA
Drain-Source Leakage Current	$V_{GS} = 0\text{V}, V_{DS} = 40\text{V}$	$I_{DSS}$	--	--	1	$\mu\text{A}$
	$V_{GS} = 0\text{V}, V_{DS} = 40\text{V}$ $T_J = 125^\circ\text{C}$		--	--	100	
Drain-Source On-State Resistance (Note 3)	$V_{GS} = 10\text{V}, I_D = 10\text{A}$	$R_{DS(on)}$	--	8.5	11	m $\Omega$
	$V_{GS} = 7\text{V}, I_D = 8\text{A}$		--	10	17.2	
Forward Transconductance (Note 3)	$V_{DS} = 10\text{V}, I_D = 10\text{A}$	$g_{fs}$	--	40	--	S
<b>Dynamic</b> (Note 4)						
Total Gate Charge	$V_{GS} = 10\text{V}, V_{DS} = 20\text{V},$ $I_D = 10\text{A}$	$Q_g$	--	25	--	nC
Total Gate Charge	$V_{GS} = 7\text{V}, V_{DS} = 20\text{V},$ $I_D = 8\text{A}$	$Q_g$	--	17	--	
Gate-Source Charge		$Q_{gs}$	--	7	--	
Gate-Drain Charge		$Q_{gd}$	--	6	--	
Input Capacitance	$V_{GS} = 0\text{V}, V_{DS} = 20\text{V}$ $f = 1.0\text{MHz}$	$C_{iss}$	--	1506	--	pF
Output Capacitance		$C_{oss}$	--	144	--	
Reverse Transfer Capacitance		$C_{rss}$	--	75	--	
Gate Resistance	$f = 1.0\text{MHz}$	$R_g$	0.6	1.9	3.8	$\Omega$
<b>Switching</b> (Note 4)						
Turn-On Delay Time	$V_{GS} = 10\text{V}, V_{DS} = 20\text{V},$ $I_D = 10\text{A}, R_G = 2\Omega,$	$t_{d(on)}$	--	7	--	ns
Turn-On Rise Time		$t_r$	--	10	--	
Turn-Off Delay Time		$t_{d(off)}$	--	15	--	
Turn-Off Fall Time		$t_f$	--	5	--	
<b>Source-Drain Diode</b>						
Forward Voltage (Note 3)	$V_{GS} = 0\text{V}, I_S = 10\text{A}$	$V_{SD}$	--	--	1.2	V
Reverse Recovery Time	$I_S = 10\text{A},$ $di/dt = 100\text{A}/\mu\text{s}$	$t_{rr}$	--	15	--	ns
Reverse Recovery Charge		$Q_{rr}$	--	8	--	nC

**Notes:**

1. Silicon limited current only.
2.  $L = 0.3\text{mH}, V_{GS} = 10\text{V}, V_{DD} = 25\text{V}, R_G = 25\Omega, I_{AS} = 17\text{A},$  Starting  $T_J = 25^\circ\text{C}$
3. Pulse test: Pulse Width  $\leq 300\mu\text{s}$ , duty cycle  $\leq 2\%$ .
4. Switching time is essentially independent of operating temperature.

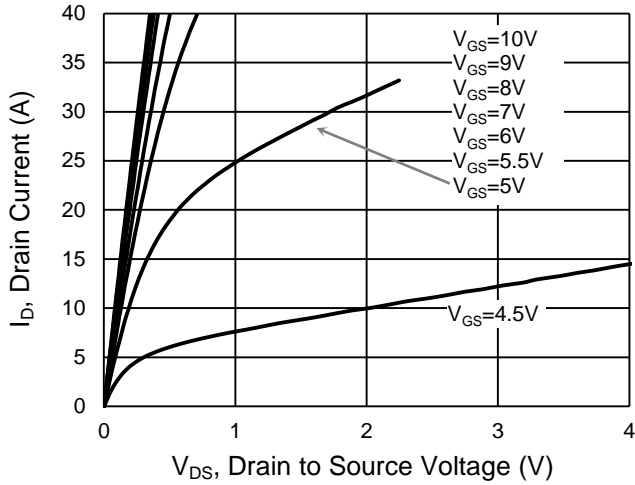
**ORDERING INFORMATION**

ORDERING CODE	PACKAGE	PACKING
TSM110NB04DCR RLG	PDFN56 Dual	2,500pcs / 13" Reel

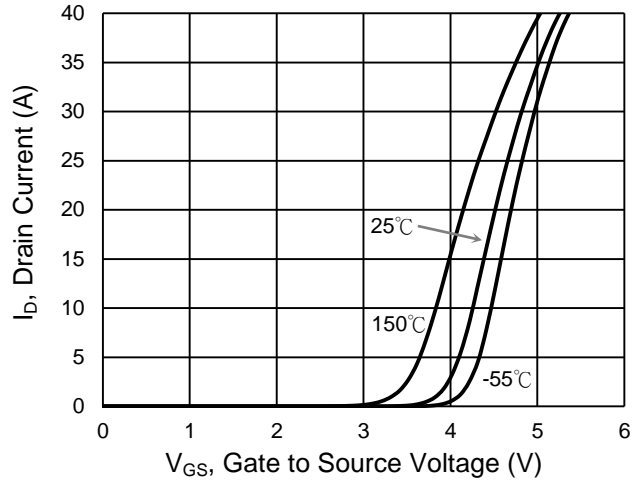
**CHARACTERISTICS CURVES**

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

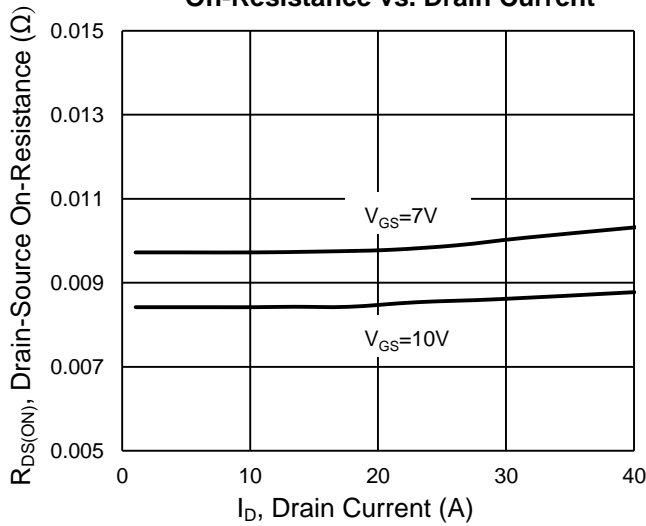
**Output Characteristics**



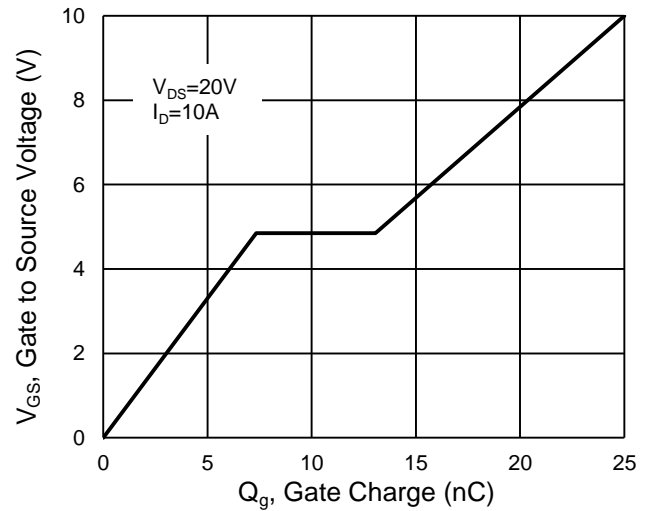
**Transfer Characteristics**



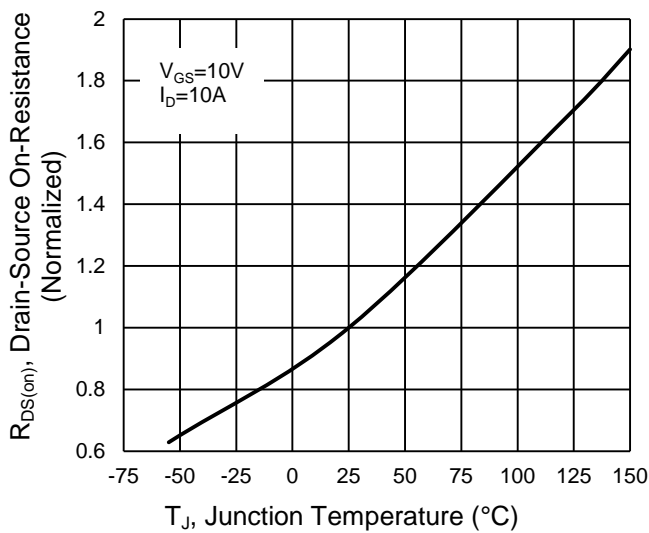
**On-Resistance vs. Drain Current**



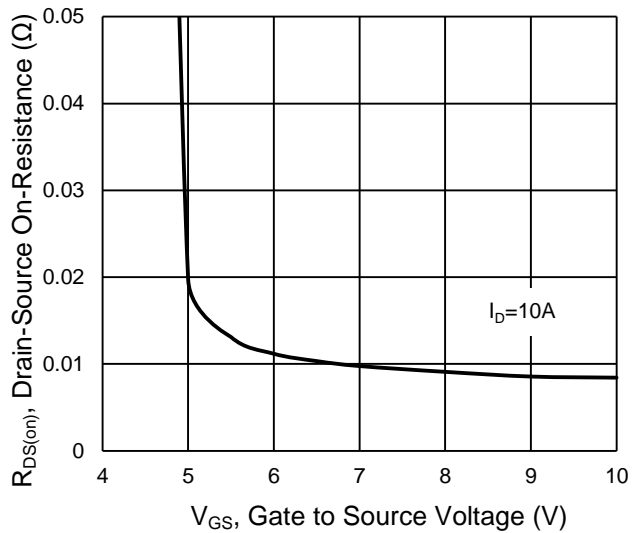
**Gate-Source Voltage vs. Gate Charge**



**On-Resistance vs. Junction Temperature**



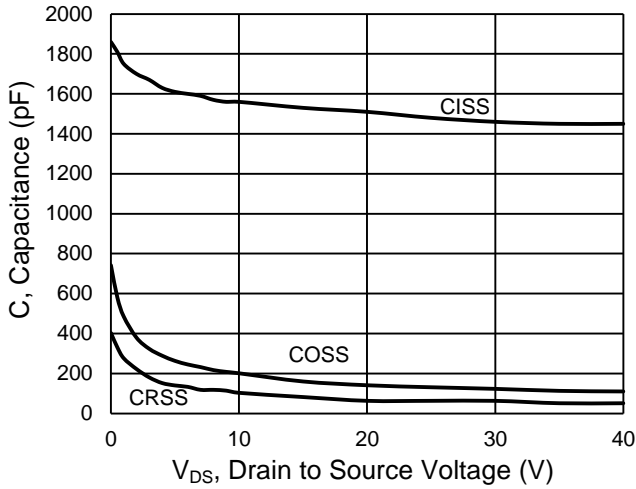
**On-Resistance vs. Gate-Source Voltage**



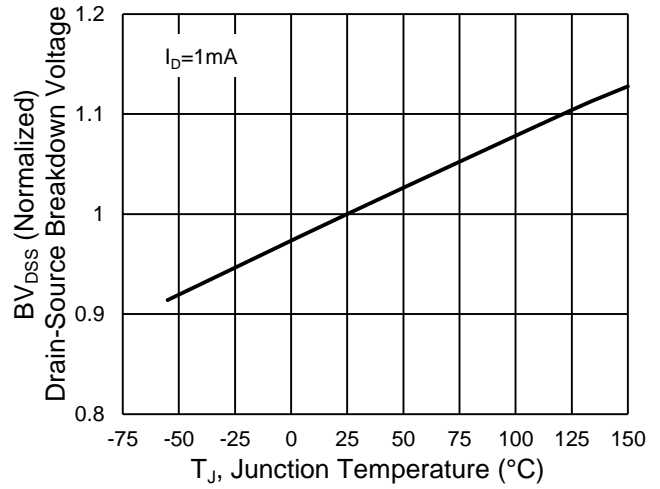
**CHARACTERISTICS CURVES**

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

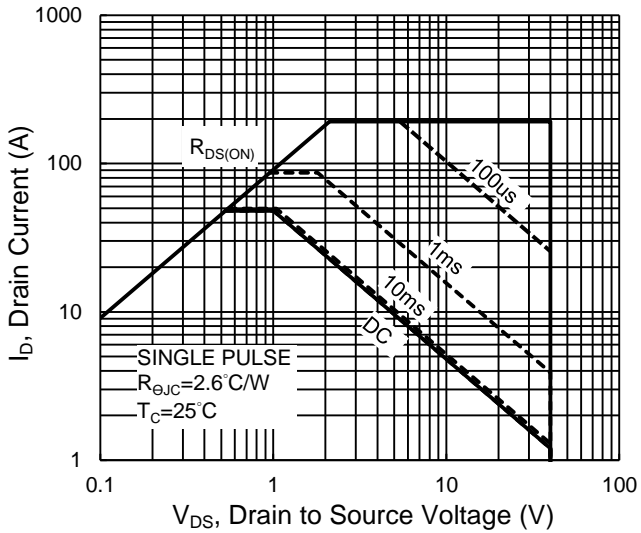
**Capacitance vs. Drain-Source Voltage**



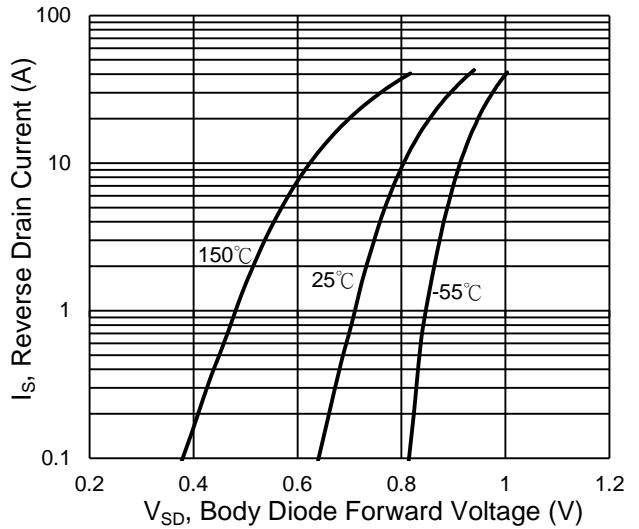
**$BV_{DSS}$  vs. Junction Temperature**



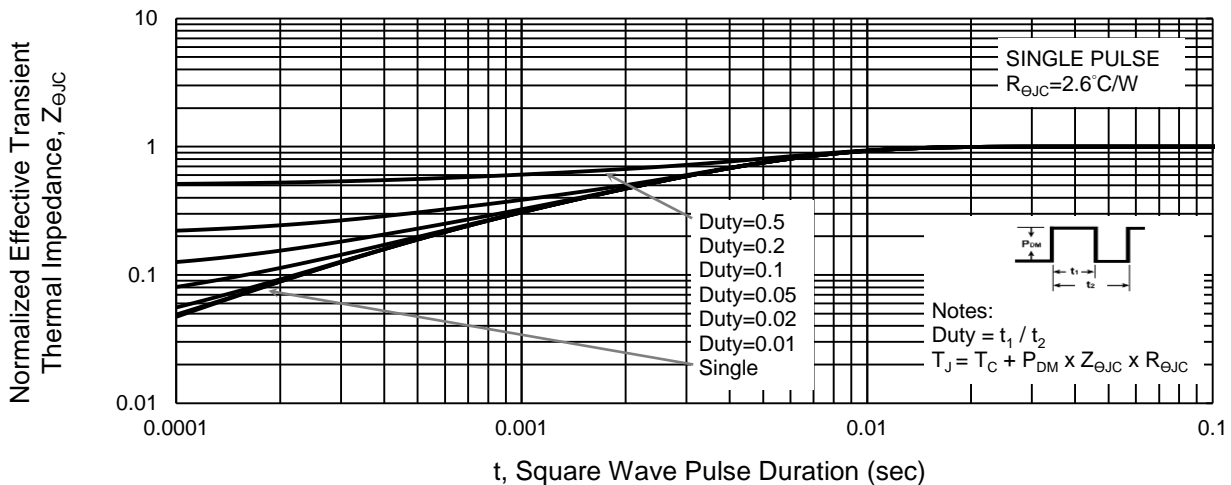
**Maximum Safe Operating Area, Junction-to-Case**



**Source-Drain Diode Forward Current vs. Voltage**

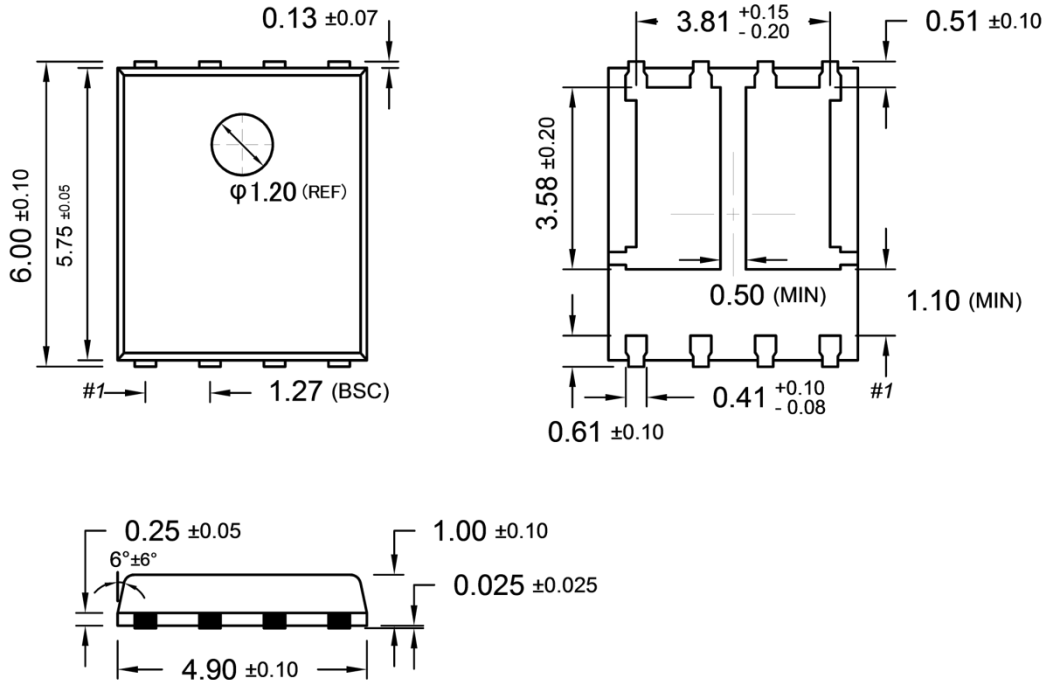


**Normalized Thermal Transient Impedance, Junction-to-Case**

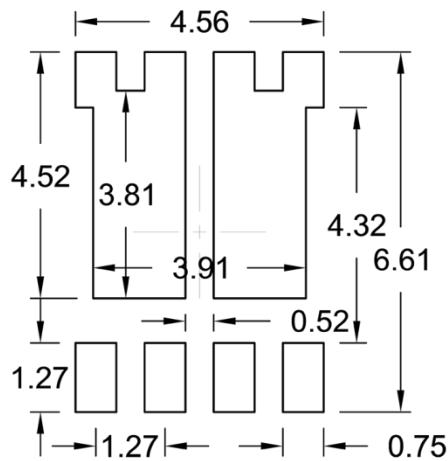


**PACKAGE OUTLINE DIMENSIONS** (Unit: Millimeters)

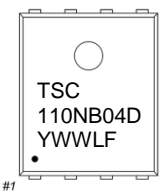
**PDFN56 Dual**



**SUGGESTED PAD LAYOUT** (Unit: Millimeters)



**MARKING DIAGRAM**



- Y** = Year Code
- WW** = Week Code (01~52)
- L** = Lot Code (1~9,A~Z)
- F** = Factory Code

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