

VALUE

600

10

6.1

HALOGEN

UNIT

V

Ω

nC

## **N-Channel Power MOSFET**

600V, 1A, 10Ω

#### FEATURES

- Advanced planar process
- 100% avalanche tested
- Low R<sub>DS(ON)</sub> 8Ω (Typ.)
- Low gate charge typical @ 6.1 nC (Typ.)
- Low Crss typical @4.2pF (Typ.)

#### APPLICATION

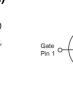
- Power Supply
- Lighting
- Charger

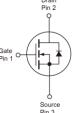


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**KEY PERFORMANCE PARAMETERS** 

PARAMETER

 $V_{\text{DS}}$ 

R<sub>DS(on)</sub> (max)

 $Q_{g}$ 

Notes: MSL 3 (Moisture Sensitivity Level) for TO-252 (D-PAK), SOT-223 per J-STD-020

PARAMETER	SYMBOL	IPAK/DPAK	SOT-223	UNIT
Drain-Source Voltage	V <sub>DS</sub>	60	V	
Gate-Source Voltage	V <sub>GS</sub>	±30		V
Continuous Drain Current <sup>(Note 1)</sup> $\frac{T_{C} = 25^{\circ}C}{T_{C} = 100^{\circ}C}$	- I <sub>D</sub>	1	7	A
Pulsed Drain Current (Note 2)	I <sub>DM</sub>	4		А
Total Power Dissipation @ $T_C = 25^{\circ}C$	P <sub>DTOT</sub>	39	2.1	W
Single Pulsed Avalanche Energy (Note 3)	E <sub>AS</sub>	5		mJ
Single Pulsed Avalanche Current (Note 3)	I <sub>AS</sub>	1		А
Peak Diode Recovery dv/dt <sup>(Note 4)</sup>	dv/dt	4.	5	V/ns
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	- 55 to	+150	°C

PARAMETER	SYMBOL	IPAK/DPAK	SOT-223	UNIT		
Junction to Case Thermal Resistance	R <sub>ejc</sub>	2.87		°C/W		
Junction to Ambient Thermal Resistance	R <sub>OJA</sub>	110	60	°C/W		

**Notes:**  $R_{\Theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins.  $R_{\Theta JA}$  is guaranteed by design while  $R_{\Theta CA}$  is determined by the user's board design.  $R_{\Theta JA}$  shown below for single device operation on FR-4 PCB in still air.



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PARAMETER	CONDITIONS	SYMBOL	MIN	ТҮР	MAX	UNIT
Static (Note 5)						•
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250 \mu A$	BV <sub>DSS</sub>	600			V
Drain-Source On-State Resistance	$V_{GS} = 10V, I_D = 0.5A$	R <sub>DS(ON)</sub>		8	10	Ω
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	V <sub>GS(TH)</sub>	2.5	3.5	4.5	V
Zero Gate Voltage Drain Current	$V_{DS} = 600V, V_{GS} = 0V$	I <sub>DSS</sub>			10	μA
Gate Body Leakage	$V_{GS} = \pm 30V, V_{DS} = 0V$	I <sub>GSS</sub>			±100	nA
Forward Transfer Conductance	$V_{DS} = 10V, I_{D} = 0.5A$	<b>g</b> <sub>fs</sub>		0.8		S
Dynamic (Note 6)						
Total Gate Charge		Qg		6.1		
Gate-Source Charge	$V_{DS} = 480V, I_D = 1A,$	Q <sub>gs</sub>		1.4		nC
Gate-Drain Charge	V <sub>GS</sub> = 10V	Q <sub>gd</sub>		3.3		
Input Capacitance		C <sub>iss</sub>		138		
Output Capacitance	$V_{DS} = 25V, V_{GS} = 0V,$ f = 1.0MHz	C <sub>oss</sub>		17.1		pF
Reverse Transfer Capacitance		C <sub>rss</sub>		4.2		
Gate Resistance	F = 1MHz, open drain	R <sub>g</sub>		12.5		Ω
Switching (Note 7)						
Turn-On Delay Time		t <sub>d(on)</sub>		7.7		
Turn-On Rise Time	$V_{DD} = 300V, R_{G} = 25\Omega$	t <sub>r</sub>		6.8		
Turn-Off Delay Time	$I_{\rm D} = 1$ A, $V_{\rm GS} = 10$ V	t <sub>d(off)</sub>		15.3		ns
Turn-Off Fall Time	-	t <sub>f</sub>		14.9		
Source-Drain Diode (Note 5)	·					
Diode Forward Voltage	$I_{\rm S}$ = 1A, $V_{\rm GS}$ = 0V	V <sub>SD</sub>		0.9	1.4	V
Source Current	Integral reverse diode	I <sub>S</sub>			1	
Source Current (Pulse)	In the MOSFET	I <sub>SM</sub>			4	A

Notes:

1. Current limited by package.

- 2. Pulse width limited by the maximum junction temperature.
- 3. L = 10mH, I<sub>AS</sub> = 1A, V<sub>DD</sub> = 50V, R<sub>G</sub> = 25 $\Omega$ , Starting T<sub>J</sub> = 25<sup>o</sup>C.
- 4.  $I_{SD} \le 1A$ ,  $V_{DD} \le BV_{DSS}$ , di/dt  $\le 200A/us$ , Starting  $T_J = 25^{\circ}C$ .
- 5. Pulse test:  $PW \le 300\mu s$ , duty cycle  $\le 2\%$ .
- 6. For DESIGN AID ONLY, not subject to production testing.
- 7. Switching time is essentially independent of operating temperature.



#### **ORDERING INFORMATION**

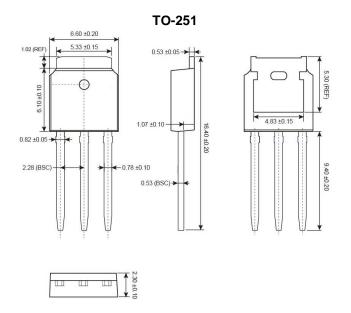
PART NO.	PACKAGE	PACKING
TSM1NB60CH C5G	TO-251	75 pcs / Tube
TSM1NB60CP ROG	TO-252	2,500 pcs / 13" Reel
TSM1NB60CW RPG	SOT-223	2,500 pcs / 13" Reel

Note:

1. Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC

2. Halogen-free according to IEC 61249-2-21 definition





#### **MARKING DIAGRAM**

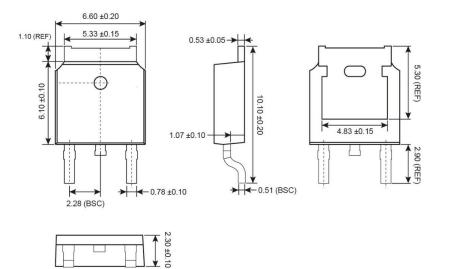
#1

	Y = Year Code
50	M = Month Code for Halogen Free Product
1NB60 YML	<b>O</b> =Jan <b>P</b> =Feb <b>Q</b> =Mar <b>R</b> =Apr
	<b>S</b> =May <b>T</b> =Jun <b>U</b> =Jul <b>V</b> =Aug
	W =Sep X =Oct Y =Nov Z =Dec
	L = Lot Code (1~9, A~Z)
#1	

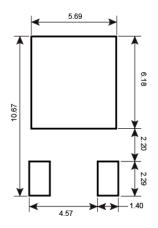




TO-252



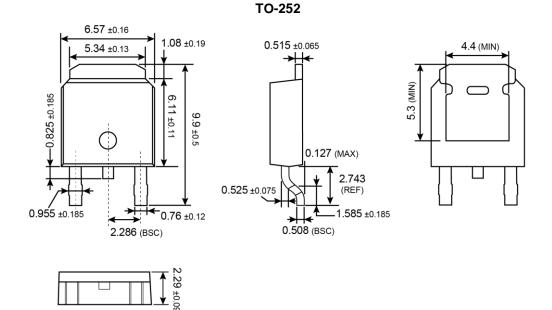
## SUGGESTED PAD LAYOUT



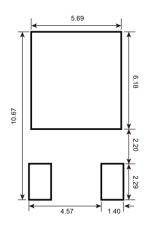
#### **MARKING DIAGRAM**

50	<ul><li>Y = Year Code</li><li>M = Month Code for Halogen</li></ul>	Free Product
1NB60 YML	<ul> <li>O =Jan P =Feb</li> <li>S =May T =Jun</li> <li>W =Sep X =Oct</li> <li>L = Lot Code (1~9, A~Z)</li> </ul>	U =Jul V =Aug





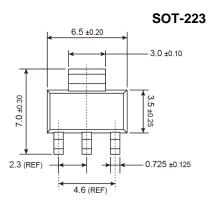
#### SUGGESTED PAD LAYOUT (Unit: Millimeters)



### **MARKING DIAGRAM**

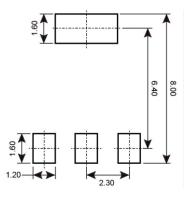
5	<ul><li>Y = Year Code</li><li>M = Month Code for Halog</li></ul>	en Free Product
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	W =Sep X =Oct	Y =Nov Z =Dec
#1	L = Lot Code (1~9, A~Z)	







## SUGGESTED PAD LAYOUT



#### **MARKING DIAGRAM**

1N YN	B60 /IL	
#1		

Υ	= Year Code
Μ	= Month Code for Halogen Free Product

<b>O</b> =Jan	P =Feb	<b>Q</b> =Mar	R =Apr
C May	T lun	11 1.1	V Aug

S	=May	т	=Jun	U	=Jul	V	=Aug
W	=Sep	Х	=Oct	Υ	=Nov	Ζ	=Dec

L = Lot Code (1~9, A~Z)



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