

SOT-23



Pin Definition:

1. Gate
2. Source
3. Drain

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (m Ω)	I_D (A)
-20	70 @ $V_{GS} = -4.5V$	-3.3
	90 @ $V_{GS} = -2.5V$	-2.0
	130 @ $V_{GS} = -1.8V$	-1.0

Features

- Advance Trench Process Technology
- High Density Cell Design for Ultra Low On-resistance

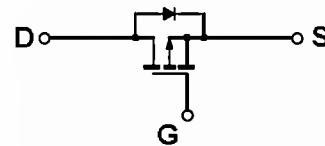
Application

- Load Switch
- PA Switch

Ordering Information

Part No.	Package	Packing
TSM2313CX RF	SOT-23	3Kpcs / 7" Reel

Block Diagram



P-Channel MOSFET

Absolute Maximum Rating (Ta = 25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	± 12	V
Continuous Drain Current, V_{GS} @4.5V.	I_D	-3.3	A
Pulsed Drain Current, V_{GS} @4.5V	I_{DM}	-20	A
Continuous Source Current (Diode Conduction) ^{a,b}	I_S	-1.7	A
Maximum Power Dissipation	P_D	Ta = 25°C	2
		Ta = 70°C	1.3
Operating Junction Temperature	T_J	+150	°C
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to +150	°C

Thermal Performance

Parameter	Symbol	Limit	Unit
Junction to Case Thermal Resistance	$R_{\theta JC}$	75	°C/W
Junction to Ambient Thermal Resistance (PCB mounted)	$R_{\theta JA}$	120	°C/W

Notes:

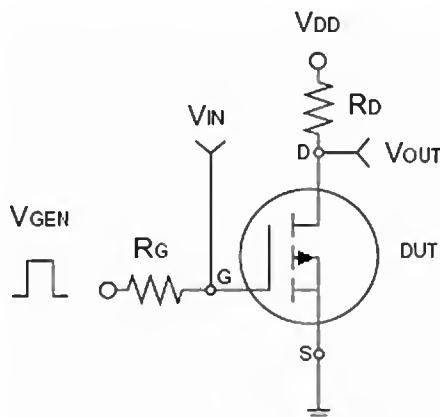
- a. Pulse width limited by the Maximum junction temperature
- b. Surface Mounted on FR4 Board, $t \leq 5$ sec.

Electrical Specifications (Ta = 25°C unless otherwise noted)

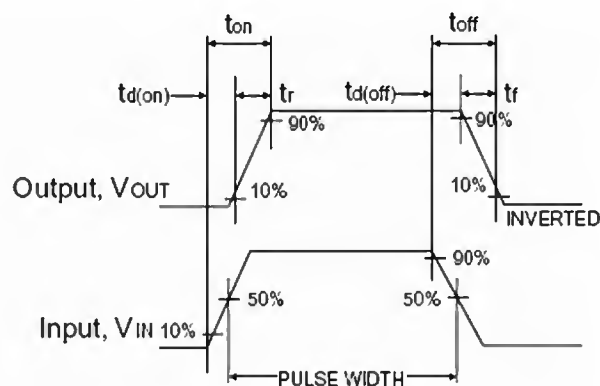
Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = -250\mu A$	BV_{DSS}	-20	--	--	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\mu A$	$V_{GS(TH)}$	-0.6	--	-1.4	V
Gate Body Leakage	$V_{GS} = \pm 12V, V_{DS} = 0V$	I_{GSS}	--	--	± 100	nA
Zero Gate Voltage Drain Current	$V_{DS} = -20V, V_{GS} = 0V$	I_{DSS}	--	--	-1.0	μA
On-State Drain Current ^a	$V_{DS} = -5V, V_{GS} = -4.5V$	$I_{D(ON)}$	-15	--	--	A
Drain-Source On-State Resistance ^a	$V_{GS} = -4.5V, I_D = -3.3A$	$R_{DS(ON)}$	--	55	70	m Ω
	$V_{GS} = -2.5V, I_D = -2.0A$		--	70	90	
	$V_{GS} = -1.8V, I_D = -1.0A$		--	120	130	
Forward Transconductance ^a	$V_{DS} = -10V, I_D = -4.7A$	g_{fs}	--	11	--	S
Diode Forward Voltage	$I_S = -1.7A, V_{GS} = 0V$	V_{SD}	--	-0.8	-1.2	V
Dynamic^b						
Total Gate Charge	$V_{DS} = -10V, I_D = -4.7A, V_{GS} = -4.5V$	Q_g	--	6	9	nC
Gate-Source Charge		Q_{gs}	--	1.4	--	
Gate-Drain Charge		Q_{gd}	--	1.9	--	
Input Capacitance	$V_{DS} = -10V, V_{GS} = 0V, f = 1.0MHz$	C_{iss}	--	640	--	pF
Output Capacitance		C_{oss}	--	180	--	
Reverse Transfer Capacitance		C_{rss}	--	90	--	
Switching^c						
Turn-On Delay Time	$V_{DD} = -10V, R_L = 10\Omega, I_D = -1A, V_{GEN} = -4.5V, R_G = 6\Omega$	$t_{d(on)}$	--	22	35	nS
Turn-On Rise Time		t_r	--	35	55	
Turn-Off Delay Time		$t_{d(off)}$	--	45	70	
Turn-Off Fall Time		t_f	--	25	50	

Notes:

- a. pulse test: PW $\leq 300\mu s$, duty cycle $\leq 2\%$
- b. For DESIGN AID ONLY, not subject to production testing.
- b. Switching time is essentially independent of operating temperature.

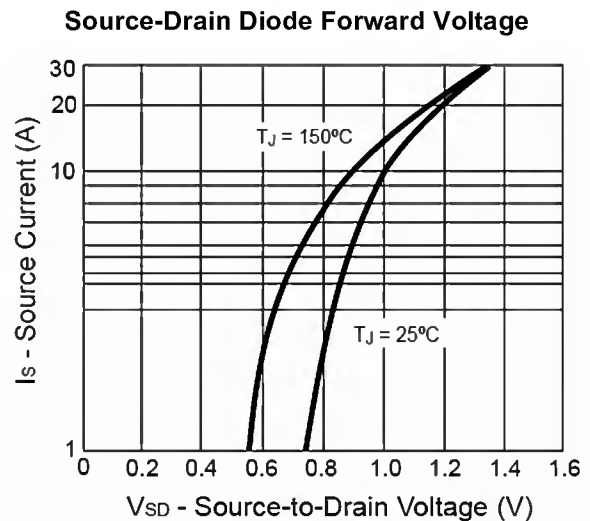
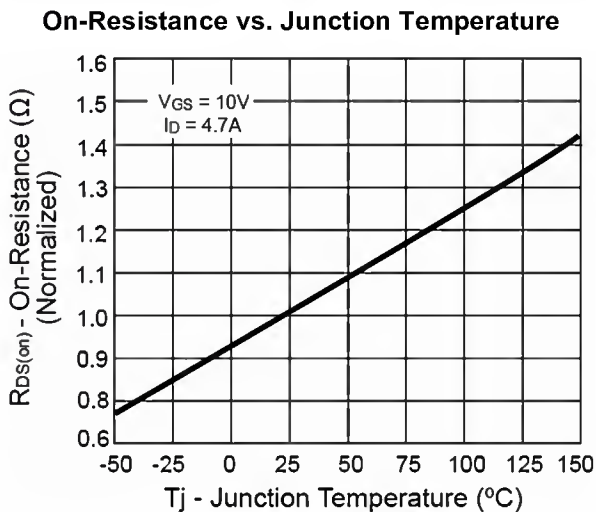
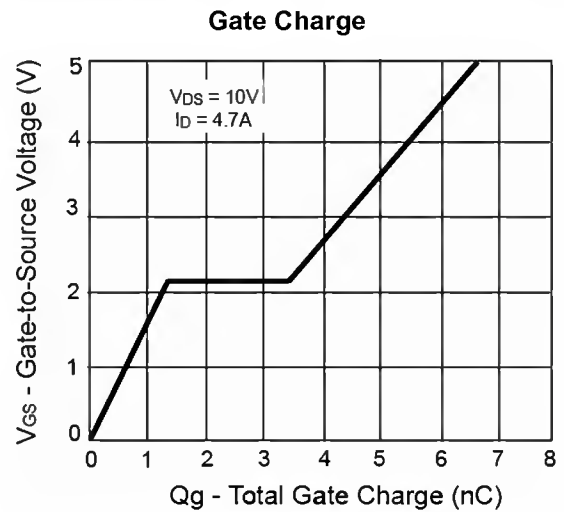
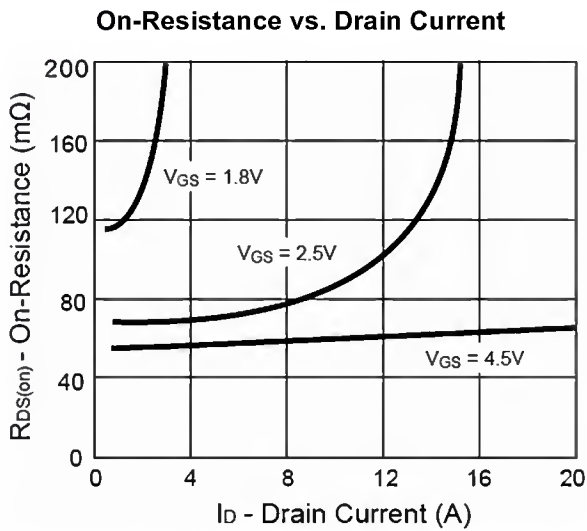
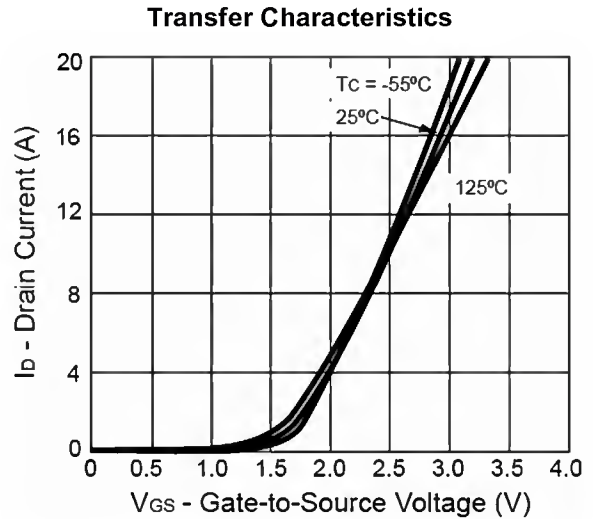
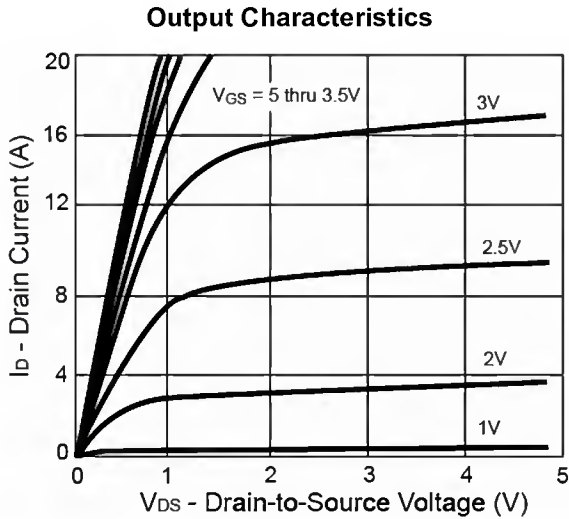


Switching Test Circuit



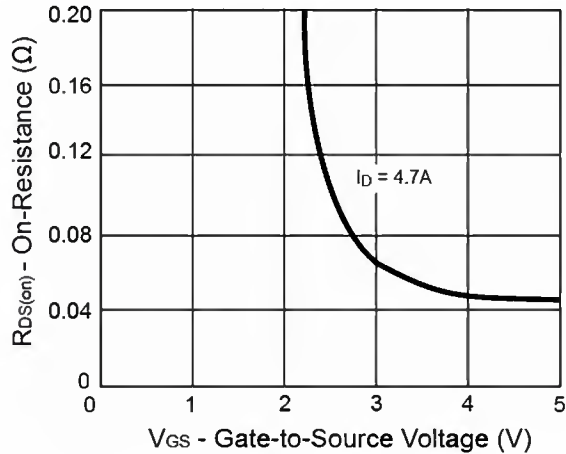
Switchin Waveforms

Electrical Characteristics Curve (Ta = 25°C, unless otherwise noted)

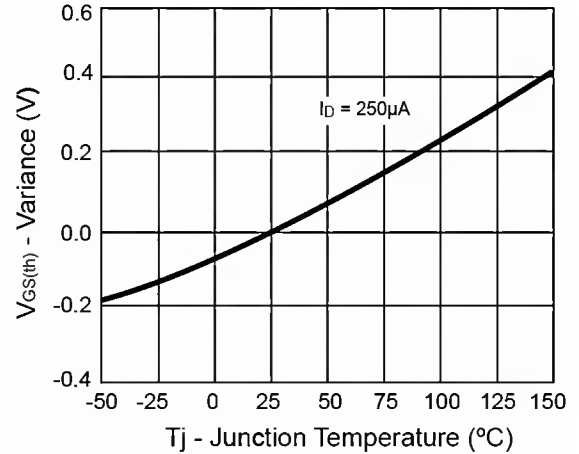


Electrical Characteristics Curve (Ta = 25°C, unless otherwise noted)

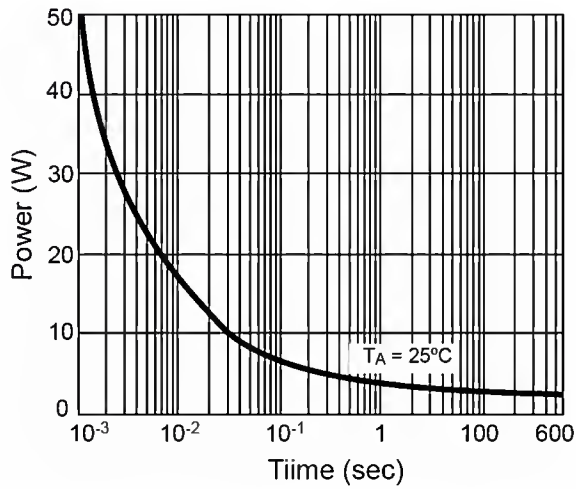
On-Resistance vs. Gate-Source Voltage



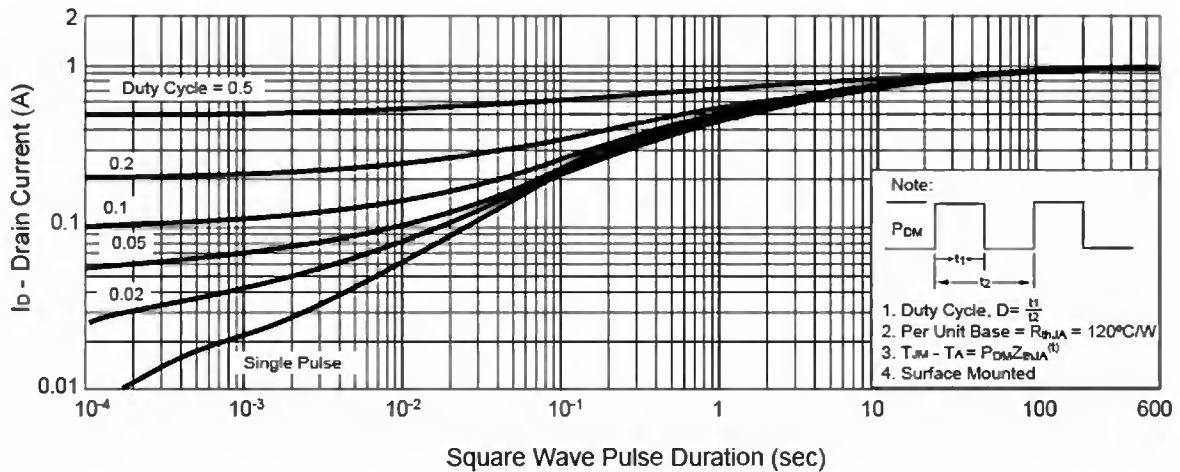
Threshold Voltage



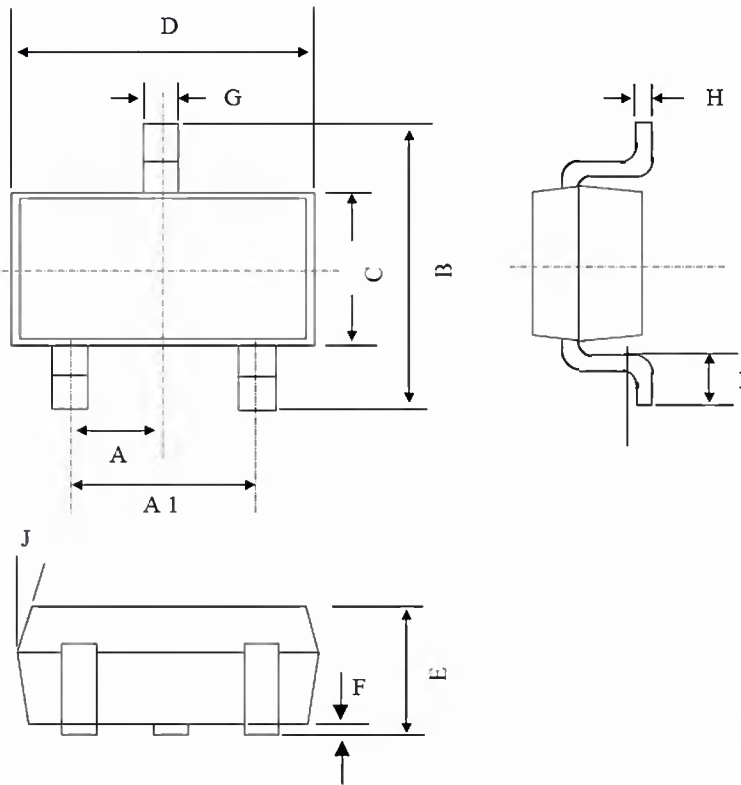
Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient

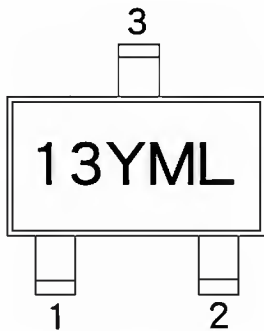


SOT-23 Mechanical Drawing



SOT-23 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX.
A	0.95 BSC		0.037 BSC	
A1	1.9 BSC		0.074 BSC	
B	2.60	3.00	0.102	0.118
C	1.40	1.70	0.055	0.067
D	2.80	3.10	0.110	0.122
E	1.00	1.30	0.039	0.051
F	0.00	0.10	0.000	0.004
G	0.35	0.50	0.014	0.020
H	0.10	0.20	0.004	0.008
I	0.30	0.60	0.012	0.024
J	5°	10°	5°	10°

Marking Diagram



- 13** = Device Code
- Y** = Year Code
- M** = Month Code
(A=Jan, B=Feb, C=Mar, D=Apl, E=May, F=Jun, G=Jul, H=Aug, I=Sep, J=Oct, K=Nov, L=Dec)
- L** = Lot Code

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