

N-Channel Power MOSFET

40V, 3.9A, 45mΩ

FEATURES

- Advance Trench Process Technology
- High density cell design for Ultra Low On-resistance
- Pb-free plating
- Compliant to RoHS Directive 2011/65/EU and in accordance to WEE2002/96/EC
- Halogen-free according to IEC 61249-2-21 definition

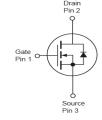
APPLICATION

- Load Switch
- Stepper Motors

KEY PERFORMANCE PARAMETERS					
PARA	METER	VALUE	UNIT		
V	DS	40	V		
R _{DS(on)} (max)	$V_{GS} = 10V$	45	mΩ		
	$V_{GS} = 4.5V$	62.5			
Qg		10	nC		







Notes: MSL 3 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T _A = 25°C unless otherwise noted)					
PARAMETER	SYMBOL	LIMIT	UNIT		
Drain-Source Voltage	V _{DS}	40	V		
Gate-Source Voltage	V _{GS}	±20	V		
Continuous Drain Current (Note 1)	I _D	3.9	А		
Pulsed Drain Current (Note 2)	I _{DM}	16	А		
Total Power Dissipation @ $T_A = 25^{\circ}C$	P _{DTOT}	1.25	W		
Operating Junction and Storage Temperature Range	T _J , T _{STG}	- 55 to +150	°C		

THERMAL PERFORMANCE						
PARAMETER	SYMBOL	LIMIT	UNIT			
Junction to Case Thermal Resistance	R _{eJC}	50	°C/W			
Junction to Ambient Thermal Resistance	R _{eja}	100	°C/W			

Notes: $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\Theta JA}$ is guaranteed by design while $R_{\Theta CA}$ is determined by the user's board design. $R_{\Theta JA}$ shown below for single device operation on FR-4 PCB with minimum recommended footprint in still air.





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PARAMETER	CONDITIONS SYMBOL		MIN	ТҮР	MAX	UNIT	
Static (Note 3)			•	•			
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250 \mu A$	BV _{DSS}	40			V	
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	V _{GS(TH)}	1		3	V	
Gate Body Leakage	$V_{GS} = \pm 20V, V_{DS} = 0V$	I _{GSS}			±100	nA	
Zero Gate Voltage Drain Current	$V_{DS} = 32V, V_{GS} = 0V$	I _{DSS}			1.0	μA	
	V _{GS} = 10V, I _D = 3.9A			36	45	6	
Drain-Source On-State Resistance	$V_{GS} = 4.5V, I_D = 3.5A$	R _{DS(on)}		50	62.5	mΩ	
Dynamic ^(Note 4)							
Total Gate Charge		Qg		10		nC	
Gate-Source Charge	$V_{DS} = 20V, I_D = 3.9A,$	Q _{gs}		1.6			
Gate-Drain Charge	$V_{GS} = 10V$	Q _{gd}		2.1			
Input Capacitance		C _{iss}		540			
Output Capacitance	$V_{DS} = 20V, V_{GS} = 0V,$	C _{oss}		80		pF	
Reverse Transfer Capacitance	f = 1.0MHz	C _{rss}		45			
Switching (Note 5)			•	•	•		
Turn-On Delay Time		t _{d(on)}		5			
Turn-On Rise Time	$V_{DD} = 20V, R_L = 20\Omega,$	tr		12		- ns	
Turn-Off Delay Time	$I_D = 1A, V_{GEN} = 10V,$	t _{d(off)}		20			
Turn-Off Fall Time	$R_{G} = 6\Omega$	t _f		15			
Source-Drain Diode (Note 3)		1					
Forward On Voltage	I _S = 1.25A, V _{GS} = 0V	V _{SD}		0.8	1.2	V	

Notes:

1. Current limited by package

2. Pulse width limited by the maximum junction temperature

3. Pulse test: PW \leq 300µs, duty cycle \leq 2%

4. For DESIGN AID ONLY, not subject to production testing.

5. Switching time is essentially independent of operating temperature.



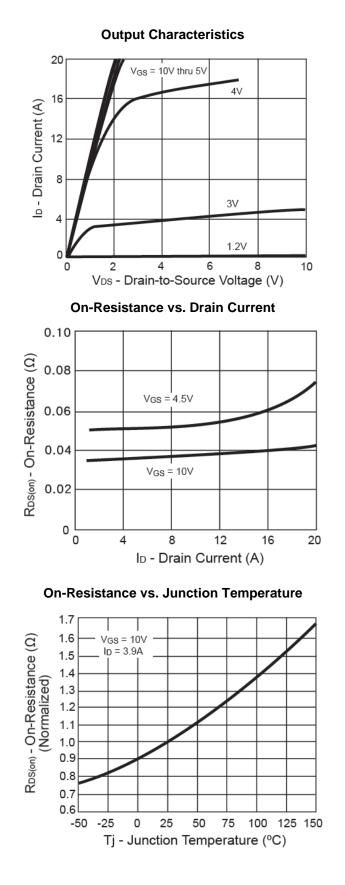
ORDERING INFORMATION

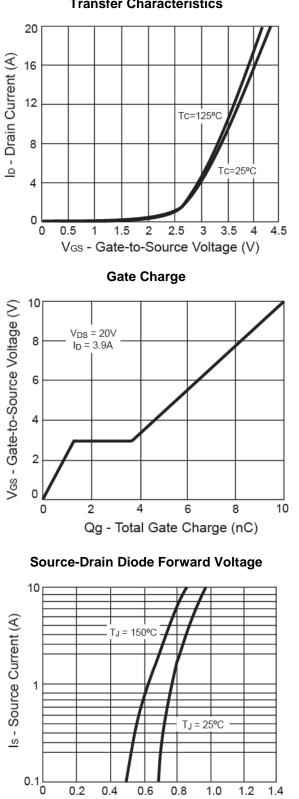
PART NO.	PACKAGE	PACKING
TSM2318CX RFG	SOT-23	3,000pcs / 7" Reel



CHARACTERISTICS CURVES

 $(T_c = 25^{\circ}C \text{ unless otherwise noted})$





Transfer Characteristics

1.4

1.2

1.0

0.2

0.4

0.6

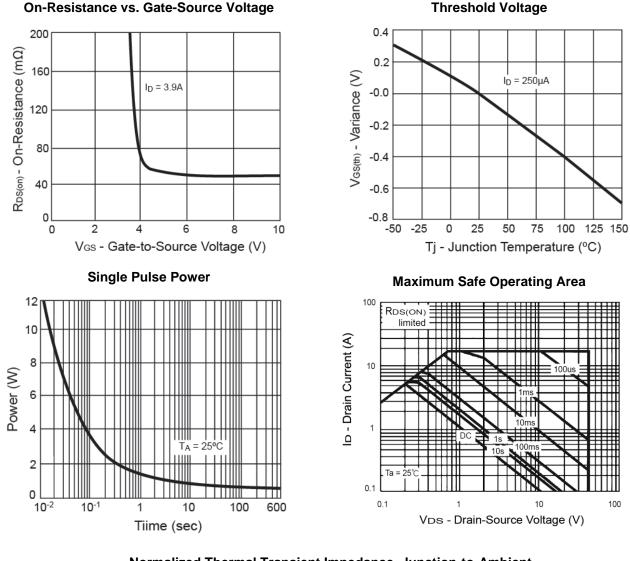
0.8

Vsp - Source-to-Drain Voltage (V)

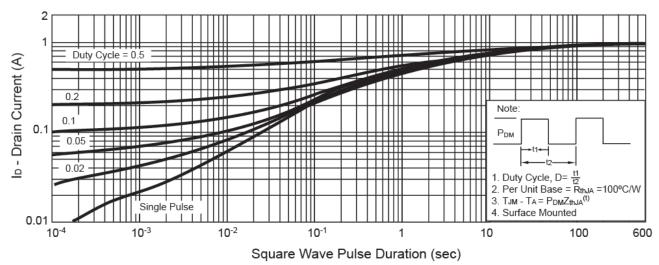


CHARACTERISTICS CURVES

(Tc = 25°C unless otherwise noted)

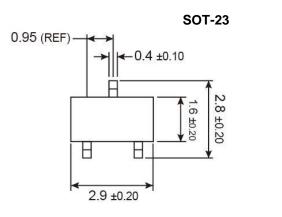


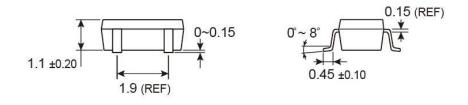




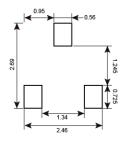


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

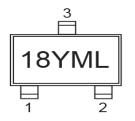




SUGGESTED PAD LAYOUT



MARKING DIAGRAM



Y	= Year Code						
Μ	= Month Code	for	Haloge	en Fr	ee Proo	duct	
	O =Jan	Ρ	=Feb	Q	=Mar	R	=Apr
	S =May	т	=Jun	U	=Jul	V	=Aug
	W =Sep	Х	=Oct	Υ	=Nov	Ζ	=Dec
L	= Lot Code (1-	-9,	A~Z)				



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