

UNIT

V

Ω

nC

VALUE

800

4.2

N-Channel Power MOSFET

800V, 3A, 4.2Ω

TO-251(IPAK)

D

- **FEATURES**
- Low R_{DS(ON)} 3.3Ω (Typ.)
- Low gate charge typical @ 19nC (Typ.)
- Low Crss typical @ 10.2pF (Typ.)

TO-220

Improved dv/dt capability

APPLICATION

- **Power Supply**
- Lighting

Pb-Free	HALOG

PARAMETER

 V_{DS}

R_{DS(on)} (max)

Notes: MSL 3 (Moisture Sensitivity Level) for TO-252 (D-PAK) per J-STD-020

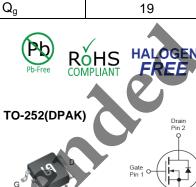
ITO-220

ABSOLUTE MAXIMUM RATINGS (T _A = 25°C unless otherwise noted)							
PARAMETER	SYMBOL	LIMIT					
		IPAK/DPAK	ITO-220	TO-220	UNIT		
Drain-Source Voltage	V _{DS}	800			V		
Gate-Source Voltage	V _{GS}	±30			V		
Continuous Drain Current (Note 4) $T_c = 25^{\circ}C$ $T_c = 100^{\circ}C$			A				
	I _D						
Pulsed Drain Current (Note 2)	I _{DM}	12			А		
Single Pulsed Avalanche Energy (Note 3)	E _{AS}	48			mJ		
Single Pulsed Avalanche Current (Note 3)	I _{AS}	3			А		
Repetitive Avalanche Energy (Note 3)	E _{AR}	9.4			mJ		
Repetitive Avalanche Energy ^(Note 4)	dV/dt	4.5		V/ns			
Total Power Dissipation @ T _c = 25°C	P _{DTOT}	94	32	94	W		
Operating Junction and Storage Temperature Range	T_{J},T_{STG}	- 55 to +150			°C		

THERMAL PERFORMANCE					
PARAMETER	SYMBOL				
		IPAK/DPAK	ITO-220	TO-220	UNIT
Junction to Case Thermal Resistance	R _{eJc}	1.33	3.9	1.33	°C/W
Junction to Ambient Thermal Resistance	R _{OJA}	110	62.5		°C/W

Notes: R_{0JA} is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. R_{0JA} is guaranteed by design while R_{0CA} is determined by the user's board design. R_{0JA} shown below for single device operation on FR-4 PCB in still air





KEY PERFORMANCE PARAMETERS



Taiwan Semiconductor

ELECTRICAL SPECIFICAT	FIONS (T _A = 25°C unless	otherwise not	ed)			
PARAMETER	CONDITIONS	SYMBOL	MIN	ТҮР	MAX	UNIT
Static (Note 5)						•
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250 \mu A$	BV _{DSS}	800			V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	V _{GS(TH)}	2		4	V
Gate Body Leakage	$V_{GS} = \pm 30 \text{V}, V_{DS} = 0 \text{V}$	I _{GSS}			±100	nA
Zero Gate Voltage Drain Current	$V_{DS} = 800V, V_{GS} = 0V$	I _{DSS}			10	μA
Drain-Source On-State Resistance	$V_{GS} = 10V, I_D = 1.5A$	R _{DS(ON)}		3.3	4.2	Ω
Forward Transfer Conductance	$V_{DS} = 30V, I_{D} = 1.5A$	g _{fs}		3.7		S
Dynamic ^(Note 6)						
Total Gate Charge		Qg	7	19		
Gate-Source Charge	$V_{DS} = 640V, I_D = 3A,$ $V_{GS} = 10V$	Q _{gs}		4		nC
Gate-Drain Charge	$V_{GS} = 10V$	Q _{gd}		7.6		
Input Capacitance		C _{iss}		696		pF
Output Capacitance	V _{DS} = 25V, V _{GS} = 0V, f = 1.0MHz	C _{oss}		65		
Reverse Transfer Capacitance		C _{rss}		10.2		
Gate Resistance	F = 1MHz, open drain	Rg		3.2		Ω
Switching ^(Note 7)						
Turn-On Delay Time		t _{d(on)}		48		
Turn-On Rise Time	$V_{GS} = 10V, I_D = 3A,$	t _r		36		
Turn-Off Delay Time	$V_{DD} = 400V, R_{G} = 25\Omega$	t _{d(off)}		106		ns
Turn-Off Fall Time		t _f 4	41			
Source-Drain Diode (Note 5)						
Source Current	Integral reverse diode	I _S			3	Α
Source Current (Pulse)	in the MOSFET	I _{SM}			12	Α
Diode Forward Voltage	$I_{\rm S}$ = 3A, $V_{\rm GS}$ = 0V	V _{SD}			1.5	V
Reverse Recovery Time	$V_{GS} = 0V, I_{S} = 3A,$	t _{rr}		370		ns
Reverse Recovery Charge	dI _F /dt = 100A/us	Q _{rr}		1.8		μC

Notes:

1. Current limited by package

- 2. Pulse width limited by the maximum junction temperature
- 3. L = 10mH, I_{AS} = 3A, V_{DD} = 50V, R_G = 25 Ω , Starting T_J = 25 $^{\circ}$ C
- 4. $I_{SD} \le 3A$, dI/dt $\le 200A/uS$, $V_{DD} \le BV_{DSS}$, Starting $T_J = 25^{\circ}C$
- 5. Pulse test: PW \leq 300µs, duty cycle \leq 2%
- 6. For DESIGN AID ONLY, not subject to production testing.
- 7. Switching time is essentially independent of operating temperature.

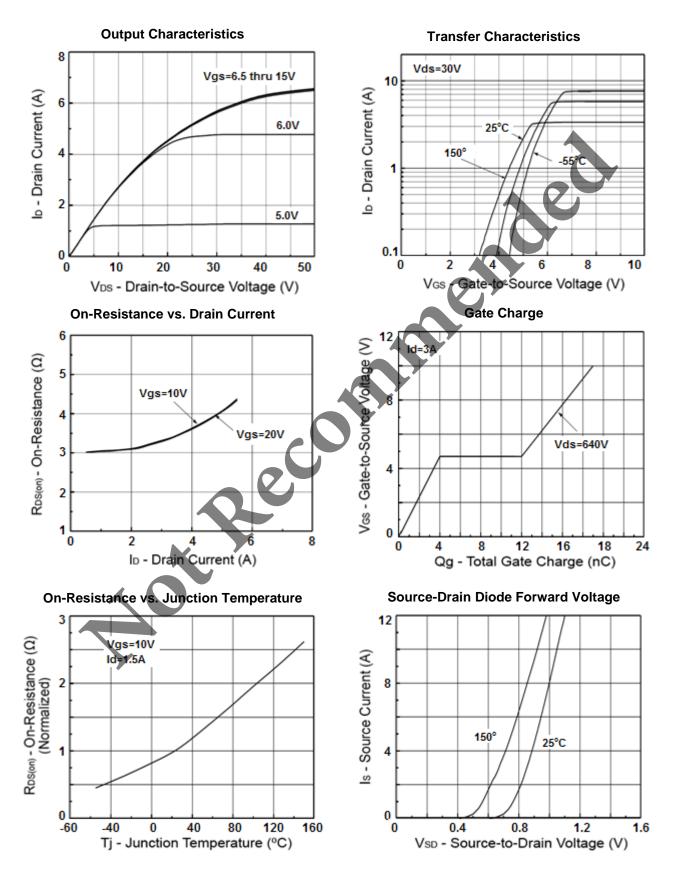


ORDERING INFORMATION



CHARACTERISTICS CURVES

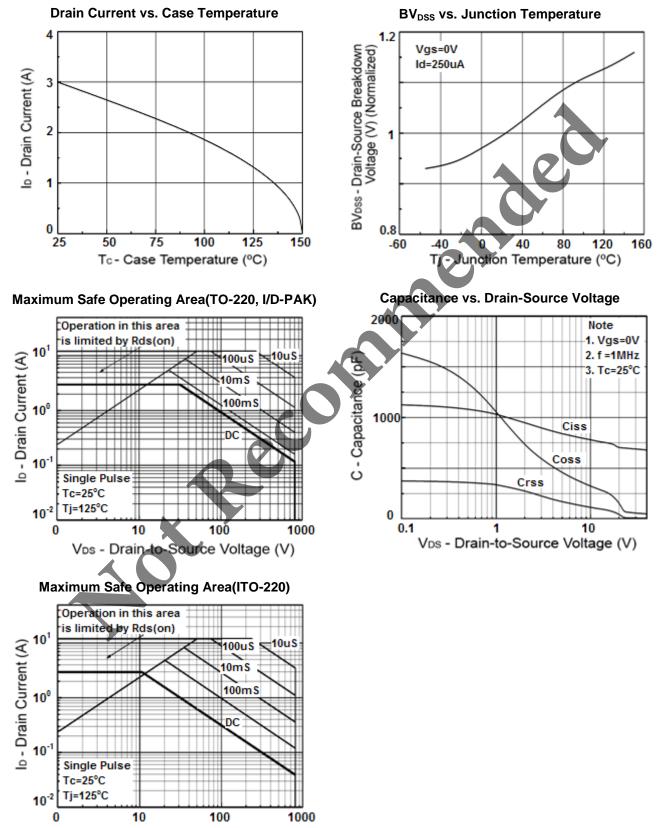
 $(T_c = 25^{\circ}C \text{ unless otherwise noted})$





CHARACTERISTICS CURVES

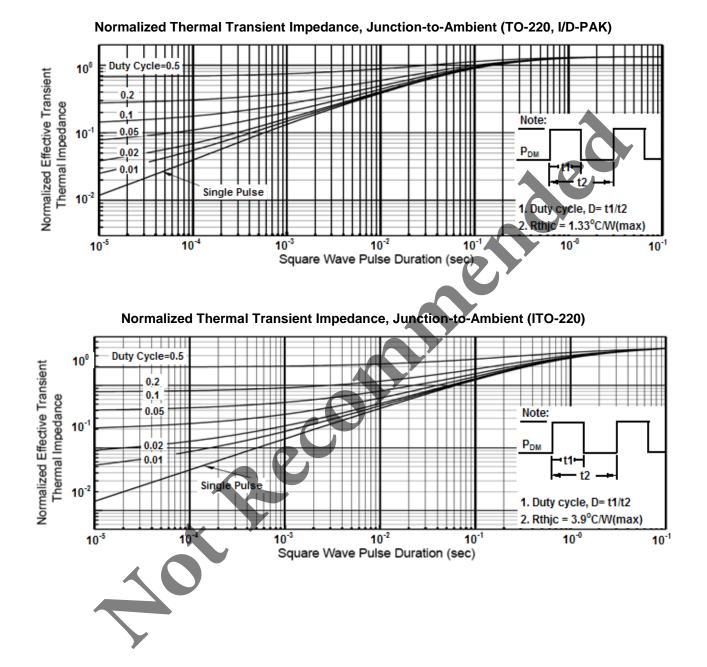
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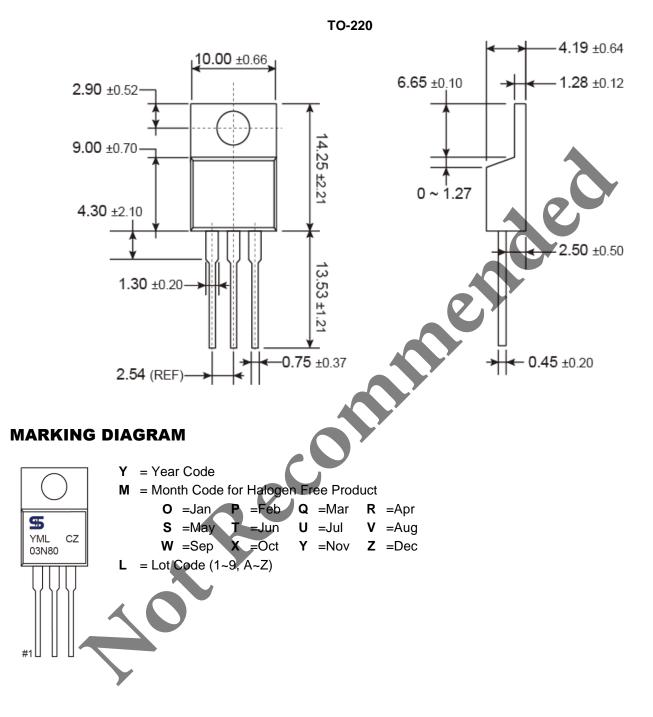


CHARACTERISTICS CURVES

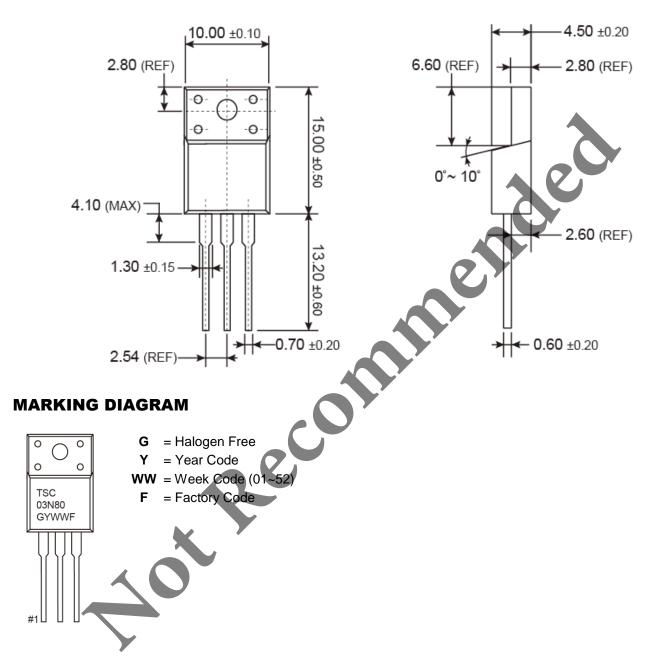
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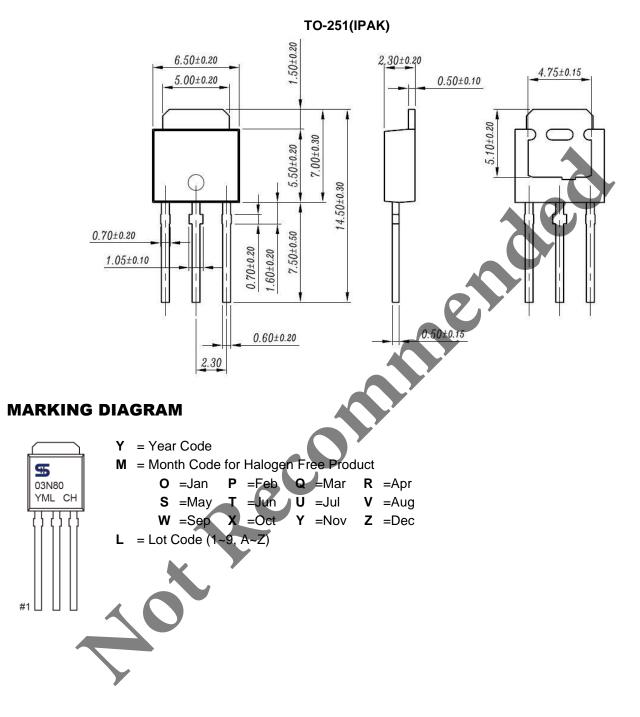






ITO-220

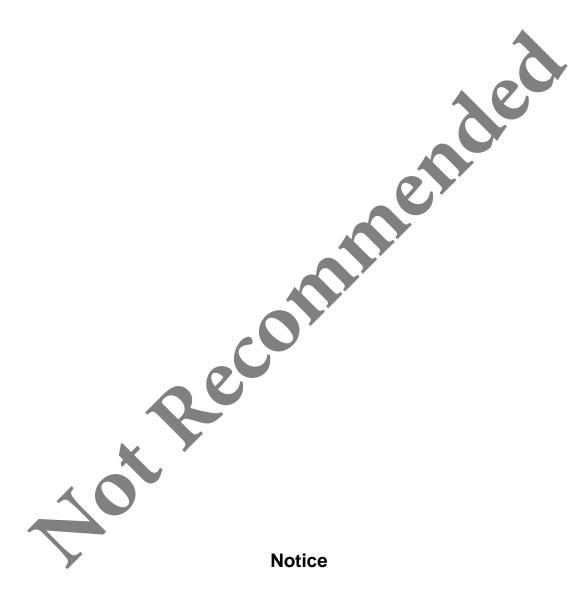






TO-252(DPAK) 2,30±0.20 6.50±0.20 1.50±0.20 5.00±0.20 0.50 4.75±0.15 5.10 ± 0.20 7.00 ± 0.30 5.50 ± 0.20 20±0.30 0.80±0.30 Н H 2.50 ± 0.30 0.60±0.20 0~0.20 0.85±0.20 1.20±0.30 2.30 0.50±0.15 SUGGESTED PAD LAYOUT (Unit: Millimeters) 5.69 6.18 10.67 2.20 2.29 - 1.40 4.57 **MARKING DIAGRAM** Year Code Month Code for Halogen Free Product м Ŧ **Q** =Mar **R** =Apr **O** =Jan P =Feb 03N80 YML CP **S** =May T =Jun U =Jul V =Aug W =Sep X =Oct Y =Nov Z =Dec П = Lot Code $(1 \sim 9, A \sim Z)$ L





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