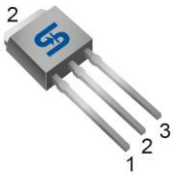
TSM60N750

600V, 6A, 0.75Ω
N-Channel Power MOSFET

TO-252 (DPAK)

TO-251 (IPAK)



Pin Definition:
1. Gate
2. Drain
3. Source

Key Parameter Performance

Parameter	Value	Unit
V_{DS}	600	V
$R_{DS(on)}$ (max)	0.75	Ω
Q_g	10.8	nC

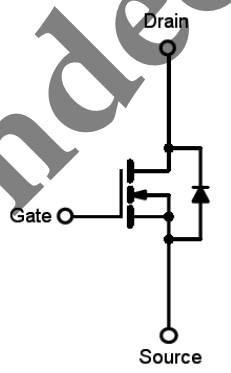
Features

- Super-Junction technology
- High performance due to small figure-of-merit
- High ruggedness performance
- High commutation performance

Application

- Power Supply.
- Lighting

Block Diagram



N-Channel MOSFET

Ordering Information

Part No.	Package	Packing
TSM60N750CH C5G	TO-251	75pcs / Tube
TSM60N750CP ROG	TO-252	2.5kpcs / 13" Reel

Note: "G" denotes for Halogen- and Antimony-free as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds

Absolute Maximum Ratings (T_A=25°C unless otherwise noted)

Parameter		Symbol	Limit IPAK/DPAK	Unit
Drain-Source Voltage		V_{DS}	600	V
Gate-Source Voltage		V_{GS}	±30	V
Continuous Drain Current (Note 1)	T_C = 25°C	I_D	6	A
Pulsed Drain Current (Note 2)		I_{DM}	18	A
Total Power Dissipation @ T_C=25°C		P_{DTOT}	62.5	W
Single Pulsed Avalanche Energy (Note 3)		E_{AS}	90	mJ
Single Pulsed Avalanche Current (Note 3)		I_{AS}	1.9	A
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +150	°C

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Thermal Performance

Parameter	Symbol	Limit	Unit
		IPAK/DPAK	
Junction to Case Thermal Resistance	$R_{\Theta JC}$	2	°C/W
Junction to Ambient Thermal Resistance	$R_{\Theta JA}$	62	°C/W

Electrical Specifications (T_J=25°C unless otherwise noted)

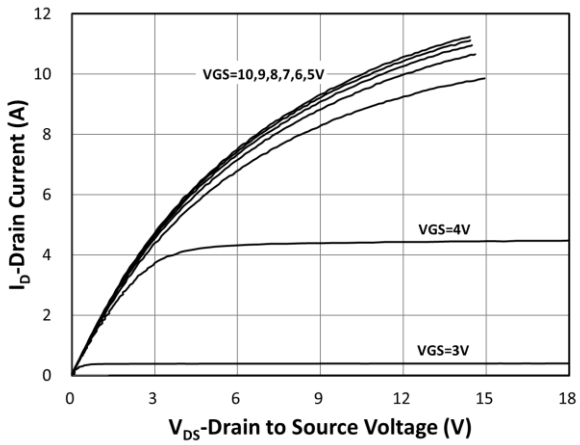
Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static (Note 4)						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	BV_{DSS}	600	--	--	V
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	$V_{GS(TH)}$	2	3	4	V
Gate Body Leakage	V_{GS} = ±30V, V_{DS} = 0V	I_{GSS}	--	--	±100	nA
Zero Gate Voltage Drain Current	V_{DS} = 600V, V_{GS} = 0V	I_{DSS}	--	--	1	μA
Drain-Source On-State Resistance	V_{GS} = 10V, I_D = 3A	$R_{DS(ON)}$	--	0.53	0.75	Ω
Dynamic (Note 5)						
Total Gate Charge	V_{DS} = 380V, I_D = 6A, V_{GS} = 10V	Q_g	--	10.8	--	nC
Gate-Source Charge		Q_{gs}	--	2.7	--	
Gate-Drain Charge		Q_{gd}	--	3.7	--	
Input Capacitance	V_{DS} = 100V, V_{GS} = 0V, f = 1.0MHz	C_{iss}	--	554	--	pF
Output Capacitance		C_{oss}	--	46	--	
Gate Resistance	f=1MHz, open drain	R_g	--	2.7	--	Ω
Switching (Note 6)						
Turn-On Delay Time	V_{DD} = 380V, R_{GEN} = 25Ω, I_D = 6A, V_{GS} = 10V,	$t_{d(on)}$	--	17.3	--	ns
Turn-On Rise Time		t_r	--	22	--	
Turn-Off Delay Time		$t_{d(off)}$	--	28	--	
Turn-Off Fall Time		t_f	--	22	--	
Source-Drain Diode (Note 4)						
Forward On Voltage	I_S=6A, V_{GS}=0V	V_{SD}	--	--	1.4	V
Reverse Recovery Time	V_R=200V, I_S=3A dI$_F$/dt=100A/μs	t_{rr}	--	182	--	ns
Reverse Recovery Charge		Q_{rr}	--	1.3	--	μC

Notes:

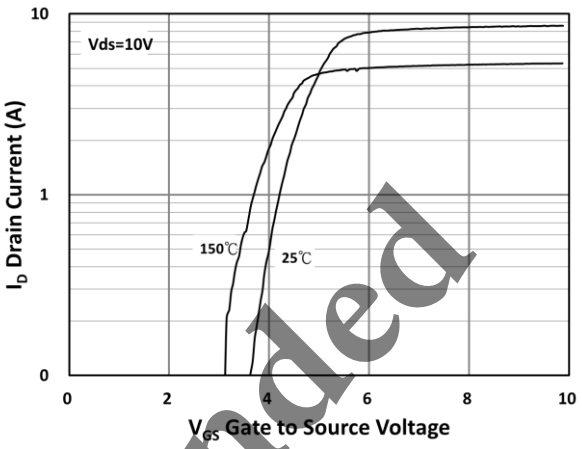
1. Current limited by package
2. Pulse width limited by the maximum junction temperature
3. L=50mH, I_{AS}=1.9A, V_{DD}=50V, R_G=25Ω, Starting T_J=25°C
4. Pulse test: PW ≤ 300μs, duty cycle ≤ 2%
5. For DESIGN AID ONLY, not subject to production testing.
6. Switching time is essentially independent of operating temperature.

Electrical Characteristics Curves

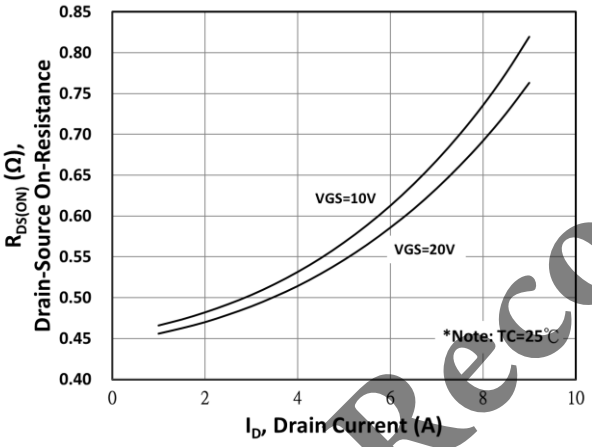
Output Characteristics



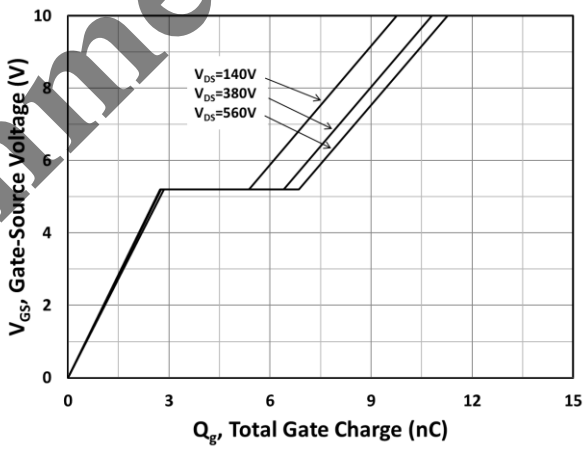
Transfer Characteristics



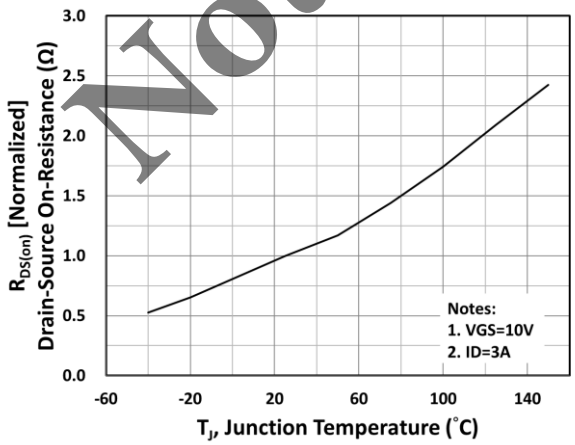
On-Resistance vs. Drain Current



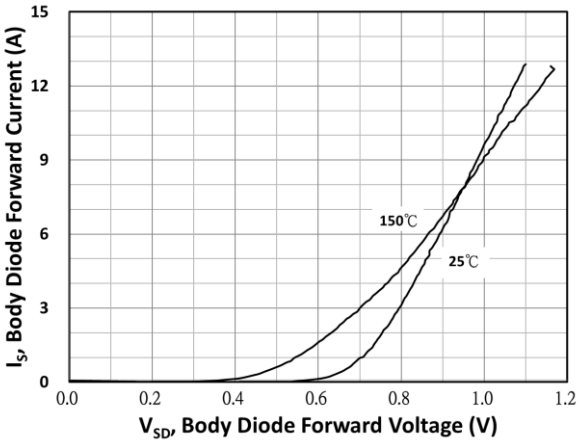
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Current vs. Voltage



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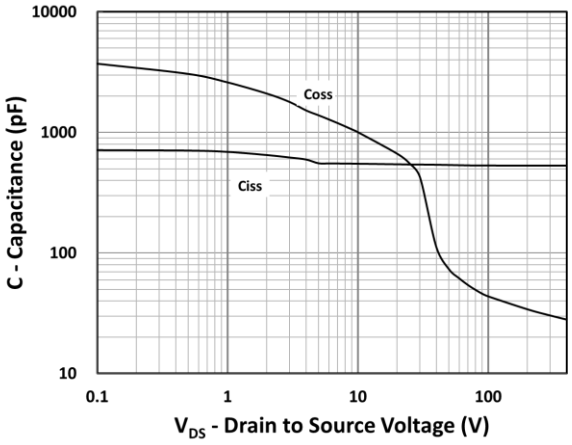
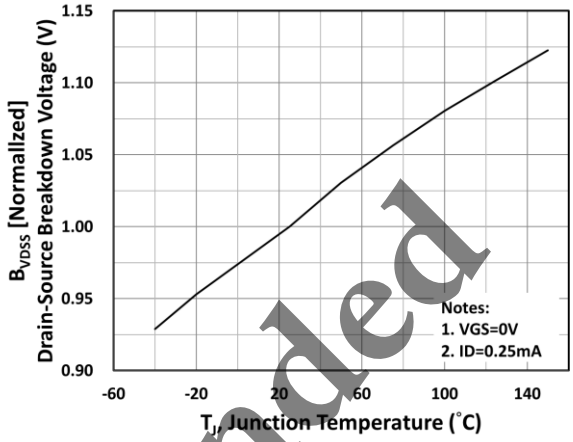
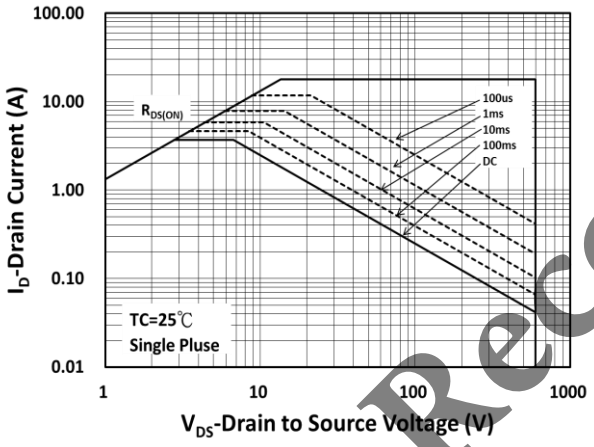
Capacitance vs. Drain-Source Voltage



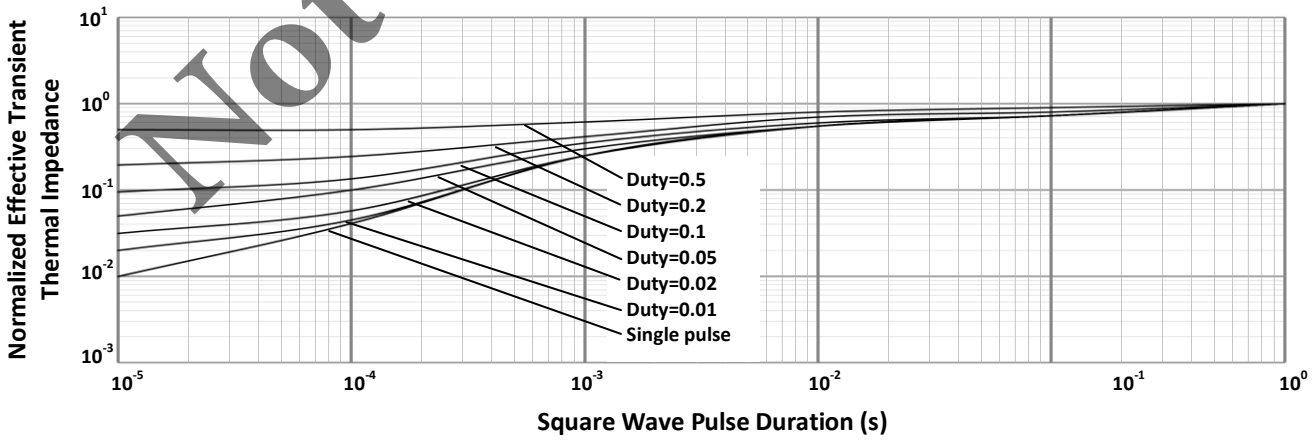
BV_{DSS} vs. Junction Temperature



Maximum Safe Operating Area (DPAK/IPAK)



Normalized Thermal Transient Impedance, Junction-to-Case (DPAK/IPAK)



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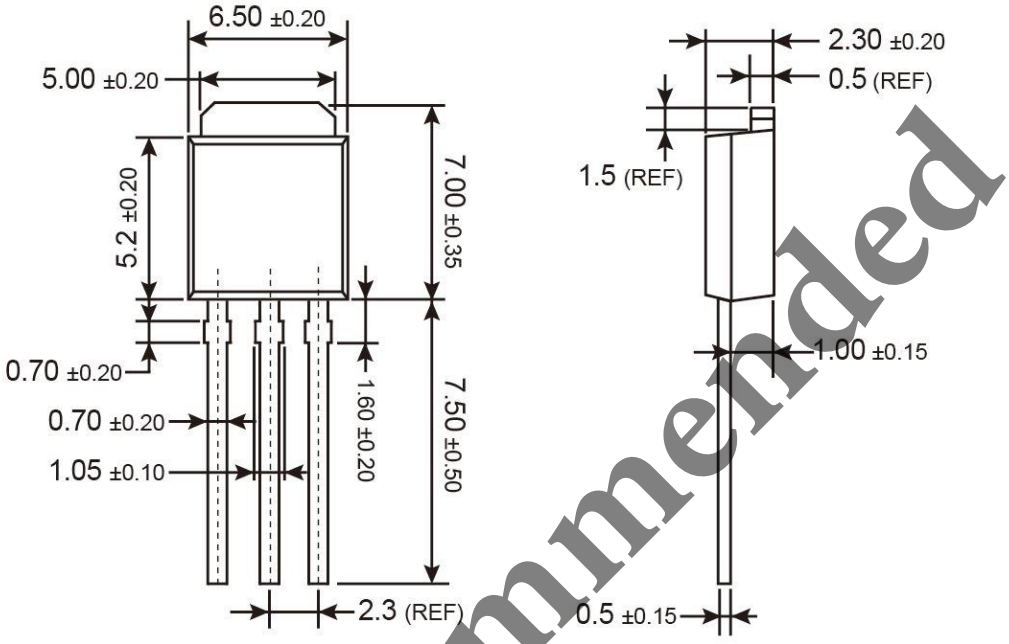
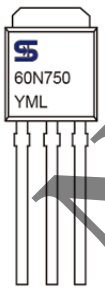
TO-251 (IPAK) Mechanical Drawing



Unit: Millimeters

Marking Diagram



Y = Year Code
M = Month Code for Halogen Free Product
(**O**=Jan, **P**=Feb, **Q**=Mar, **R**=Apl, **S**=May, **T**=Jun, **U**=Jul, **V**=Aug, **W**=Sep, **X**=Oct, **Y**=Nov, **Z**=Dec)
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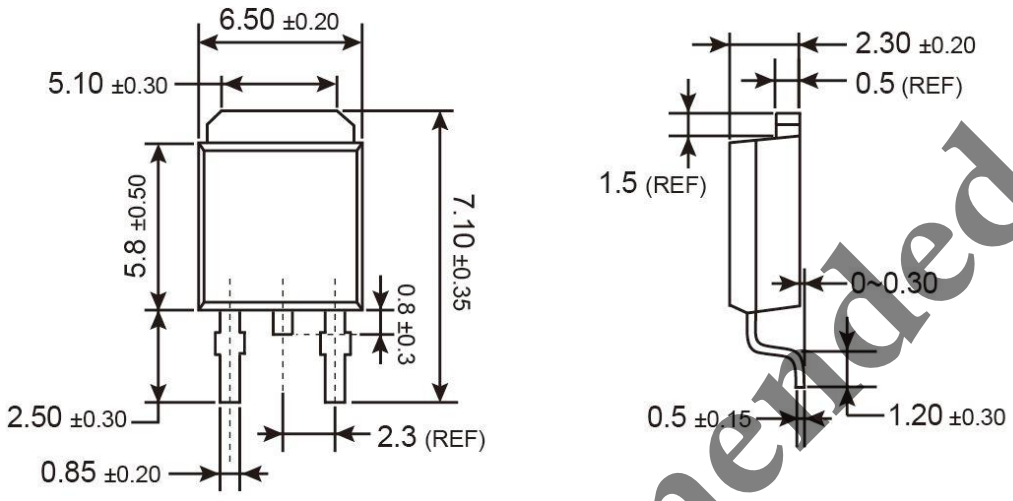
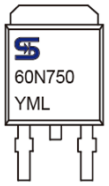


Unit: Millimeters

Marking Diagram



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