

P-Channel Power MOSFET

-60V, -18A, 68mΩ

FEATURES

- Improved dV/dt capability
- Fast switching
- 100% Eas Guaranteed
- Pb-free plating
- RoHS compliant
- Halogen-free mold compound

KEY PERFORMANCE PARAMETERS		
PARAMETER	VALUE	UNIT
V_{DS}	-60	V
$R_{DS(on)}$ (max)	$V_{GS} = -10V$	68
	$V_{GS} = -4.5V$	110
Q_g	16.4	nC

APPLICATION

- Motor Drive
- Power Tools
- LED Lighting



Notes: Moisture sensitivity level: level 3. Per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)					
PARAMETER	SYMBOL	IPAK/DPAK	ITO-220	TO-220	UNIT
Drain-Source Voltage	V_{DS}	-60			V
Gate-Source Voltage	V_{GS}	±20			V
Continuous Drain Current (Note 1)	I_D	$T_C = 25^\circ\text{C}$	-18		A
		$T_C = 100^\circ\text{C}$	-11		
Pulsed Drain Current (Note 2)	I_{DM}	-72			A
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_{DTOT}	20	17	42	W
Single Pulsed Avalanche Energy (Note 3)	E_{AS}	12.8			mJ
Single Pulsed Avalanche Current (Note 3)	I_{AS}	-16			A
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to +150			$^\circ\text{C}$

THERMAL PERFORMANCE					
PARAMETER	SYMBOL	IPAK/DPAK	ITO-220	TO-220	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	6.1	7.5	3	$^\circ\text{C/W}$
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	62			$^\circ\text{C/W}$

Notes: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 PCB in still air.

ELECTRICAL SPECIFICATIONS ($T_C = 25^\circ\text{C}$ unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static (Note 4)						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = -250\mu A$	BV_{DSS}	-60	--	--	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\mu A$	$V_{GS(TH)}$	-1.2	-1.6	-2.2	V
Gate Body Leakage	$V_{GS} = \pm 20V, V_{DS} = 0V$	I_{GSS}	--	--	± 100	nA
Zero Gate Voltage Drain Current	$V_{DS} = -60V, V_{GS} = 0V$	I_{DSS}	--	--	-1	μA
	$V_{DS} = -48V, T_C = 125^\circ\text{C}$		--	--	-10	
Drain-Source On-State Resistance	$V_{GS} = -10V, I_D = -6A$	$R_{DS(on)}$	--	54	68	m Ω
	$V_{GS} = -4.5V, I_D = -3A$		--	72	110	
Forward Transconductance	$V_{DS} = -10V, I_D = -6A$	g_{fs}	--	8.5	--	S
Dynamic (Note 5)						
Total Gate Charge	$V_{DS} = -30V, I_D = -6A, V_{GS} = -10V$	Q_g	--	16.4	--	nC
Gate-Source Charge		Q_{gs}	--	2.8	--	
Gate-Drain Charge		Q_{gd}	--	3.6	--	
Input Capacitance	$V_{DS} = -30V, V_{GS} = 0V, f = 1.0\text{MHz}$	C_{iss}	--	870	--	pF
Output Capacitance		C_{oss}	--	70	--	
Reverse Transfer Capacitance		C_{rss}	--	42	--	
Gate Resistance	$f = 1\text{MHz}, \text{open drain}$	R_g	--	16	--	Ω
Switching (Note 6)						
Turn-On Delay Time	$V_{DD} = -30V, R_{GEN} = 6\Omega, I_D = -1A$	$t_{d(on)}$	--	8.3	--	ns
Turn-On Rise Time		t_r	--	29.6	--	
Turn-Off Delay Time		$t_{d(off)}$	--	51.7	--	
Turn-Off Fall Time		t_f	--	15.6	--	
Source-Drain Diode (Note 3)						
Forward On Voltage	$I_S = -1A, V_{GS} = 0V$	V_{SD}	--	--	-1	V
Reverse Recovery Time	$I_S = 1A, di_f/dt = 100A/\mu s$	t_{rr}	--	20	--	ns
Reverse Recovery Charge		Q_{rr}	--	10	--	nC
Maximum Continuous Forward Current	Integral reverse diode in the MOSFET	I_S	--	--	-13	A
Maximum Pulse Forward Current		I_{SM}	--	--	-52	A

Notes:

- Current limited by package
- Pulse width limited by the maximum junction temperature
- $L = 0.1\text{mH}, I_{AS} = -16A, V_{DD} = -25V, R_G = 25\Omega, \text{Starting } T_J = 25^\circ\text{C}$
- Pulse test: $PW \leq 300\mu s, \text{duty cycle} \leq 2\%$
- For DESIGN AID ONLY, not subject to production testing.
- Switching time is essentially independent of operating temperature.

ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM680P06CZ C0G	TO-220	50pcs / Tube
TSM680P06CI C0G	ITO-220	50pcs / Tube
TSM680P06CH C5G	TO-251S (IPAK SL)	75pcs / Tube
TSM680P06CP ROG	TO-252 (DPAK)	2,500pcs / 13" Reel

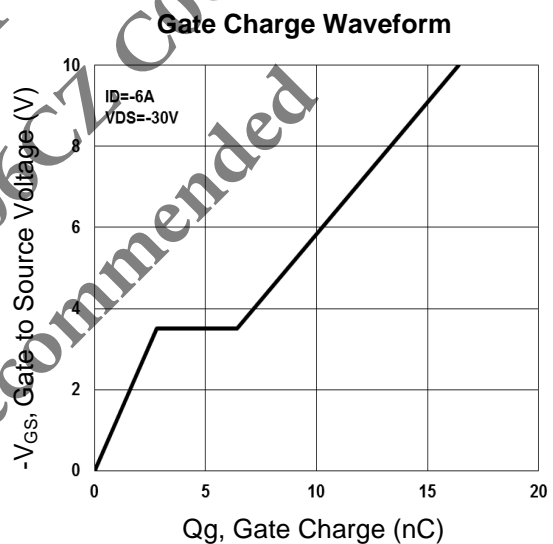
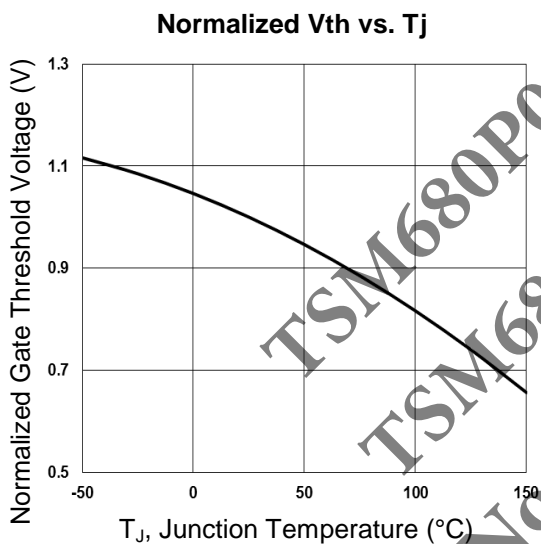
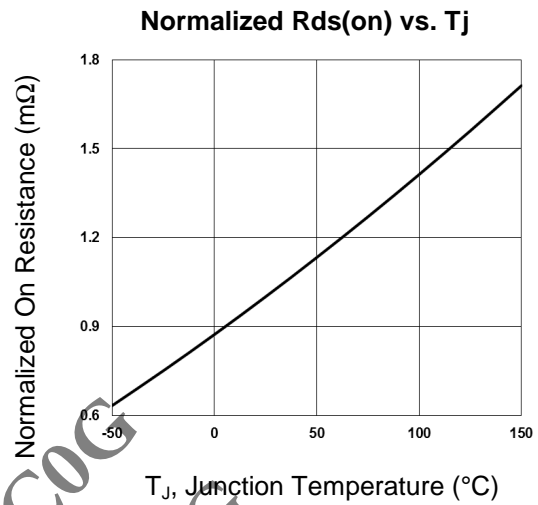
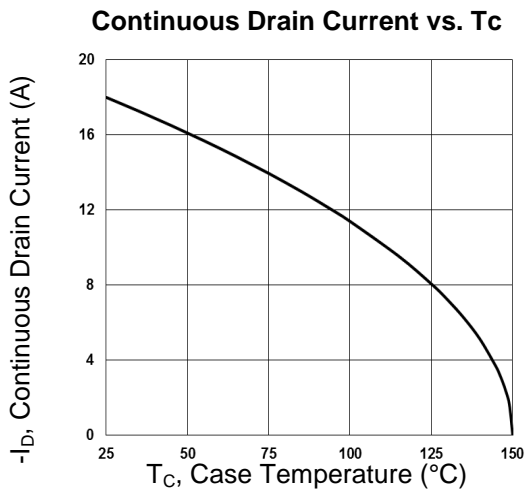
Note:

1. Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC
2. Halogen-free according to IEC 61249-2-21 definition

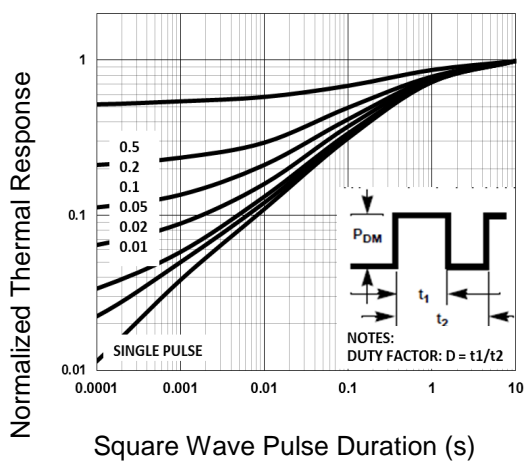
TSM680P06CI C0G
 TSM680P06CZ C0G
 Not Recommended

CHARACTERISTICS CURVES

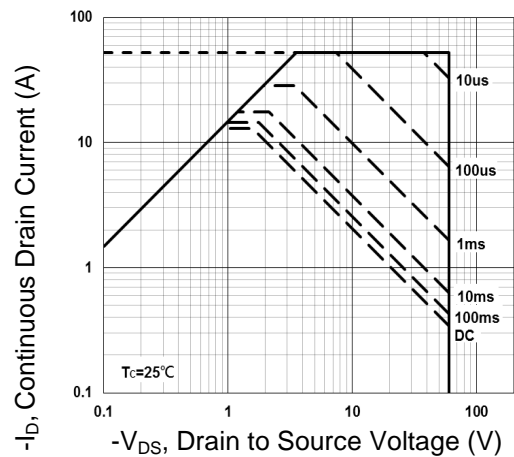
($T_C = 25^\circ\text{C}$ unless otherwise noted)



Normalized Transient Impedance (TO-251S)



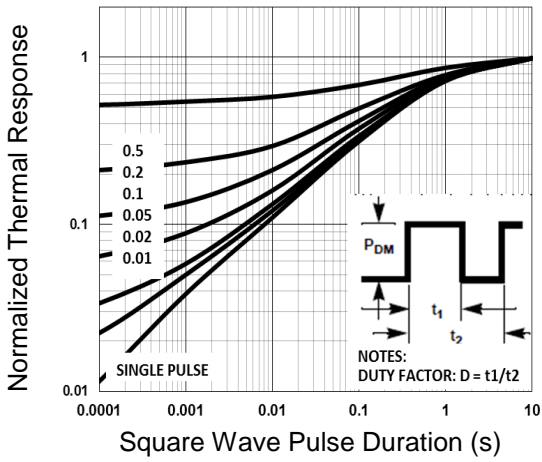
Maximum Safe Operation Area (TO-251S)



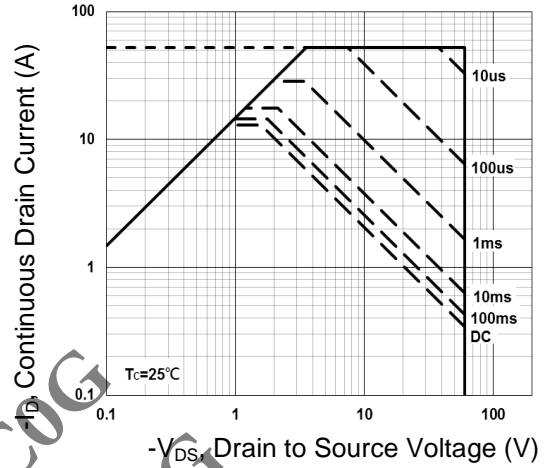
CHARACTERISTICS CURVES

($T_c = 25^\circ\text{C}$ unless otherwise noted)

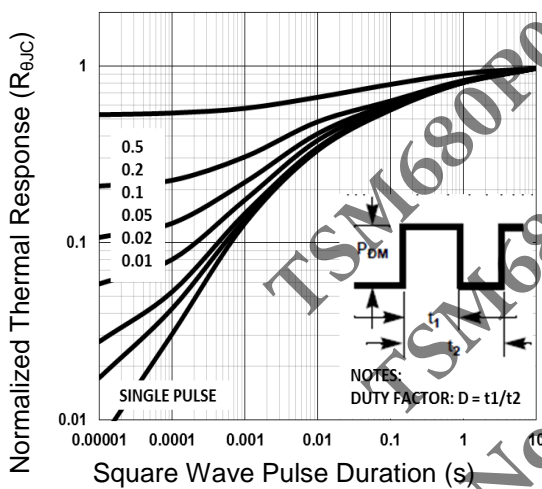
Normalized Transient Impedance (TO-252)



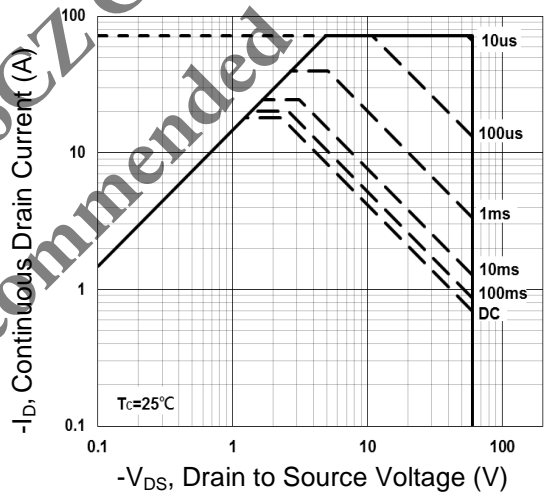
Maximum Safe Operation Area (TO-252)



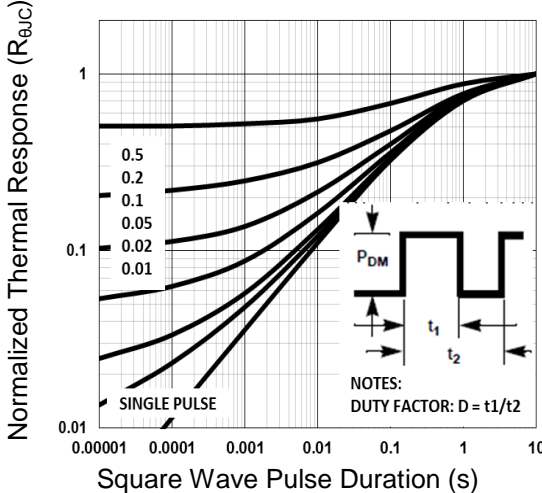
Normalized Transient Impedance (TO-220)



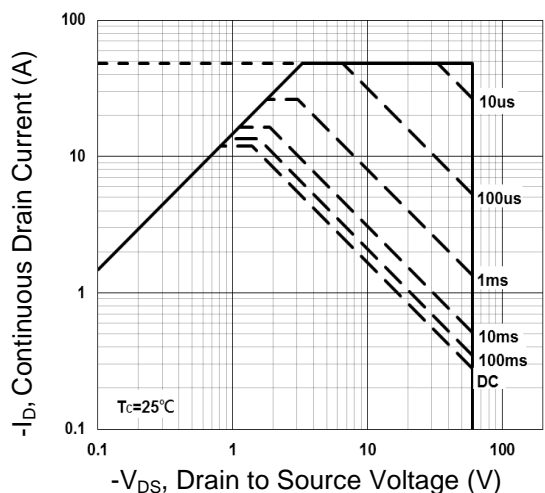
Maximum Safe Operation Area (TO-220)



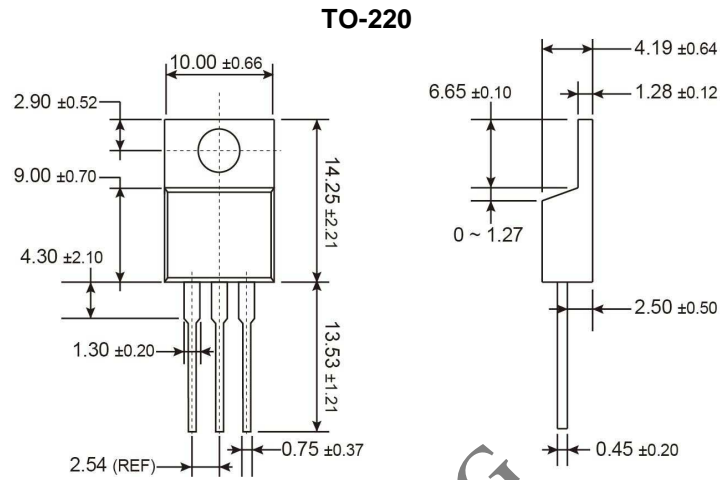
Normalized Transient Impedance (ITO-220)



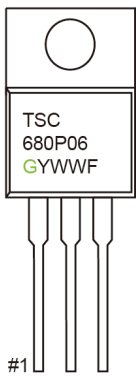
Maximum Safe Operation Area (ITO-220)



PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)



MARKING DIAGRAM



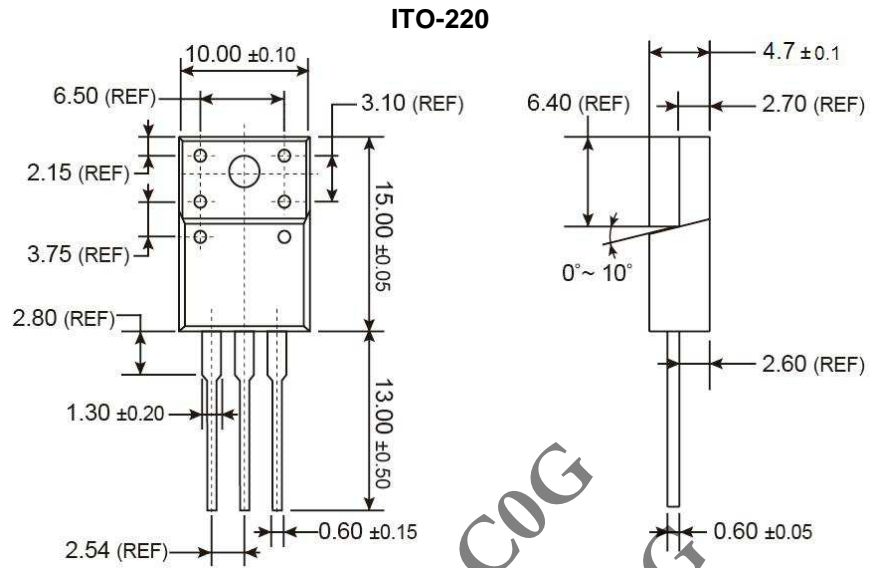
- G** = Halogen Free
- Y** = Year Code
- WW** = Week Code (01~52)
- F** = Factory Code

TSM680P06CI COG

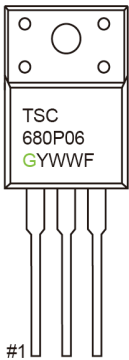
TSM680P06CZ COG

Not Recommended

PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)



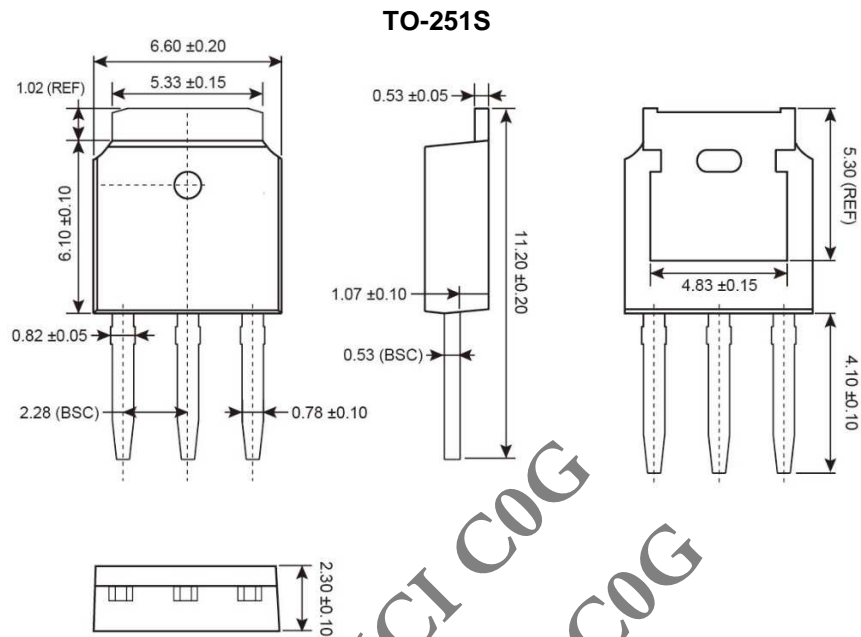
MARKING DIAGRAM



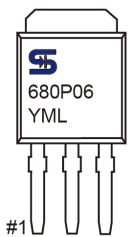
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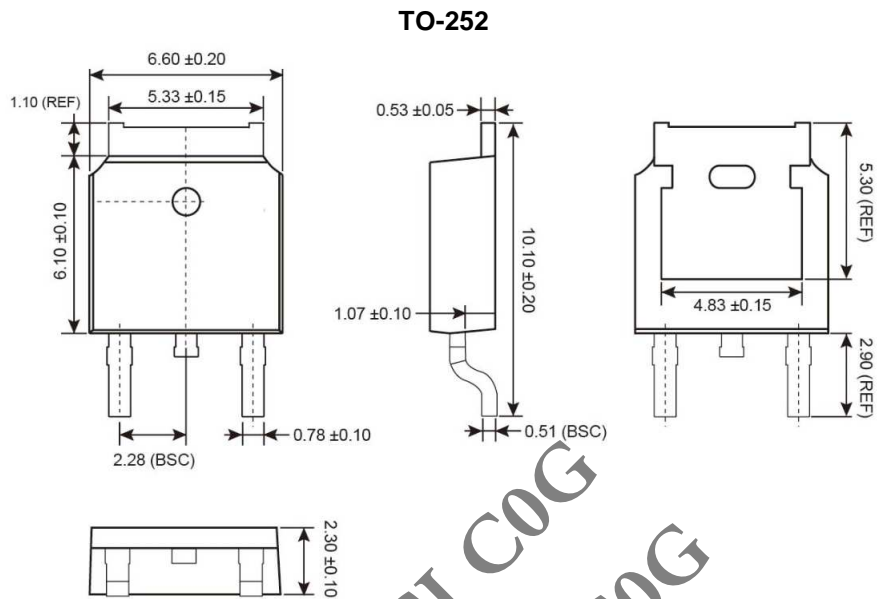
MARKING DIAGRAM



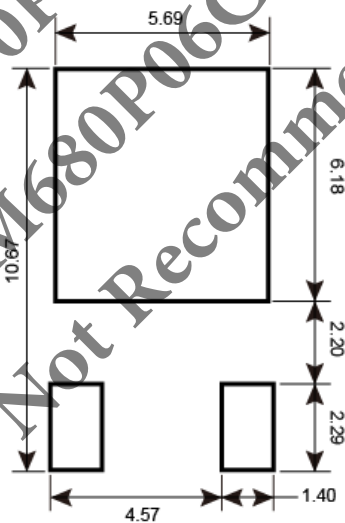
- Y** = Year Code
- M** = Month Code for Halogen Free Product
 - O** =Jan **P** =Feb **Q** =Mar **R** =Apr
 - S** =May **T** =Jun **U** =Jul **V** =Aug
 - W** =Sep **X** =Oct **Y** =Nov **Z** =Dec
- L** = Lot Code (1~9, A~Z)

TSM680P06CI COG
Not Recommended
TSM680P06CZ COG

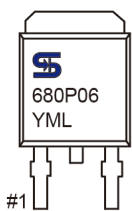
PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)



SUGGESTED PAD LAYOUT



MARKING DIAGRAM



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TSM680P06CI COG
TSM680P06CZ COG
Not Recommended

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