

## N-Channel Power MOSFET

700V, 3.3A, 1.4Ω

### FEATURES

- Super-Junction technology
- High performance due to small figure-of-merit
- High ruggedness performance
- High commutation performance

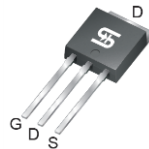
### APPLICATION

- Power Supply
- Lighting

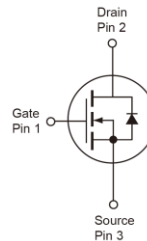
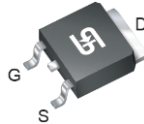
KEY PERFORMANCE PARAMETERS		
PARAMETER	VALUE	UNIT
$V_{DS}$	700	V
$R_{DS(on)}$ (max)	1.4	Ω
$Q_g$	7.7	nC



TO-251 (IPAK)



TO-252 (DPAK)



**Notes:** MSL 3 (Moisture Sensitivity Level) for TO-252 (D-PAK) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	700	V
Gate-Source Voltage	$V_{GS}$	±30	V
Continuous Drain Current <sup>(Note 1)</sup>	$I_D$	$T_C = 25^\circ\text{C}$	3.3
		$T_C = 100^\circ\text{C}$	2.0
Pulsed Drain Current <sup>(Note 2)</sup>	$I_{DM}$	9.9	A
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	$P_{DTOT}$	38	W
Single Pulsed Avalanche Energy <sup>(Note 3)</sup>	$E_{AS}$	64	mJ
Single Pulsed Avalanche Current <sup>(Note 3)</sup>	$I_{AS}$	1.6	A
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	- 55 to +150	°C

THERMAL PERFORMANCE			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	3.3	°C/W
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	62	°C/W

**Notes:**  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins.  $R_{\theta JA}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.  $R_{\theta JA}$  shown below for single device operation on FR-4 PCB in still air.

<b>ELECTRICAL SPECIFICATIONS</b> ( $T_C = 25^\circ\text{C}$ unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
<b>Static</b> (Note 4)						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	$BV_{DSS}$	700	--	--	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	$V_{GS(TH)}$	2	3	4	V
Gate Body Leakage	$V_{GS} = \pm 30V, V_{DS} = 0V$	$I_{GSS}$	--	--	$\pm 100$	nA
Zero Gate Voltage Drain Current	$V_{DS} = 700V, V_{GS} = 0V$	$I_{DSS}$	--	--	1	$\mu A$
Drain-Source On-State Resistance	$V_{GS} = 10V, I_D = 1.2A$	$R_{DS(ON)}$	--	0.9	1.4	$\Omega$
<b>Dynamic</b> (Note 5)						
Total Gate Charge	$V_{DS} = 380V, I_D = 3.3A,$ $V_{GS} = 10V$	$Q_g$	--	7.7	--	nC
Gate-Source Charge		$Q_{gs}$	--	1.9	--	
Gate-Drain Charge		$Q_{gd}$	--	2.8	--	
Input Capacitance	$V_{DS} = 100V, V_{GS} = 0V,$ $f = 1.0MHz$	$C_{iss}$	--	370	--	pF
Output Capacitance		$C_{oss}$	--	34	--	
Gate Resistance	$F = 1MHz, \text{open drain}$	$R_g$	--	3.4	--	$\Omega$
<b>Switching</b> (Note 6)						
Turn-On Delay Time	$V_{DD} = 380V,$ $R_{GEN} = 25\Omega,$ $I_D = 3.3A, V_{GS} = 10V,$	$t_{d(on)}$	--	14	--	ns
Turn-On Rise Time		$t_r$	--	22	--	
Turn-Off Delay Time		$t_{d(off)}$	--	24	--	
Turn-Off Fall Time		$t_f$	--	20	--	
<b>Source-Drain Diode</b> (Note 4)						
Forward On Voltage	$I_S = 3.3A, V_{GS} = 0V$	$V_{SD}$	--	--	1.4	V
Reverse Recovery Time	$V_R = 200V, I_S = 2A$	$t_{rr}$	--	163	--	ns
Reverse Recovery Charge		$di_f/dt = 100A/\mu s$	$Q_{rr}$	--	1	--

**Notes:**

1. Current limited by package
2. Pulse width limited by the maximum junction temperature
3.  $L = 50mH, I_{AS} = 1.6A, V_{DD} = 50V, R_G = 25\Omega, \text{Starting } T_J = 25^\circ\text{C}$
4. Pulse test:  $PW \leq 300\mu s, \text{duty cycle} \leq 2\%$
5. For DESIGN AID ONLY, not subject to production testing.
6. Switching time is essentially independent of operating temperature.

**ORDERING INFORMATION**

<b>PART NO.</b>	<b>PACKAGE</b>	<b>PACKING</b>
TSM70N1R4CH C5G	TO-251 (IPAK)	75pcs / Tube
TSM70N1R4CP ROG	TO-252 (DPAK)	2,500pcs / 13" Reel

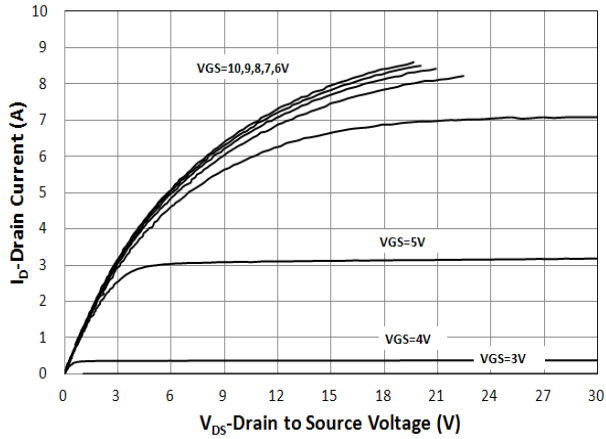
**Note:**

1. Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC
2. Halogen-free according to IEC 61249-2-21 definition

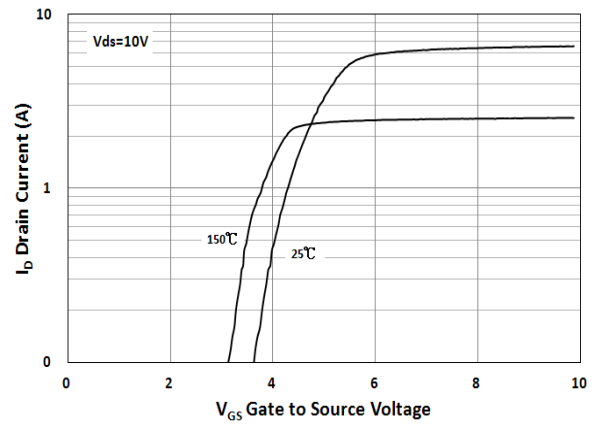
**CHARACTERISTICS CURVES**

( $T_C = 25^\circ\text{C}$  unless otherwise noted)

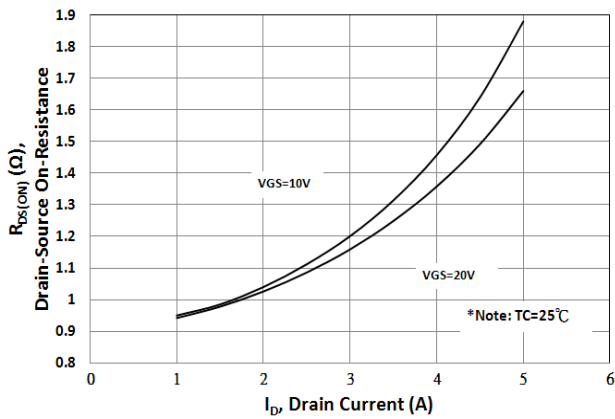
**Output Characteristics**



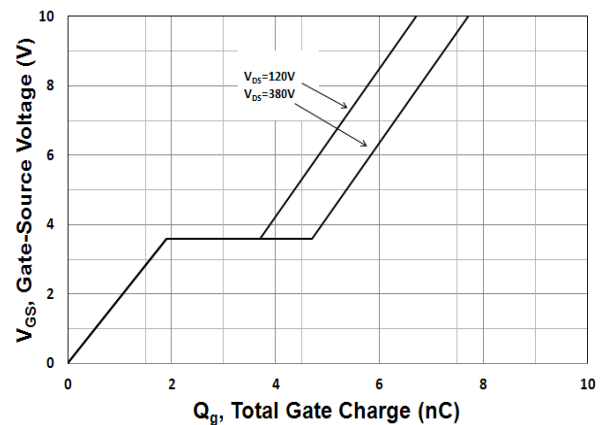
**Transfer Characteristics**



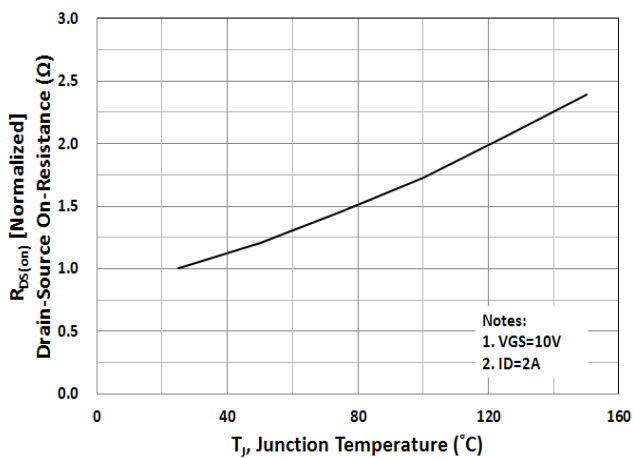
**On-Resistance vs. Drain Current**



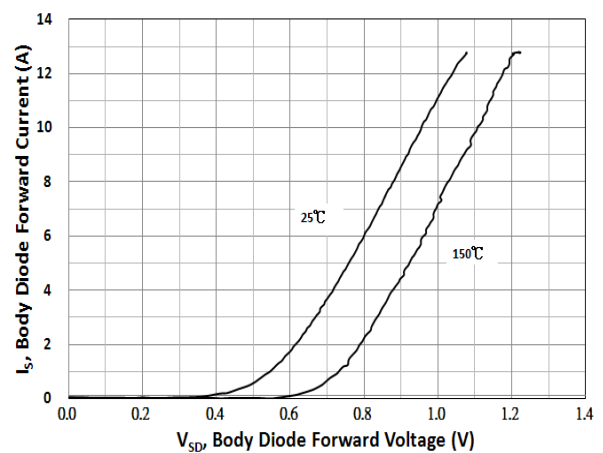
**Gate-Source Voltage vs. Gate Charge**



**On-Resistance vs. Junction Temperature**



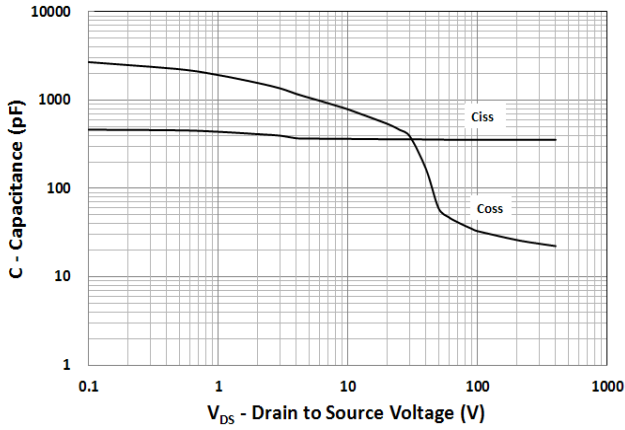
**Source-Drain Diode Forward Current vs. Voltage**



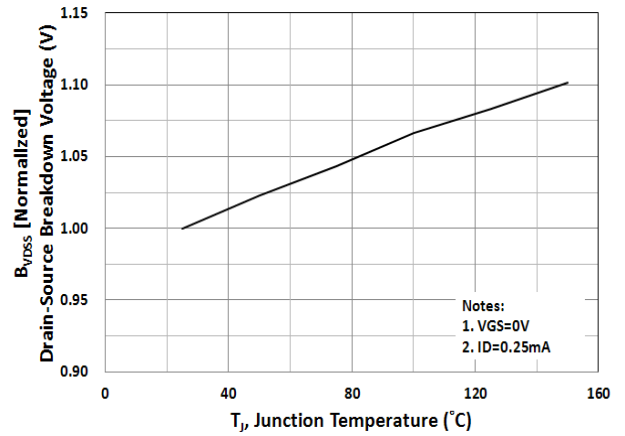
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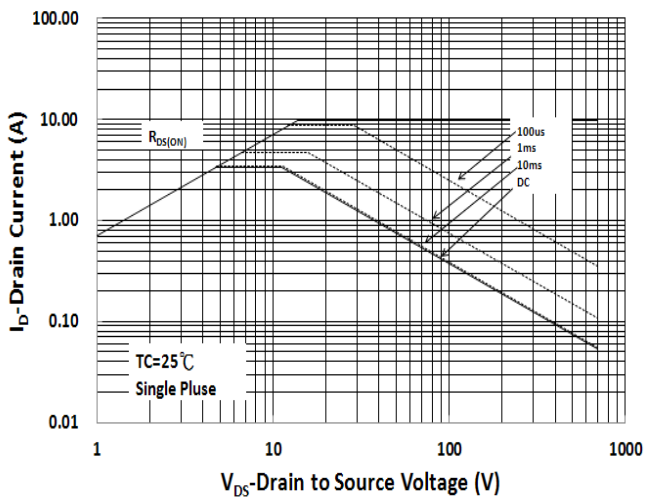
**Capacitance vs. Drain-Source Voltage**



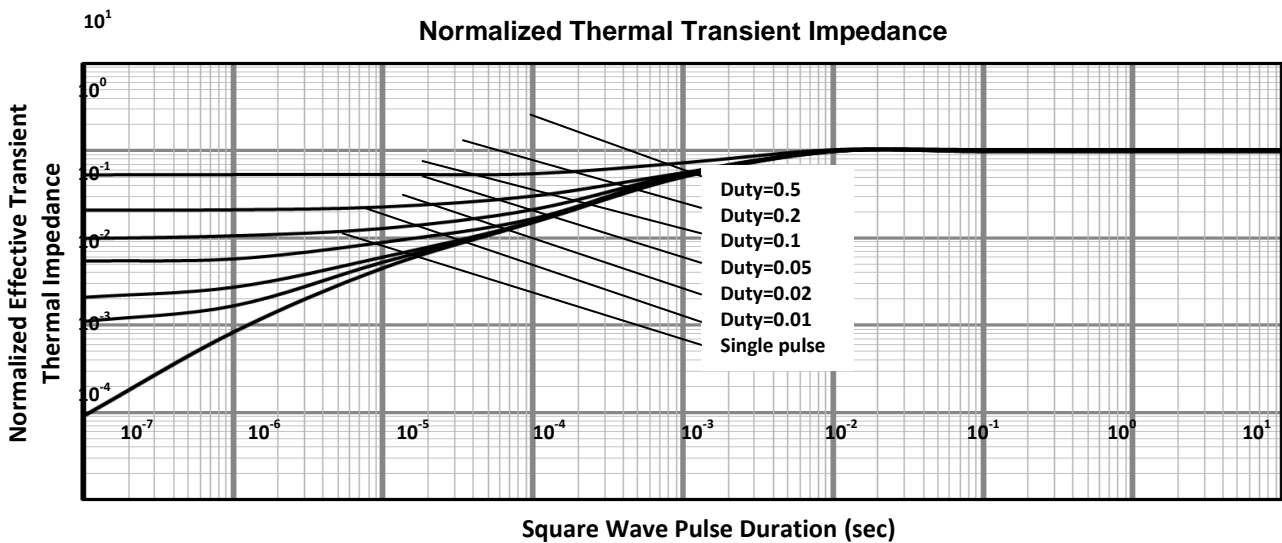
**$BV_{DSS}$  vs. Junction Temperature**



**Maximum Safe Operating Area**

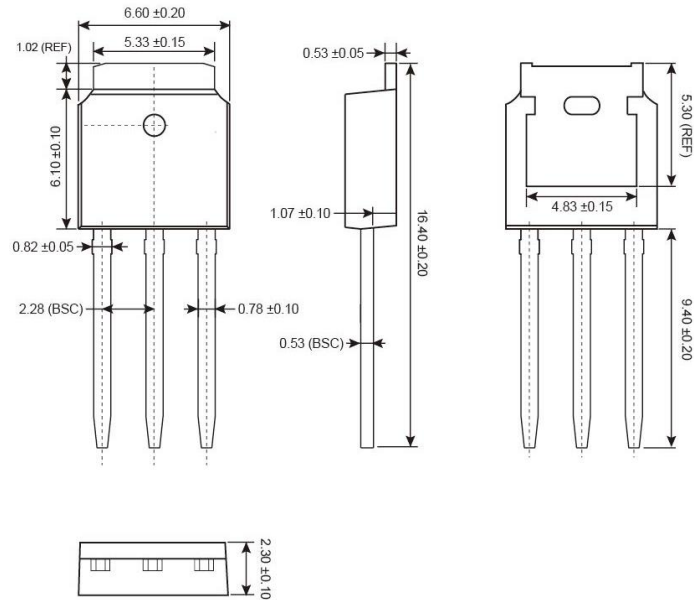


**Normalized Thermal Transient Impedance**

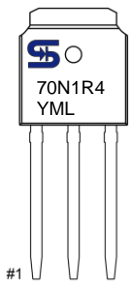


**PACKAGE OUTLINE DIMENSIONS** (Unit: Millimeters)

**TO-251 (IPAK)**

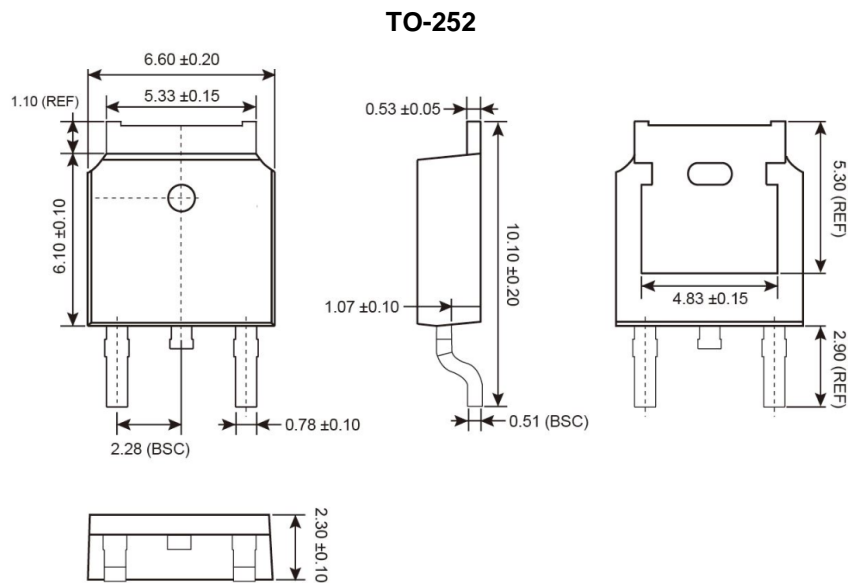


**MARKING DIAGRAM**

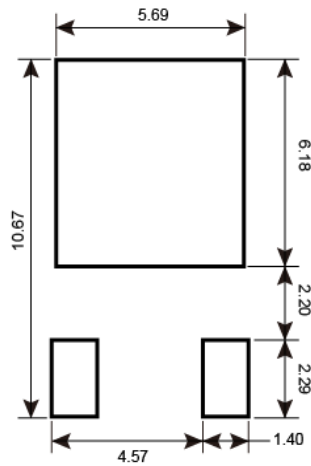


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- M** = Month Code for Halogen Free Product
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- L** = Lot Code (1~9, A~Z)

**PACKAGE OUTLINE DIMENSIONS** (Unit: Millimeters)



**SUGGESTED PAD LAYOUT** (Unit: Millimeters)



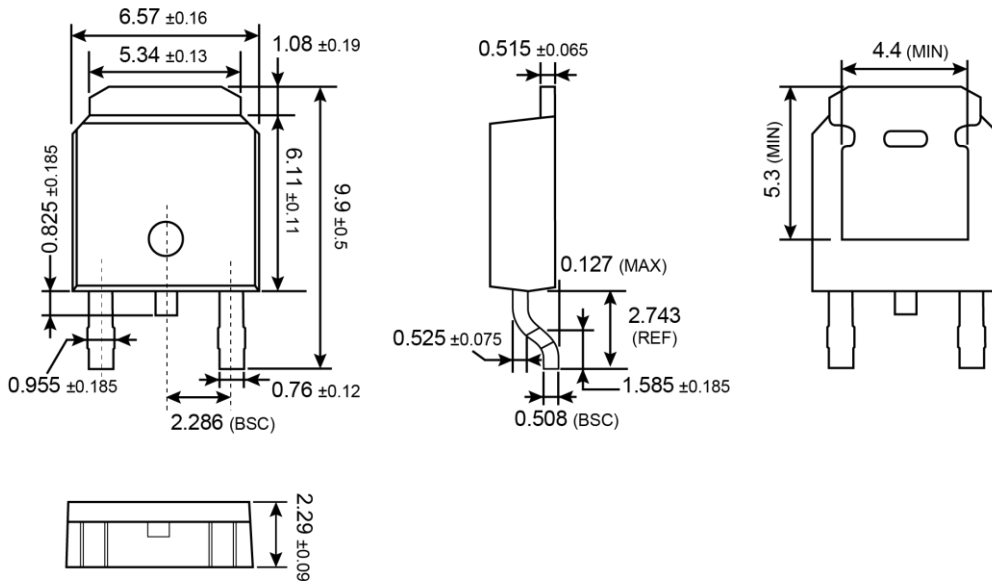
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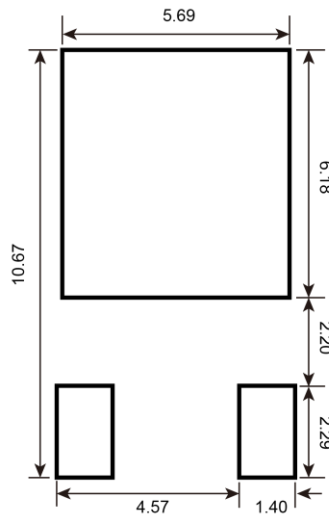
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**PACKAGE OUTLINE DIMENSIONS** (Unit: Millimeters)

**TO-252**



**SUGGESTED PAD LAYOUT** (Unit: Millimeters)



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