

N-Channel Power MOSFET

800V, 5.5A, 1.2Ω

FEATURES

- Super-Junction technology
- High performance due to small figure-of-merit
- High ruggedness performance
- High commutation performance
- Pb-free plating
- Compliant to RoHS Directive 2011/65/EU and in accordance to WEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21 definition

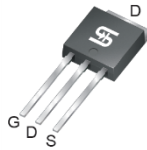
KEY PERFORMANCE PARAMETERS		
PARAMETER	VALUE	UNIT
V_{DS}	800	V
$R_{DS(on)}$ (max)	1.2	Ω
Q_g	19.4	nC

APPLICATION

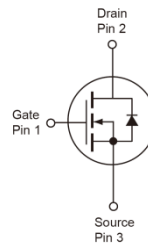
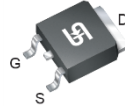
- Power Supply
- Lighting



TO-251 (IPAK)



TO-252 (DPAK)



Notes: MSL 3 (Moisture Sensitivity Level) for TO-252 (D-PAK) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	800	V
Gate-Source Voltage	V_{GS}	±30	V
Continuous Drain Current ^(Note 1)	I_D	$T_C = 25^\circ\text{C}$	5.5
		$T_C = 100^\circ\text{C}$	3.4
Pulsed Drain Current ^(Note 2)	I_{DM}	16.5	A
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_{DTOT}	110	W
Single Pulsed Avalanche Energy ^(Note 3)	E_{AS}	121	mJ
Single Pulsed Avalanche Current ^(Note 3)	I_{AS}	2.2	A
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to +150	°C

THERMAL PERFORMANCE

PARAMETER	SYMBOL	LIMIT	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	1.14	$^{\circ}\text{C}/\text{W}$
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	62	$^{\circ}\text{C}/\text{W}$

Notes: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 PCB with minimum recommended footprint in still air.

ELECTRICAL SPECIFICATIONS ($T_A = 25^{\circ}\text{C}$ unless otherwise noted)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static (Note 4)						
Drain-Source Breakdown Voltage	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$	BV_{DSS}	800	--	--	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	$V_{GS(TH)}$	2	--	4	V
Gate Body Leakage	$V_{GS} = \pm 30\text{V}, V_{DS} = 0\text{V}$	I_{GSS}	--	--	± 100	nA
Zero Gate Voltage Drain Current	$V_{DS} = 800\text{V}, V_{GS} = 0\text{V}$	I_{DSS}	--	--	1	μA
Drain-Source On-State Resistance	$V_{GS} = 10\text{V}, I_D = 2.75\text{A}$	$R_{DS(on)}$	--	0.9	1.2	Ω
Dynamic (Note 5)						
Total Gate Charge	$V_{DS} = 380\text{V}, I_D = 5.5\text{A},$ $V_{GS} = 10\text{V}$	Q_g	--	19.4	--	nC
Gate-Source Charge		Q_{gs}	--	3.4	--	
Gate-Drain Charge		Q_{gd}	--	9.6	--	
Input Capacitance	$V_{DS} = 100\text{V}, V_{GS} = 0\text{V},$ $f = 1.0\text{MHz}$	C_{iss}	--	685	--	pF
Output Capacitance		C_{oss}	--	62	--	
Gate Resistance	$F = 1\text{MHz}, \text{open drain}$	R_g	--	3.4	--	Ω
Switching (Note 6)						
Turn-On Delay Time	$V_{DD} = 380\text{V},$ $R_{GEN} = 25\Omega,$ $I_D = 5.5\text{A}, V_{GS} = 10\text{V},$	$t_{d(on)}$	--	22	--	ns
Turn-On Rise Time		t_r	--	11	--	
Turn-Off Delay Time		$t_{d(off)}$	--	55	--	
Turn-Off Fall Time		t_f	--	10	--	
Source-Drain Diode (Note 4)						
Forward On Voltage	$I_S = 5.5\text{A}, V_{GS} = 0\text{V}$	V_{SD}	--	--	1.4	V
Reverse Recovery Time	$V_R = 100\text{V}, I_S = 5.5\text{A}$ $di_f/dt = 100\text{A}/\mu\text{s}$	t_{rr}	--	240	--	ns
Reverse Recovery Charge		Q_{rr}	--	2.5	--	μC

Notes:

- Current limited by package.
- Pulse width limited by the maximum junction temperature.
- $L = 50\text{mH}, I_{AS} = 2.2\text{A}, V_{DD} = 50\text{V}, R_G = 25\Omega,$ Starting $T_J = 25^{\circ}\text{C}$
- Pulse test: $PW \leq 300\mu\text{s}, \text{duty cycle} \leq 2\%$.
- For DESIGN AID ONLY, not subject to production testing.
- Switching time is essentially independent of operating temperature.

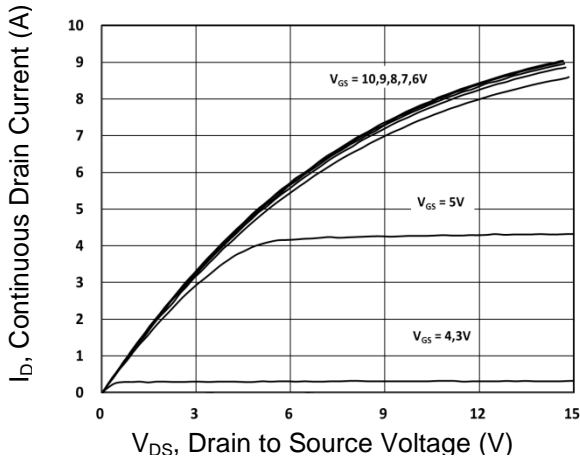
ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM80N1R2CH C5G	TO-251 (IPAK)	75pcs / Tube
TSM80N1R2CP ROG	TO-252 (DPAK)	2,500pcs / 13" Reel

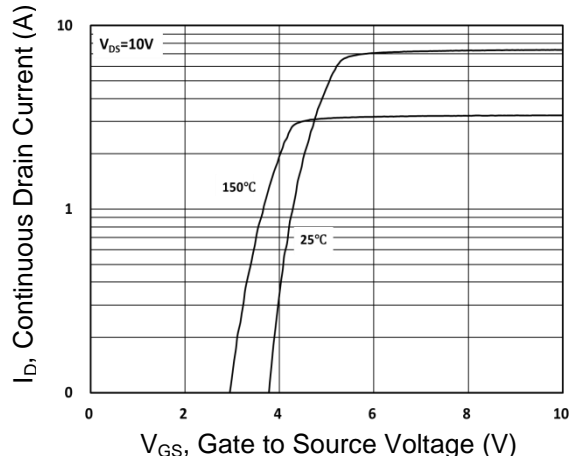
CHARACTERISTICS CURVES

($T_c = 25^\circ\text{C}$ unless otherwise noted)

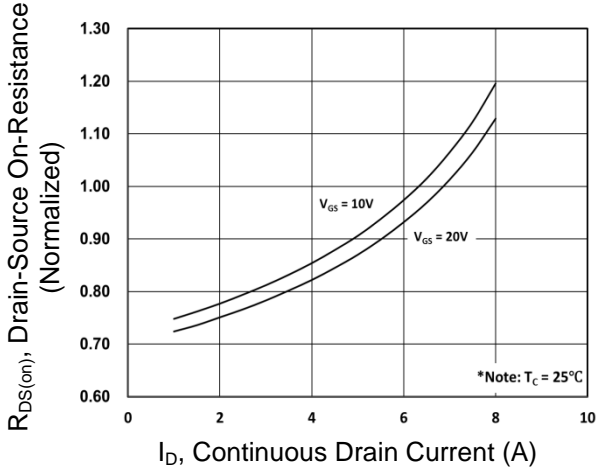
Output Characteristics



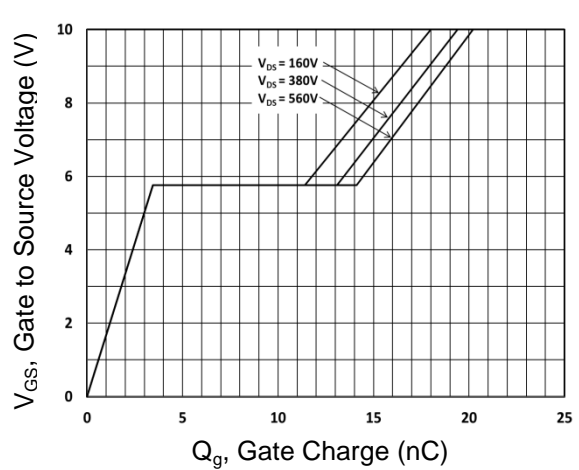
Transfer Characteristics



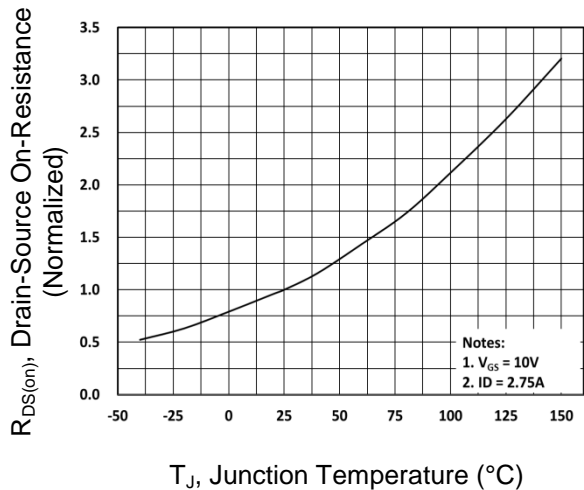
On-Resistance vs. Drain Current



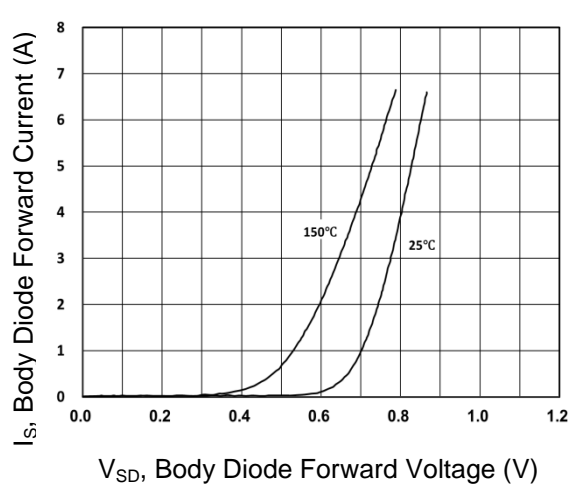
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



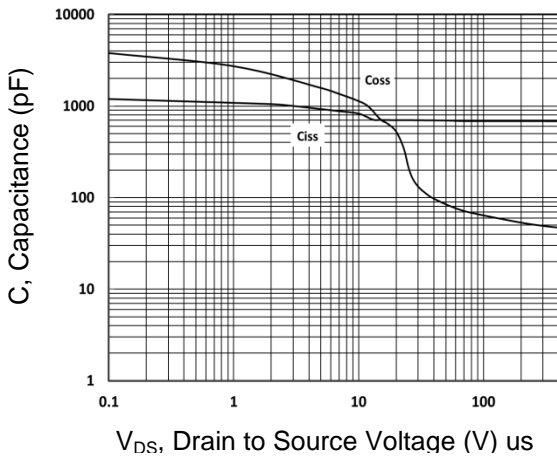
Source-Drain Diode Forward Current vs. Voltage



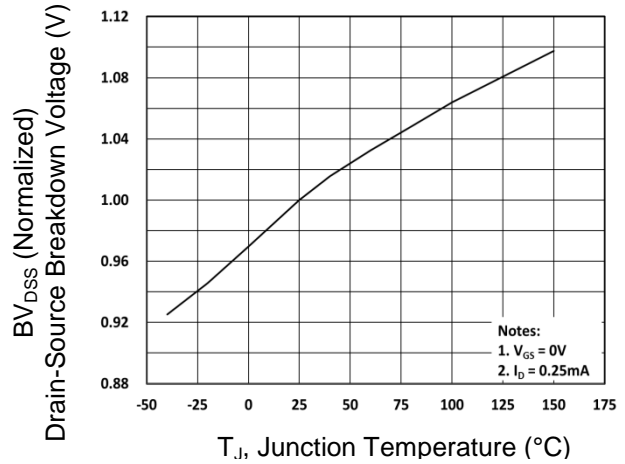
CHARACTERISTICS CURVES

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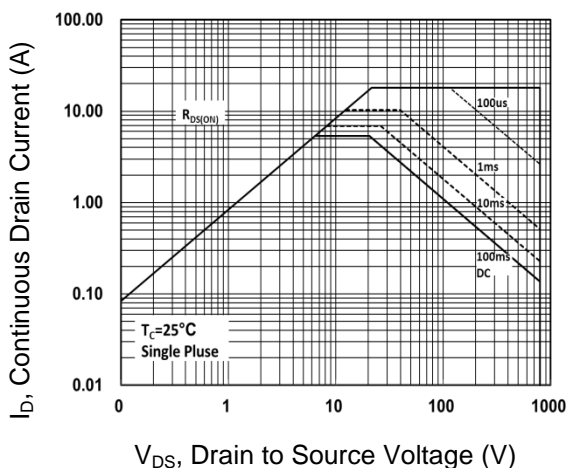
Capacitance vs. Drain-Source Voltage



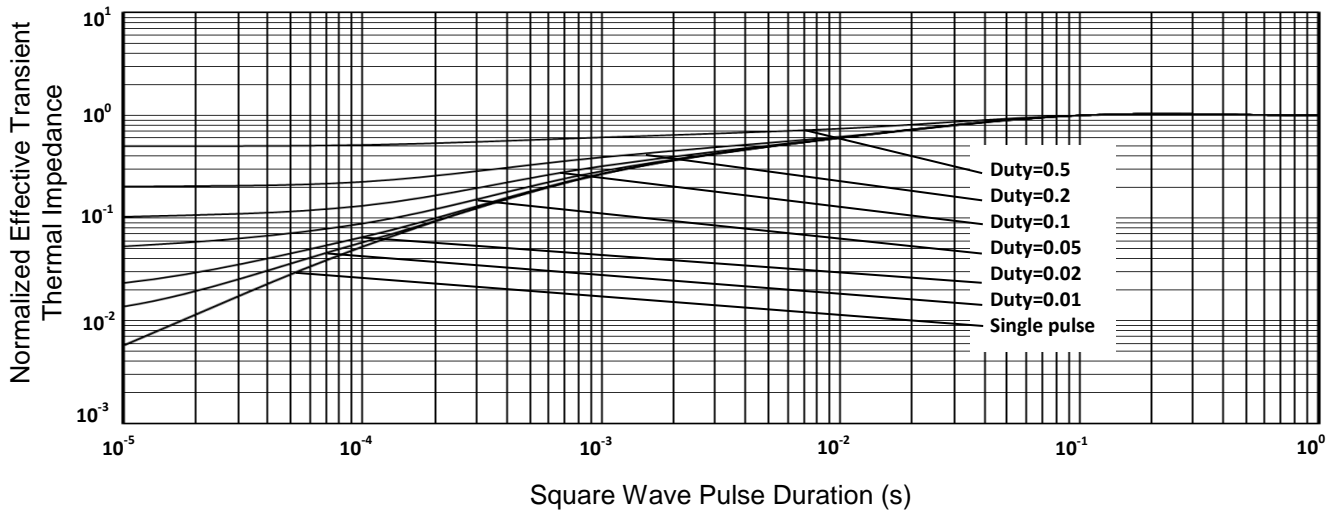
BV_{DSS} vs. Junction Temperature



Maximum Safe Operating Area

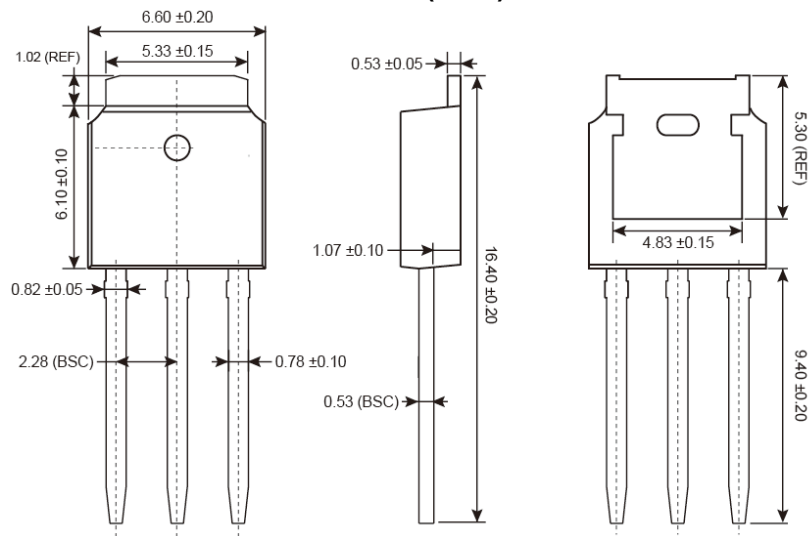


Normalized Thermal Transient Impedance, Junction-to-Case

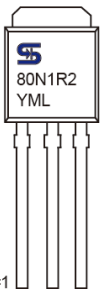


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

TO-251 (IPAK)



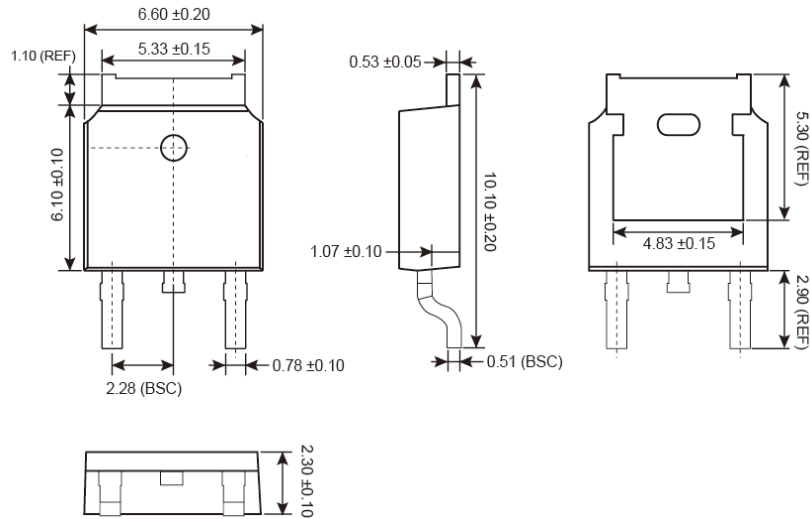
MARKING DIAGRAM



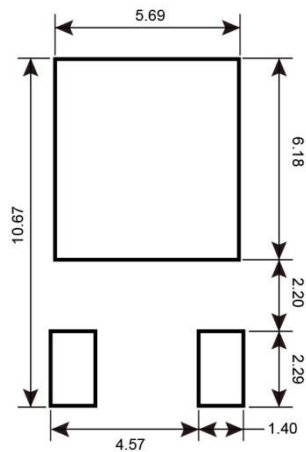
- Y** = Year Code
- M** = Month Code for Halogen Free Product
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PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

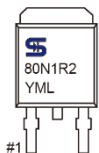
TO-252 (DPAK)



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



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