N-Channel Power MOSFET

100V, 6.5A, 95mΩ

FEATURES

- Fast switching
- Pb-free plating
- RoHS compliant
- Halogen-free mold compound

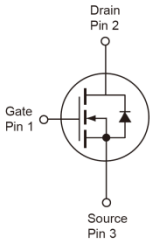
APPLICATION

- Networking
- Load Switch
- Lighting

KEY PERFORMANCE PARAMETERS			
PARAMETER		**VALUE**	**UNIT**
V_{DS}		100	V
$R_{DS(on)}$ (max)	V_{GS} = 10V	95	mΩ
	V_{GS} = 4.5V	110	
Q_g		9.3	nC

Pb-Free RoHS COMPLIANT HALOGEN FREE

SOT-223



Note: MSL 3 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)				
PARAMETER		**SYMBOL**	**LIMIT**	**UNIT**
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current (Note 1)	T_C = 25°C	I_D	6.5	A
	T_C = 100°C		4.1	
Pulsed Drain Current (Note 2)		I_{DM}	26	A
Total Power Dissipation @ T_C = 25°C		P_{DTOT}	9	W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +150	°C

THERMAL PERFORMANCE			
PARAMETER	**SYMBOL**	**LIMIT**	**UNIT**
Junction to Case Thermal Resistance	$R_{\Theta JC}$	14	°C/W
Junction to Ambient Thermal Resistance	$R_{\Theta JA}$	62	°C/W

Notes: $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\Theta JC}$ is guaranteed by design while $R_{\Theta CA}$ is determined by the user's board design. $R_{\Theta JA}$ shown below for single device operation on FR-4 PCB in still air

ELECTRICAL SPECIFICATIONS (T_A = 25°C unless otherwise noted)						
PARAMETER	**CONDITIONS**	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
Static (Note 3)						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	BV_{DSS}	100	--	--	V
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	$V_{GS(TH)}$	1.2	1.6	2.5	V
Gate Body Leakage	V_{GS} = ±20V, V_{DS} = 0V	I_{GSS}	--	--	±100	nA
Zero Gate Voltage Drain Current	V_{DS} = 100V, V_{GS} = 0V	I_{DSS}	--	--	1	μA
Drain-Source On-State Resistance	V_{GS} = 10V, I_D = 5A	$R_{DS(on)}$	--	80	95	mΩ
	V_{GS} = 4.5V, I_D = 3A		--	85	110	
Dynamic (Note 4)						
Total Gate Charge	V_{DS} = 48V, I_D = 5A, V_{GS} = 10V	Q_g	--	9.3	--	nC
Gate-Source Charge		Q_{gs}	--	2.1	--	
Gate-Drain Charge		Q_{gd}	--	1.8	--	
Input Capacitance	V_{DS} = 50V, V_{GS} = 0V, f = 1.0MHz	C_{iss}	--	1480	--	pF
Output Capacitance		C_{oss}	--	480	--	
Reverse Transfer Capacitance		C_{rss}	--	35	--	
Gate Resistance	f = 1MHz, open drain	R_g	--	1.3	--	Ω
Switching (Note 5)						
Turn-On Delay Time	V_{DD} = 30V, R_{GEN} = 3.3Ω, I_D = 1A, V_{GS} = 10V,	$t_{d(on)}$	--	2.9	--	ns
Turn-On Rise Time		t_r	--	9.5	--	
Turn-Off Delay Time		$t_{d(off)}$	--	18.4	--	
Turn-Off Fall Time		t_f	--	5.3	--	
Source-Drain Diode (Note 3)						
Forward On Voltage	I_S = 3.3A, V_{GS} = 0V	V_{SD}	--	--	1	V
Continuous Drain-Source Diode		I_S	--	--	6.5	A
Pulse Drain-Source Diode		I_{SM}	--	--	26	A

Notes:

1. Current limited by package
2. Pulse width limited by the maximum junction temperature
3. Pulse test: PW ≤ 300μs, duty cycle ≤ 2%
4. For DESIGN AID ONLY, not subject to production testing.
5. Switching time is essentially independent of operating temperature.

ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TSM950N10CW RPG	SOT-223	2,500pcs / 13” Reel

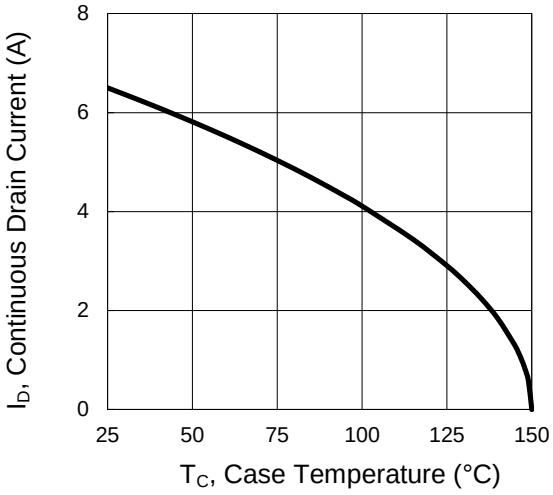
Note:

1. Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC
2. Halogen-free according to IEC 61249-2-21 definition

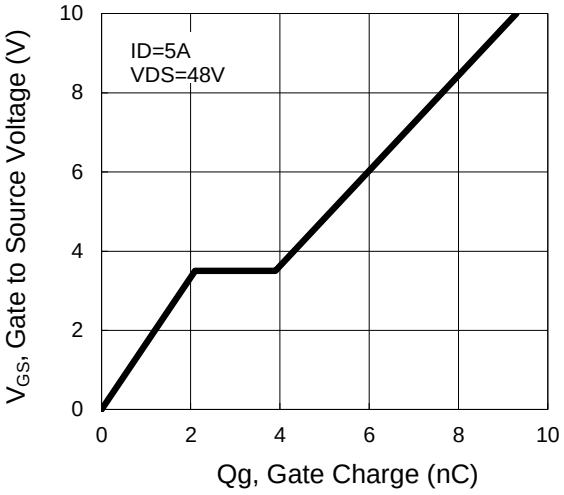
CHARACTERISTICS CURVES

(T_C = 25°C unless otherwise noted)

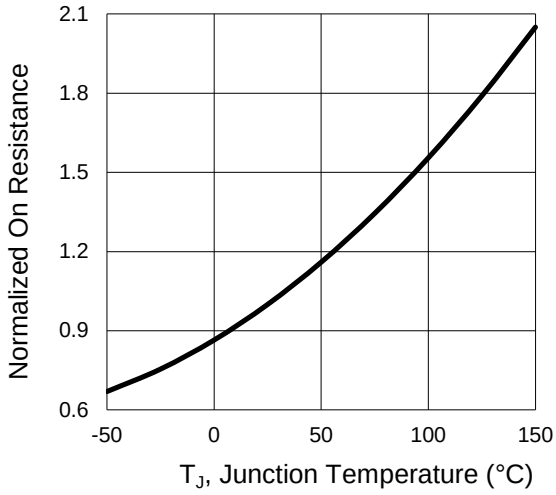
Continuous Drain Current vs. T_C



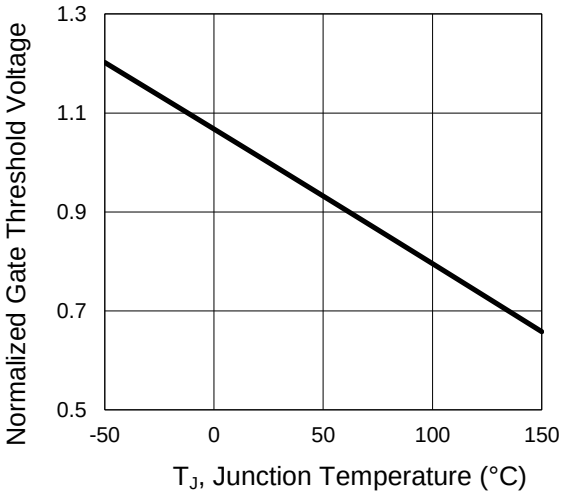
Gate Charge



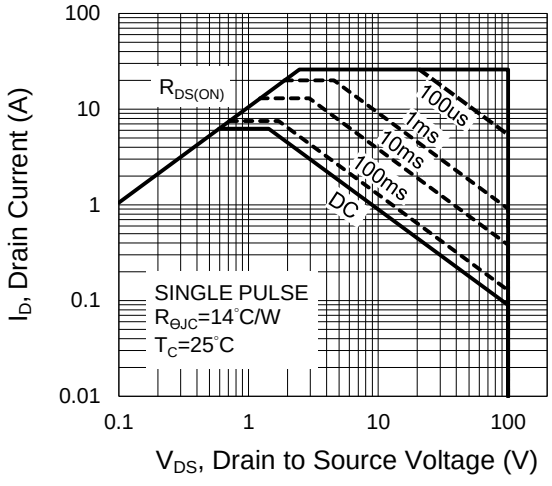
On-Resistance vs. Junction Temperature



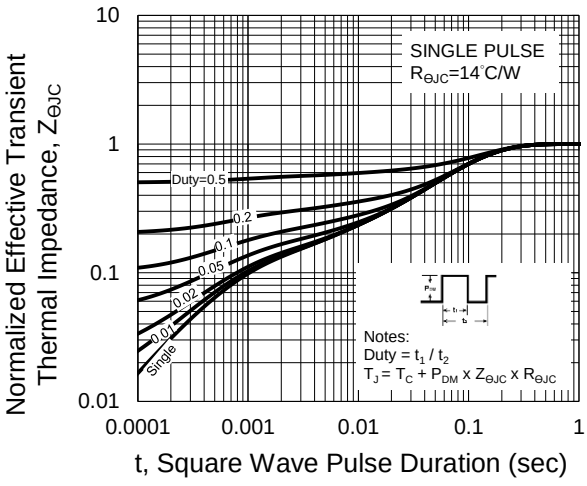
Threshold Voltage vs. Junction Temperature



Maximum Safe Operating Area

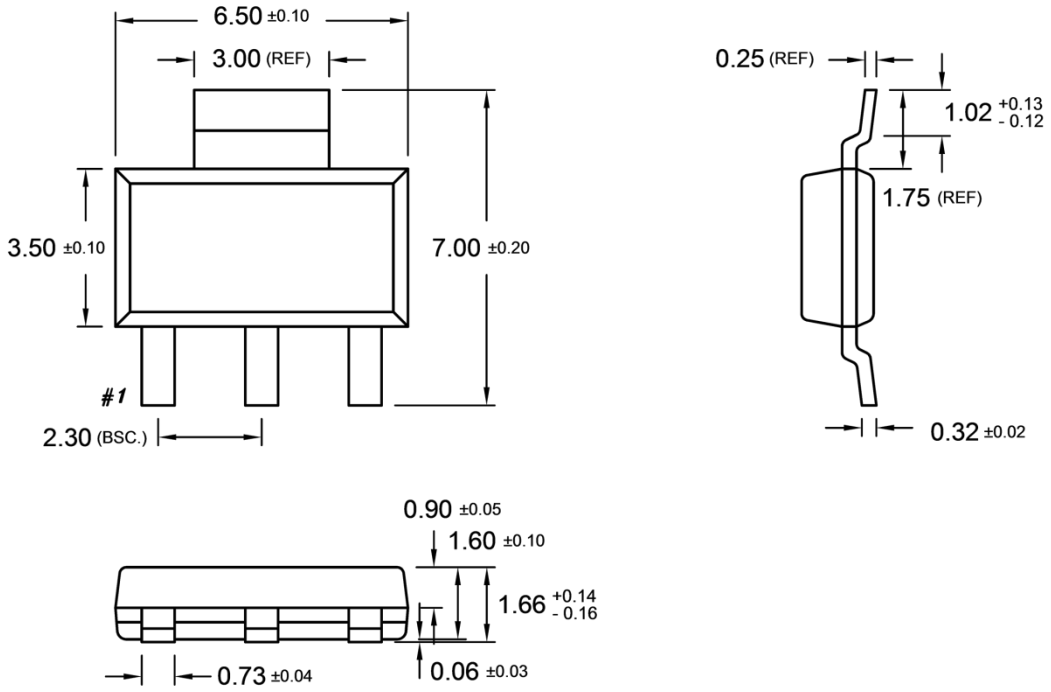


Normalized Thermal Transient Impedance Curve

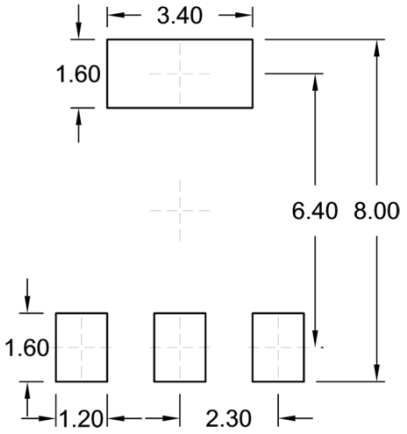


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

SOT-223



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM

Y = Year Code

M = Month Code for Halogen Free Product

O	=Jan	**P**	=Feb	**Q**	=Mar	**R**	=Apr
S	=May	**T**	=Jun	**U**	=Jul	**V**	=Aug
W	=Sep	**X**	=Oct	**Y**	=Nov	**Z**	=Dec

L = Lot Code (1~9, A~Z)

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